Development of novel high-voltage CMOS sensors (several themes)

Introduction, what is high-voltage CMOS sensor?

CMOS pixel sensor is now days the most often used imaging device. The sensor part (usually based on an n-well in p-substrate – a diode) and the readout electronics are implemented on the same chip. The photons produce electron-hole pairs at the surface of p-substrate and the electrons move by diffusion to the n-well, get collected and amplified.

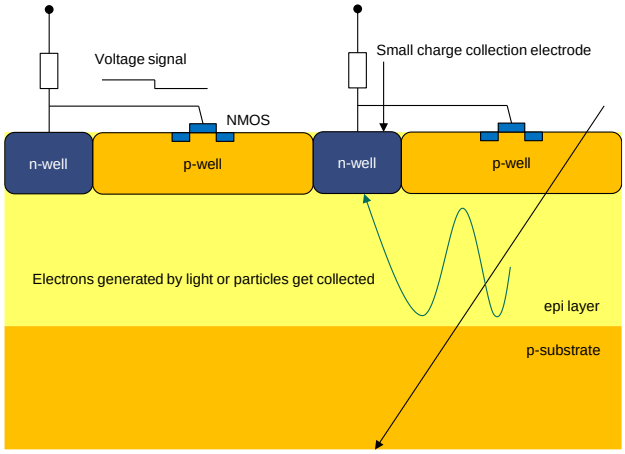

Figure 1: CMOS pixel sensor – cross section

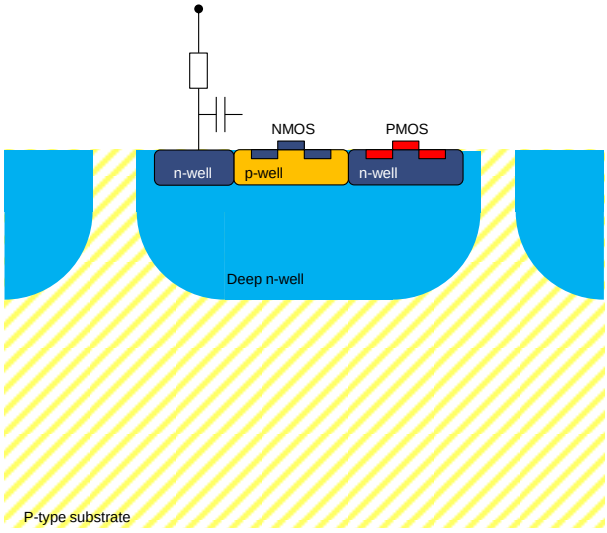

Figure 2: High-voltage CMOS pixel sensor – cross section

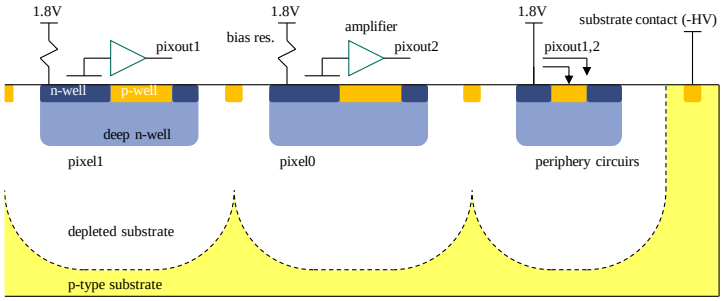

Figure 3: Pixel electronics is placed inside sensor electrode (deep n-well)

In the high voltage CMOS (HVCMOS) sensors, high reverse bias voltage is applied to the sensor diode. In this way, relatively large sensor volume, below the n-well, is depleted. The electrons generated by photons or ionizing particles in this depleted region are quickly collected by drift. Because the sensor volume is much deeper and charge collection faster that in the standard sensor, a high voltage CMOS sensor can detect not only light, but also single ionizing particles provided they generate enough number of electron-hole pairs to exceed the detection threshold (~several 100e). HVCMOS sensor makes visible the particles and radiation which cannot be detected with the standard CMOS sensors or our eyes. Several innovative solutions were needed to isolate the transistors from the high voltage. One of them is placing of amplifiers inside the sensor electrode (n-well). The sensors must work under extreme conditions – strong radiation environment, strong magnetic field and very low temperatures. Special design techniques and device modelling is required.

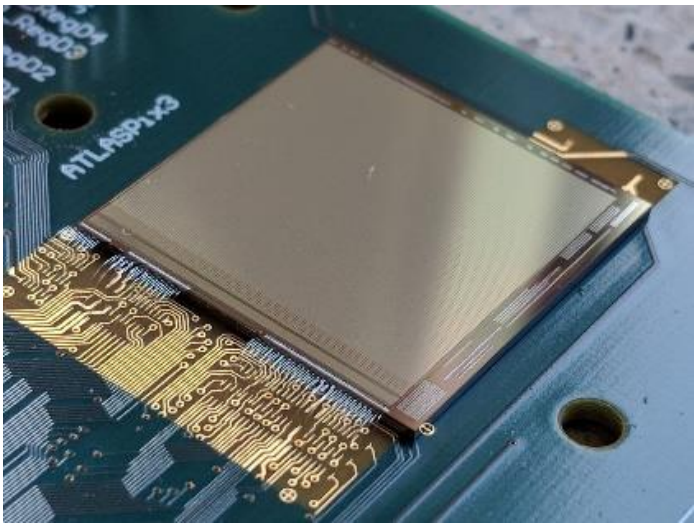

Figure 4: Photo of Atlaspix chip

Example of an HVCMOS sensor

An example of a HVCMOS sensor is the Atlaspix chip designed at KIT ADL. Atlaspix has been implemented in a 180nm HVCMOS process of foundry TSI. The chip has a size of 2.1 cm x 2.0 cm, it occupies entire reticle. Atlaspix contains analogue and digital circuits, it is a mixed mode system on a chip. Every pixel contains an amplifier that amplify signal produced by a particle. Amplified signal is shaped to a triangular form. A comparator converts the analogue signal to a digital pulse. Its threshold is set low enough to detect the signals and high enough to be insensitive to noise.

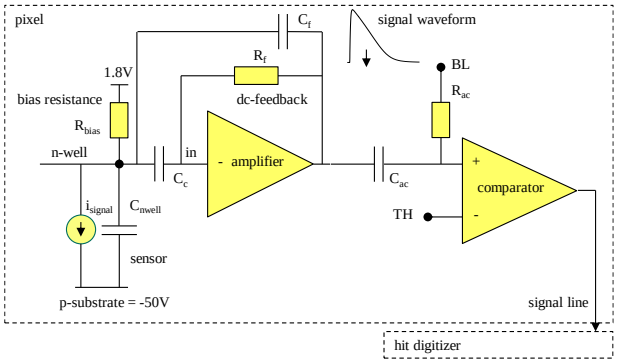

Figure 5: Pixel electronics

Comparator signals are transmitted to the periphery. Hit buffers (one per pixel) measure arrival time and duration of the pulses. They generate information (hit-words) about particle hit (arrival time, pixel address, duration). The hit-words from the buffers are filtered by their time using content addressable memory. Large synthesized digital part controls the data transfer, performs data multiplexing, formatting. The data are then serialized and sent using Gbit data links. All blocks and the full system have been developed in our group.

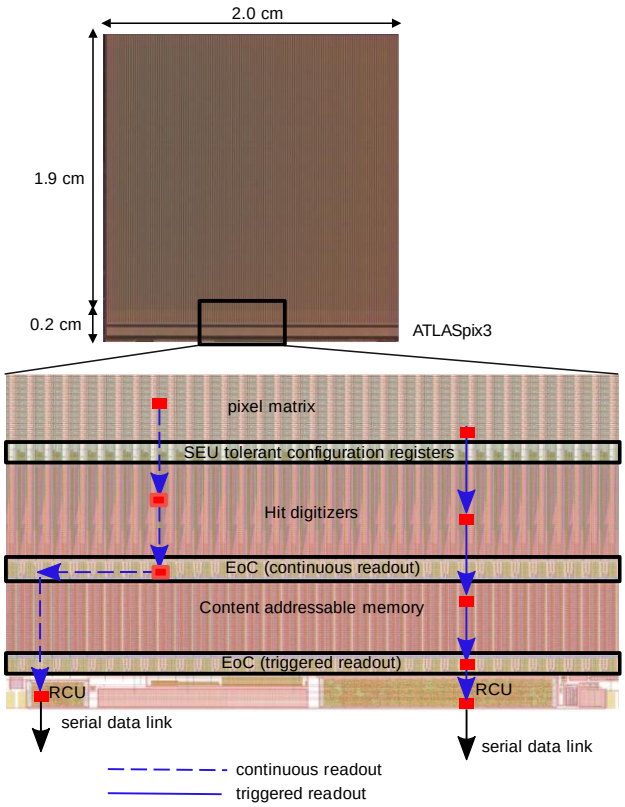

Figure 6: Digital readout circuits

Themes for student works

We are developing HVCMOS pixel sensors with the goals to improve their spatial-, time- and energy resolution, to improve rate capability, to design cost effective sensors. We would like to develop a versatile tool for scientific, medical and industrial applications as well for education.

For these tasks we need help, and we offer different master and bachelor theses and internships, that can be combined or done individually. You would learn to design and to test ASICs by working on innovative sensors within (international) scientific projects. If you chouse to focus on experimental work (tests and detector assembly), you would learn FPGA-, software- and PCB-design, chip packaging technology, have possibility to build detector-systems (with a sensor chip that is bonded to PCB, with FPGA as interface, USB controller chip, self-made software) and test them in our lab or at particle accelerators (test beams).

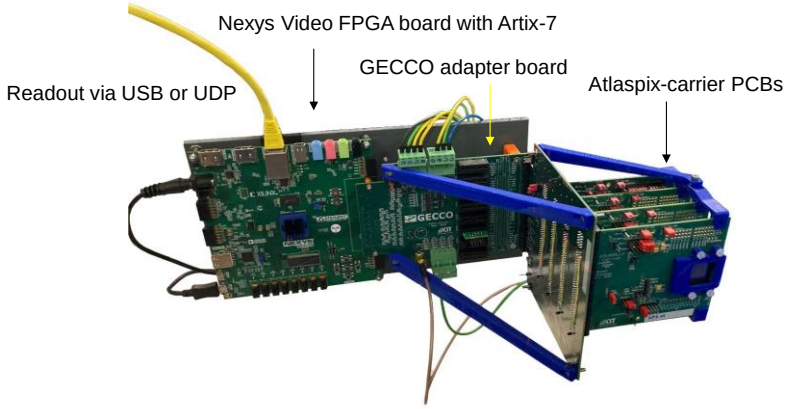

Figure 7: Beam telescope with Atlaspix sensor chips and GECCO modular readout system

Theme 1: Portable USB camera

One master/bachelor work theme could be development of potable sensor based on Atlaspix or Mupix. The system could be powered and readout via USB. Such a portable sensor could be used for education, simple imaging and spectral measurements with x-ray, radioactive sources or cosmic particle measurements. The system would be based on a commercial UCB controller chip, microcontroller and the Astropix/Mupix sensor chip. Further development of Atlaspix can be done within the thesis, such as reduction of pixel size, implementation of on-chip HV generator, digital block with an interface to USB controller.

Theme 2: Sensors with high time resolution

Time resolution in detection of photons and particles is important for many applications, two of them being medical imaging (PET) and high energy physics experiments. A high time resolution allows efficient coincidence detection of the photons/particles that originate from same event. In some cases, the position of the particle source can be calculated by the time-of-flight method.

Time resolution of an HVCMOS sensor can be improved by employing avalanche multiplication for amplification of sensor signal and by making the amplifier faster (improving its bandwidth). We are investigating both methods.

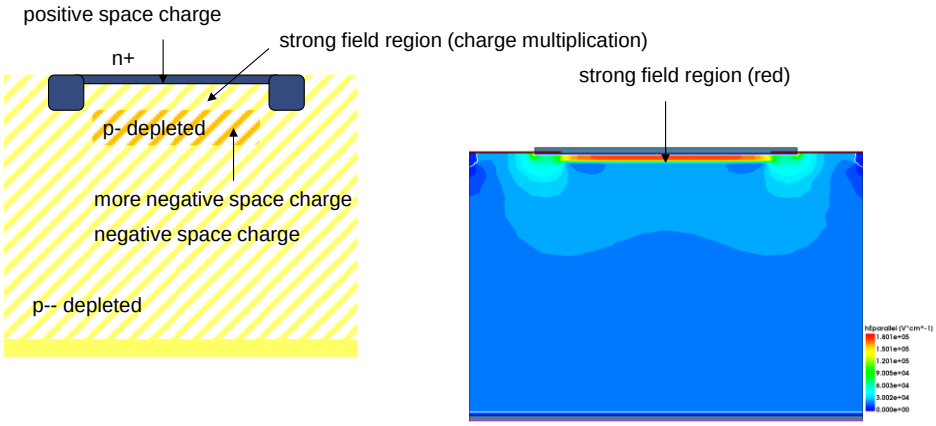

Figure 8: Avalanche sensor diode, structure and simulation

Design of sensor diode with avalanche multiplications requires knowledge about sensor structure, simulations of the electric field (TCAD simulations) in the case of certain doping densities, process modifications, design of prototypes and tests.

Standard amplifier for the particle sensor signal is a charge sensitive amplifier. It is a system with feedback and it requires an active circuit (voltage amplifier) with much higher open loop gain than actual amplification when the feedback is closed. Our idea is to amplify the sensor signal directly with a cascade of open loop voltage amplifiers.

An amplifier without feedback can have simpler structure because no high gain is needed. By careful design and using multi-stage topology a higher bandwidth can be achieved. Further improvement can be achieved by using very fast SiGe bipolar transistors as input devices.

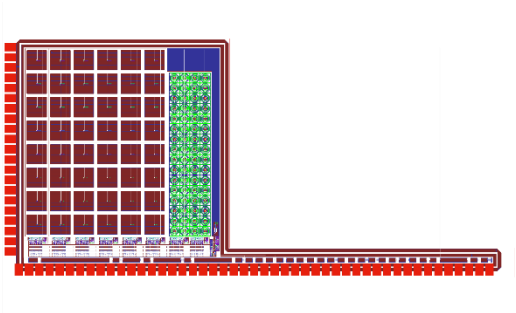

Figure 9: Sensor test chip in SiGe BiCMOS technology of IHP

The theme of the thesis would be to develop sensors with high time resolution (<100ps) based on sensors with avalanche multiplication or/and novel amplifiers. Existing test structures would be the starting point. As a fast sensor is useless without circuits for precise time measurement, one task would be development of time to digital converters with ~10ps time resolution.

Theme 3: Sensors with high rate capacility

High-rate capability means that sensor can process large amount of particle hits. Rate capability can be achieved with parallelism in data processing (smart pixel concept), fast multiplexers and fast data transmission. One theme of the thesis is the development of fast serial data links. A goal would be to design links with ~ 10Gbps data rate. We also investigate the use of wireless data transmission from sensor chip and have already designed one prototype. The theme of the thesis could be characterization of this prototype and its further development.

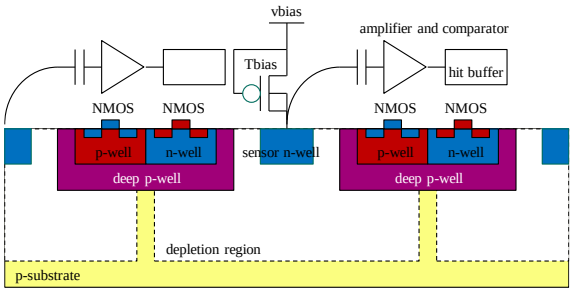

Figure 10: Pixel sensor with small electrode, cross section of two pixels

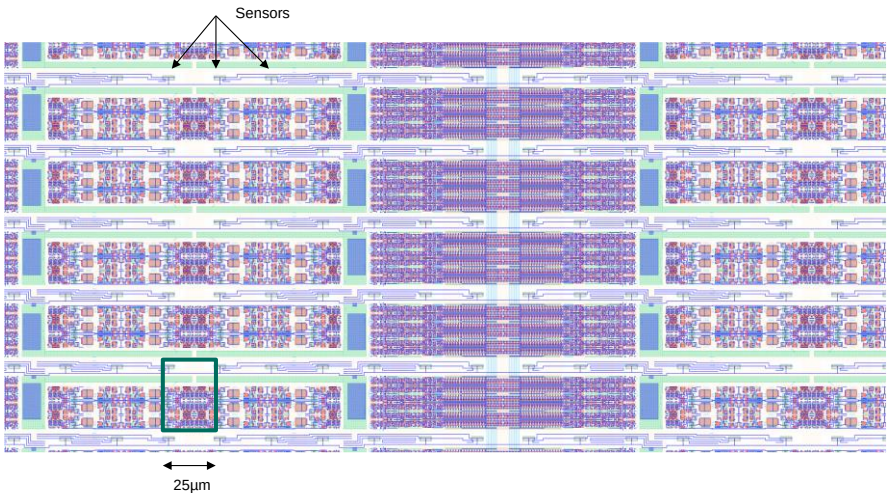

Figure 11: Pixel sensor with small electrode – layout of analogue and digital pixel electronics

Theme 4: Small pixels

Spatial resolution is one of the key parameters for imaging sensors. In the case of particle sensors, spatial resolution usually refers to the accuracy of the detection of the particle source or particle track direction. A small sensor with small pixel size can have a good spatial resolution as well as a large sensor with larger pixel size. Sometimes, the size of the detector is limited (example: digital camera) and for these smaller detectors, a high spatial resolution can be achieved by small pixel size. One possibility is implementation of HVCMOS sensors in technologies with smaller feature size, such as 55nm or 28nm. The theme of the thesis could be porting of existing designs into these nano meter scale technologies.

Another possibility to achieve smaller pixel size is so called small electrode design. By using of small collection electrode, more space can be used for readout electronics and the pixels can be smaller. High voltage can be applied to improve detection efficiency and signal collection speed. The thesis would start by revision of the existing prototype. Amplifier and sensor design would be improved to achieve smaller detector capacitance and noise of several electrons. The goal is to design a 1 cm x 1cm sensor.

Theme 4: Silicon gamma sensors with high quantum efficiency (fully depleted sensors)

Measurement of particle energy allows particle identification and improvement of image quality. All our HVCMOS sensor designs measure signal amplitude. However, this amplitude is not proportional to the full particle energy, it is just the measure of the particle's energy loss in the depleted sensor part.

Our goal is to implement an HV-CMOS sensor whose entire substrate is depleted. By stacking such fully depleted sensors, total energy of the particles can be measured. Another application would be detection of high energy photons, using silicon HV-CMOS sensors. The theme of the thesis would be simulation of the sensor structures, measurement of depletion layer depth on existing prototypes and design of next sensor iterations. One application is a proposed Compton telescope Amego-x, that we develop together with NASA. For this application, all circuits must be low power.

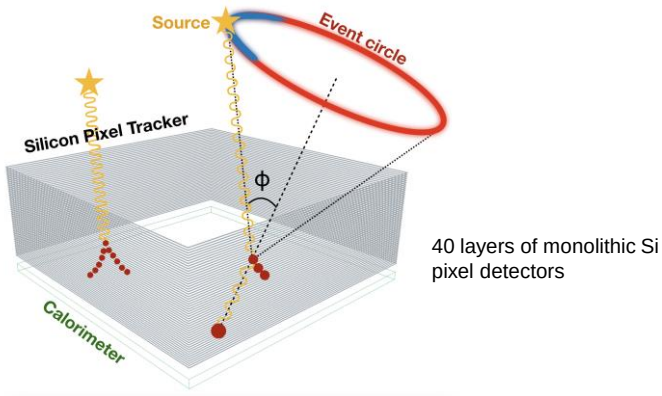

Figure 12: NASA Compton telescope

Related themes

Theme 5: Silicon photomultipliers

Silicon photomultiplier is a special type of silicon sensor where avalanche multiplication is employed to multiply the primary signal. Silicon photomultipliers work in Geiger mode with a bias voltage several volts higher than the breakdown voltage. In Geiger mode, the current generated during the avalanche continues to flow until a quench circuit lowers the bias voltage. A primary signal of only one electron hole pair (generated by e.g. visible photon) can be therefore detected. These devices can detect single photons like a PMT, which is why they are called Silicon photomultipliers. Design of sensor SiPMs requires simulations of the electric field (TCAD simulations) in the case of certain doping densities and possibly process modifications.

The thesis would start with measurements on existing prototype. Test system would be designed, that includes carrier PCB, firmware, software. Measurements with light sources would be performed.

Based on measurement results, the sensor design would be improved.

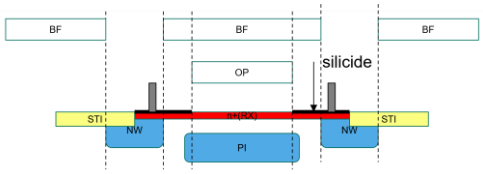

Figure 13: Silicon photomultiplier

Theme 6: ASICs at very low temperatures (cryogenic conditions)

Theme of this thesis would be measurements on integrated electronic devices – diodes, bipolar- and CMOS transistors, circuits at very low temperatures (down to 4K). You would investigate how the low temperatures influence effective doping, leakage currents, transistor static and dynamic characteristics, noise. One goal would be to perform measurements with an HVCMOS particle detector ASTROPIX. This sensor has very low power consumption and large area and is suitable for measurements in a cryostat. Particle sensors are affected by thermal and leakage current noise. since

the thermal noise and leakage currents decrease at low temperatures, one goal of the work would be to investigate whether very cold environment leads to a higher signal to noise ratio. The second part of the thesis could be design of circuits optimized for cryogenic temperature conditions. They could include low voltage and power digital circuits, low power ADCs.

Theme 7: Single event upset tolerance

Within this thesis you would investigate single event upsets in different memory cells. Single event upset occurs when particles (e.g. “cosmic muons”) generate charge in the vicinity of transistor drains which causes change in internal voltage and lead to loss of the stored bit. We have already designed several memory matrices in 28nm and 180nm technologies of different substrate types. Some cells use triple redundancy to increase SEU tolerance. SEU rate would be measured by irradiating the memory cells with a beam of high energy particles. Based on measurement results, design would be optimized.

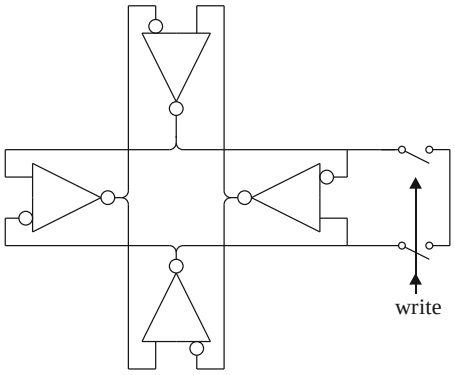

Figure 14: SEU tolerant memory cell (DICE design)

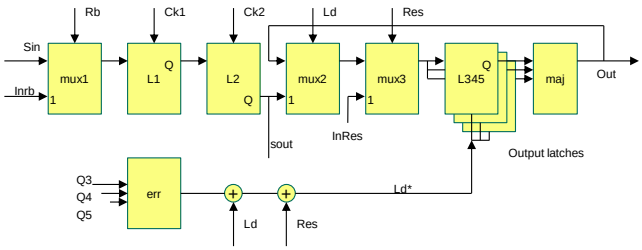

Figure 15: Triple redundant memory cell

Required skills:

Basic knowledge of ASIC design (e.g. obtained within courses DAS, DDS or PSCOC) is beneficial.

For some themes, knowledge of HDL and C++.

Duration: 6 months

Language: English or German

Location: Building 242 (IPE), Campus North

Contact: Ivan Peric (ivan.peric@kit edu)