High Voltage CMOS Active Pixel Sensor

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Abstract — The high voltage CMOS (HVCMOS) sensors are a novel type of CMOS active pixel sensors for ionizing particles that can be implemented in CMOS processes with deep n-well option. The pixel contains one sensor electrode formed with a deep n-well implanted in p-type substrate. CMOS pixel electronics, embedded in shallow wells, are placed inside the deep n-well. By biasing the substrate with a high negative voltage and by the use of a lowly doped substrate, a depleted region depth of at least 30 µm can be achieved. The electrons generated by a particle are collected by drift, which induces fast detectable signals. This publication presents a 4.2 cm^2 large HVCMOS pixel sensor implemented in a commercial 180 nm process on a lowly doped substrate and its characterization.

***Index Terms* — Radiation monitoring, Silicon radiation detectors, Ionizing radiation sensors, Radiation imaging, Particle beam measurements, Particle tracking, Position sensitive particle detector, Smart pixels, Active pixel sensors.**

I. Introduction

THE described active pixel sensor is designed for detection of ionizing particles and for measurement of their trajectories – particle tracking. The possible applications are experimental particle physics, medicine (particle therapy beam monitoring), gamma ray astrophysics (sensor for a Compton camera) and electron microscopy. The described sensor is based on a novel pixel structure which can be produced in a standard CMOS triple-well process. The readout electronics is embedded inside the pixel electrode (n-well implanted in p-substrate) used to collect the electrons generated by traversing particles. In this way, the electronics is isolated from substrate and the substrate can be biased with a high voltage which improves sensor properties such as signal amplitude, charge collection speed or radiation tolerance. We refer to such a pixel diode as the active or "smart" diode. With this name we emphasize that the cathode of the diode (n-well) contains active circuits and logic gates. The HVCMOS sensors, based on smart diodes, may be also suitable for other applications, such as construction of fully depleted back-side illuminated optical sensors or fast sensors for time of flight measurements.

A. Technical Requirements for Particle Tracking Sensors

Particle tracking can be performed by means of several layers of thin pixel sensors. Particles move through the layers and generate signals. In this way, 3-dimensional coordinates of the tracks are recorded in order to reconstruct the particle trajectories. The most important technical requirements for particle tracking sensors are: small amount of material in the detector layers, low power dissipation, high detection efficiency, radiation tolerance, good time resolution and uniformly sensitive large detector area.

The amount of material should be minimized since thick and dense structures cause particles to scatter and deteriorate particle tracking accuracy. For the same reason, cooling structures should have as little material as possible. This puts constraints to sensor chip thickness and its power dissipation. On the other hand, since charged particles penetrate sensor and ionize semiconductor along their tracks, the amount of generated electron-hole pairs is proportional to track length within the sensing-layer and thus roughly its thickness.

Particles of high energies damage the electronics and sensor by ionization (total ionizing dose damage TID) and by non-ionizing energy loss (NIEL) that leads to displacement of the silicon or dopant atoms [1]. The main damage mechanism in the case of TID is ionization in SiO_2 that is used to isolate transistors from each other (field oxide). The use of guard rings and circular gate geometry can mitigate these effects.

Displacement of Si-atoms leads to interstitials and vacancies and generates localized energy levels in the band gap that lead

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to several negative effects: a larger leakage current, more probable recombination and trapping and change of the dopant density and type. Since different particles have different NIEL, we use the unit n_{eq}/cm^2 to express the fluence of arbitrary particles that causes the same displacement damage as 1 MeV neutron/cm^2 in silicon. A sensor for particle tracking should be tolerant to the expected ionizing dose and displacement damage.

A depleted active sensor layer is desirable because the high electric field separates electrons from holes and makes them drift quickly towards the sensor electrodes. This improves time resolution and radiation tolerance. Since a larger depleted region leads to a larger signal, our goal was to increase the depleted layer depth as much as possible. This was achieved by the use of high reverse bias voltage and lowly doped substrate.

A high time resolution is desirable in order to be able to assign particle signals in different detector planes to a certain track by measuring time coincidence. A detector area with insensitive regions is in most cases not acceptable because it would lead to poor tracking efficiency. A pixel size in the order of 100 µm is for many applications sufficient. The sensor area of modern silicon tracking detectors can be ≈ 200 m^2 [2] [3].

Standard silicon-based technologies for particle tracking are strip- and hybrid pixel detectors [1] [4]. They use customized passive sensors which are arrays of diodes on a lowly doped substrate. Often, a double sided process is required since the substrate bias voltage is applied from the back side. In both cases, external readout chips are required. The sensor pixels of a hybrid pixel detector are connected to an external pixel-readout chip by bump bonds. A disadvantage of these detectors is the need for customized sensor technology. Further drawbacks are high cost and large amount of material in the case of hybrid pixel detectors and, in the case of strip sensors, the need for two sensor layers to achieve 2D resolution and measurement ambiguities when the particle flux is high. Two layers are required because the long and narrow sensor segments – strips – provide only one coordinate of the particle hit.

B. Development of CMOS and HVCMOS Sensors for particle tracking

The first monolithic active pixel sensors (MAPS) for particle tracking implemented in a commercial CMOS technology have been presented in [5]. The MAPS used an undepleted low resistivity epitaxial layer as sensing volume. Signal electrons move by diffusion and get collected by a small n-well. The pixel electronics is made only with NMOS transistors. The MAPS were sensitive to displacement damage and did not provide high time resolution because of slow charge collection and the used rolling shutter readout.

The HVCMOS sensor structure has been for the first time described in [6]. After more than 30 small size prototypes produced in several CMOS processes ranging from 65 nm CMOS to 350 nm HVCMOS (with pixel sizes down to 2.5 µm) [7] [8] [9] [10], the first monolithic HVCMOS sensor with a full reticle size matrix *ATLASpix3* has been designed. ATLASpix3 contains several novel circuits which are explained in this publication. The main project goal is to demonstrate that it is possible to construct a large detector layer for the new ATLAS Inner Tracker [2] with the HVCMOS sensors.

We would like to mention several published results that are relevant for ATLASpix3:

1) Measurements of radiation tolerance of HVCMOS smart diode detectors with similar structure as ATLASpix3 have been presented in [11] [12].

2) Measurements of depleted layer thickness and charge signal with passive test diodes and the influence of displacement damage caused by protons and neutrons have been presented in [13] [14] [15]. The test diodes were implemented on different substrates in the resistivity range 20 – 1000 Ωcm, some of them on the same 200 Ωcm substrate as ATLASpix3. It was observed that radiation causes both removal of existing acceptors and introduction of new acceptor states, which has the effect that after fluence ~ 10^{15} n_{eq}/cm^2 all investigated substrates behave similarly. The 200 Ωcm substrate showed smallest changes in terms of resistivity and signal amplitude as function of NIEL.

3) Reference [16] presents radiation induced leakage current measurements.

4) Depletion depth of 166 µm and a full depletion of the substrate has been achieved with an HVCMOS sensor described in [17].

The experience gained with these developments has been used to design ATLASpix3.

Also, the MAPS structure has been developed in past decade. Based on the structure from [5], a series of MIMOSA sensors have been designed such as MIMOSA26 and ULTIMATE [18] [19]. Signal to noise ratio and radiation tolerance has been improved by use of high resistivity depleted epitaxial layer [20].

A deep p-well was introduced (quadruple well process) in Isolated N-wells MAPS (INMAPS) [21] which allowed for the use of PMOS transistors in pixels and implementation of complex pixel electronics able to distinguish particle signals from noise. A sensor based on this structure ALPIDE has been developed for the tracking detector of ALICE experiment [22]. ALPIDE uses high resistivity epitaxial layers (e.g. thickness 25 µm, resistivity 8 kΩcm), which are partially depleted by applying moderate substrate bias. Radiation tolerance was further improved by process modifications [23] which allowed for full depletion of the epitaxial layer. Radiation hardened MAPS were proposed for application in ATLAS experiment [24].

Another particle pixel sensor structure with depleted sensing volume that is based on commercial CMOS process is SOI sensor [25] [26].

A CMOS sensor with fully depleted substrate has been presented in [27].

This paper is organized in 6 sections. Section II describes the overall ATLASpix3 chip architecture. Section III describes the pixel structure, its components such as charge sensitive amplifier and comparator. Section IV describes the digital circuits of the chip. Section V presents experimental results and VI summarizes the presented material.

C. Technical Requirements for ATLASpix3

A detector for particle tracking should be thin, it should have certain spatial and time resolution and it should stay within specifications during the operating time, i.e. after exposure to a certain radiation dose and fluence. Required time resolution is application dependent. For ATLAS, it is 25 ns [2]. This requirement originates from the working principle of the Large Hadron Collider. The particle bunches collide every 25 ns. The duration of one bunch collision is < 1 ns. It is required that a sensor precisely assigns a hit to its particle bunch collision in order to ease the track reconstruction.

The front-end electronics of ATLASpix3 is based on a charge sensitive amplifier and a comparator. The comparator provides a detection threshold. A small threshold improves detection efficiency and time resolution. The threshold is limited by noise since too low thresholds lead to a high noise hit rate. The minimum threshold also depends on the pixel to pixel threshold mismatch (dispersion). If the threshold distribution is wider, the threshold voltage, which is common for all pixels, must be set larger in order to assure that all pixels have their local thresholds above the temporal noise floor. Threshold dispersion can be reduced by use of DACs (threshold tuning) as will be discussed later.

Time resolution is limited by time walk caused by the variation of the signal. Because of time constants of the amplifier and comparator, signals with larger amplitudes cause faster response. Signals that are just above threshold lead to excessive delay. A certain ratio between minimum signal and threshold is required to keep time walk below required limit. This ratio can be estimated by simulations. For the amplifier in ATLASpix3, it is 2.06. This leads to the requirement:

$S > 2.06\ Th$

This requirement should hold for nearly all (e. g. 99%) signals and pixels. The following table summarizes the most important requirements for ATLASpix3:

TABLE I

Chip area/thickness	2 cm × 2 cm / 250 µm
Pixel size	50 µm × 150 µm
Detection efficiency	99% in 25 ns time window
Noise rate per pixel	5 Hz – 40 Hz/pixel
Power consumption	<500 mW/cm^2 (preferably 150 mW/cm^2)
Current consumption	<240 mA/cm^2
Radiation doses	800 kGy TID & 1.5 10^{15} n_{eq}/cm^2 NIEL
Operating temperature	- 25 °C (maximum ratings - 55 °C to +60 °C)
Signal, Noise and threshold	S > 2.06 Th for 99% of signals and pixels

ATLASpix3 specifications.

II. Chip Architecture

ATLASpix3 pixel detector is a system-on-chip which contains 132 × 372 pixels of 150 µm × 50 µm size. The chip area is 20.2 mm × 21 mm. The chip is implemented in a 180 nm HVCMOS technology. To enhance signal amplitude, p-type Czochralski substrate with resistivity in the range 200 - 400 Ωcm has been used instead of the standard wafer. The only high voltage device used is the high voltage deep n-well designed to have a breakdown voltage of about 65 V with respect to the substrate potential. The used technology offers 7 metal layers. The top metal layer is thick and it was used for distribution of power and time critical signals.

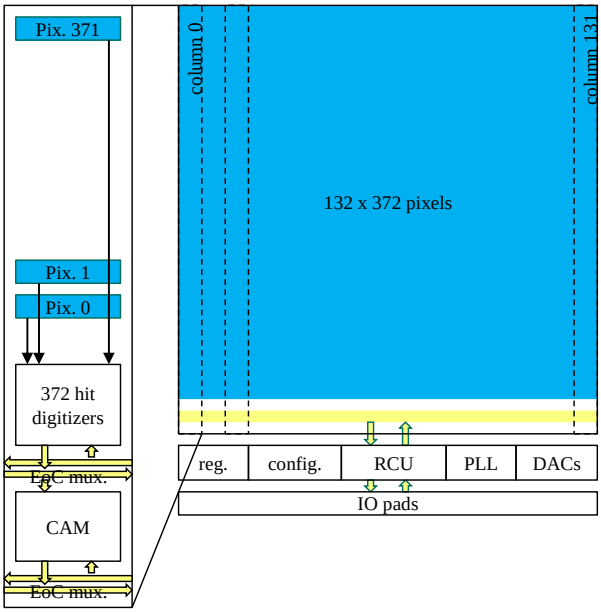

Fig. 1 Block diagram of ATLASpix3 chip.

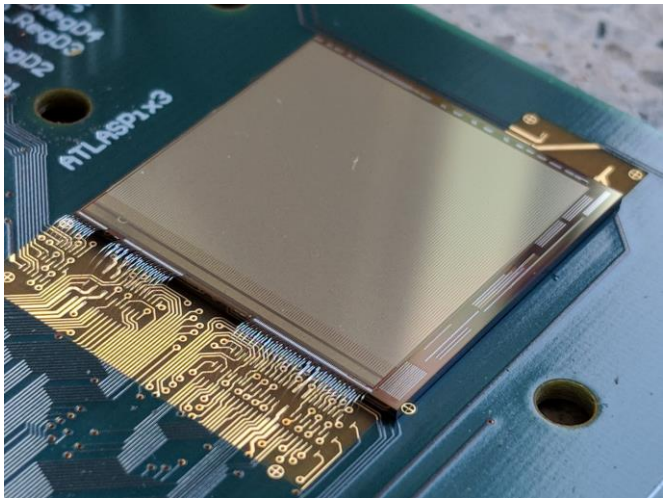

Fig. 2 Photograph of ATLASpix3. The chip area is 20.2 mm × 21 mm.

The main chip part is organized in 132 columns. One column consists of 372 pixels, 372 hit digitizers (HD) with attached 80 content addressable memory cells (CAM) and two end-of-column multiplexers (EoC mux), as shown in Fig. 1. The chip periphery also contains the readout control unit (RCU), the clock generator based on phase locked loop, configuration registers, DACs, linear regulators and IO pads. There is an on-chip shunt and low dropout linear regulator that can be used to generate 1.8 V power supply voltage from a current and in this way allow for serial powering scheme [28]. The pixel matrix extends to three die borders making the chip three-side buttable. The distances from the sensor diodes (deep n-well) to the chip edges are 96 µm (top), 184 µm (left) and 147 µm (right).

The pixels comprise analog circuits such as a charge sensitive amplifier followed by a comparator. They detect particles traversing the sensor – *particle hits*. Particle hit digitizers include digital circuits that receive the output signal of the pixel

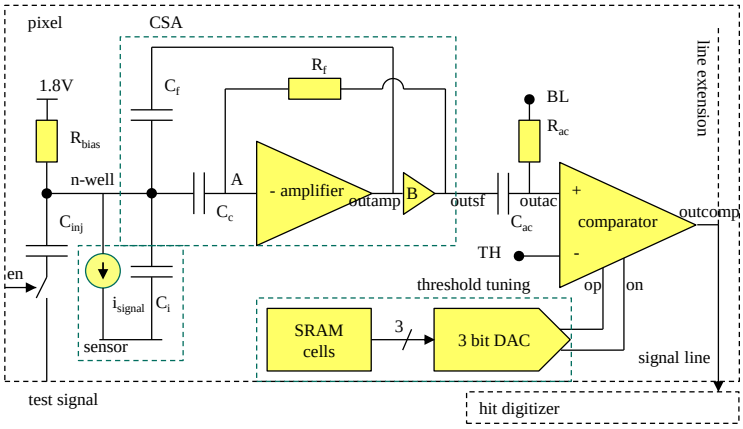

Fig. 3 Block diagram of the pixel. The main parts are the sensor diode, the AC-coupled charge sensitive amplifier (CSA) and the comparator. Voltages BL and TH are generated at the chip periphery.

comparator and generate time-, amplitude-, and spatial information of the particle hit. The hit digitizers are spatially separated from the pixels and placed at the bottom edge of the chip. The layout of the hit digitizer was done full custom and optimized to be small (75 µm × 4 µm). The periphery of the chip occupies a tenth of the area occupied by the pixels.

The approach of separating the digital parts (hit digitizers, CAM) from the analog pixel electronics has several advantages: the noise caused by digital activity is confined to the chip periphery where the digital parts are placed. The power consumption caused by clocked digital lines is smaller as no digital signals are distributed over the entire chip area. Pixel electronics is reduced to the minimum, which leads to smaller capacitance of the sensor electrode. Implementing of digital CMOS gates in pixels which are permanently clocked would lead to a crosstalk to the sensor electrodes. There are, however, a few disadvantages of this approach. A large number of lines is needed to connect the pixels to their hit digitizers. There are in our case, 49104 traces each with a length of 1.8 cm and a pitch of 0.8 µm (line spacing 0.52 µm) on the chip.

Fig. 2 shows photograph of ATLASpix3 chip.

III. Pixel

The drawing of the pixel cross section is shown in Fig. 4.

The pixel electronics are embedded in shallow n- and p-wells. A deep n-well is used to isolate the shallow wells from the p-type substrate. The deep n-well also serves as the sensor electrode that collects electrons generated by ionization. The substrate around the deep n-well is depleted by applying a high negative voltage of about - 50 V at the p-doped substrate contacts that are located at the periphery of the chip. The deep n-well is biased employing a circuit that acts as a resistance R_{bias} connected between the positive power supply rail (1.8 V) and the n-well. The DC potential of the deep n-well is close to 1.8 V. For fast signals, the n-well behaves as a capacitance C_i. The main contributions to C_i are the deep n-well capacitance to the metal structures (simulated 120 fF), the n-well/p-well and the n-well/p-substrate junction capacitances (90 fF and 20 fF) and the capacitances between the n-well and PMOS transistor electrodes. Simulated total C_i value is approximately 250 fF. The size of the deep n-well is 121 µm × 21 µm. There is a guard ring formed with p-well, p-diffusion and metal 1 between the deep n-wells of neighboring pixels.

The block diagram of the pixel is shown in Fig. 3. The main parts are the sensor diode, the AC-coupled charge sensitive amplifier (CSA) and the comparator. The negative signal charge, which is collected by the n-well, is amplified by the CSA. The comparator compares the positive amplifier output signal to a threshold. The comparator output signals are

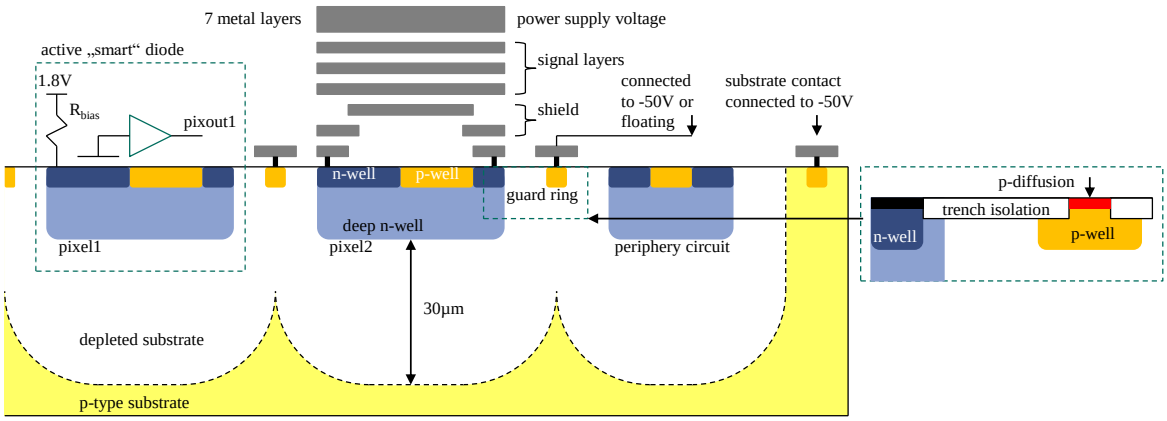

Fig. 4 Cross sectional view shows two pixels and chip periphery. The pixel electronics are embedded in n- and p-wells. A deep n-well is used to isolate the shallow wells from the p-type substrate and serves as the sensor electrode.

transmitted to the hit digitizers using long signal lines. These lines are implemented using three metal layers (metal 4 to 6) as shown in Fig. 4. Line extensions assure that all lines have nearly the same length (1.8 cm) and thus similar capacitance, independent of pixel position in the column. In this way, we equalize the rise times of the output signals. Two metal layers are available to shield the deep n-wells from the comparator signals. There is a circuit for threshold tuning (offset compensation) connected to the comparator. This circuit consists of a 3-bit differential current-steering DAC and SRAM cells to store the DAC value. A test signal circuit allows injection of a defined charge into the n-well by discharging metal-metal capacitor C_{inj}. This makes electrical tests without ionizing particle sources possible. The test signal is produced at the chip periphery, its amplitude can be varied by an on-chip DAC with 8 bits. The test signal is distributed to all pixels. It is possible to enable and disable the injection to each pixel individually.

Simulated signals outac from Fig. 3 for the input signals of 2100 e^-, 3500 e^- and 7000 e^- and the corresponding comparator responses are shown in Fig. 5.

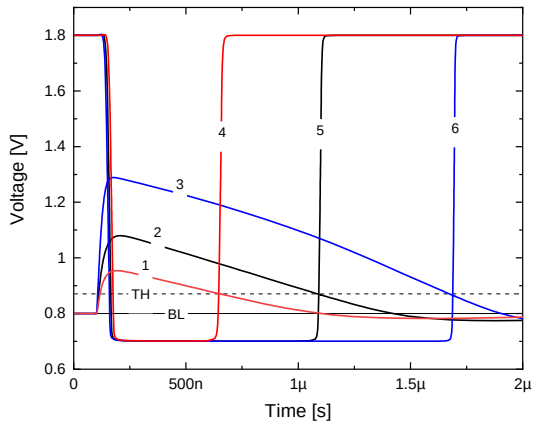

Fig. 5 Simulated waveforms. Waveforms 1, 2 and 3 are the amplifier responses (signals outac from Fig. 3) for input signal charge of 2100 e^-, 3500 e^- and 7000 e^- respectively. Waveforms 4, 5 and 6 are the corresponding comparator output signals (outcomp).

A. Charge Sensitive Amplifier

The schematic of the charge sensitive amplifier (CSA) is shown in Fig. 6. The CSA uses a folded cascode amplifier as active part. Since the gate of transistor T_{in} (node A) has a different DC potential than the n-well, AC coupling C_c is used. C_c has been implemented as a PMOS transistor.

There is a capacitive coupling of every p-diffusion to the deep n-well due to their parasitic junction capacitances. In standard CMOS circuits with the n-well at a fixed potential, these capacitances would only introduce capacitive loads. In our case, the n-well is the input node of the amplifier and the parasitic capacitances cause feedback. The junction capacitance between the drain of T_{load} and the n-well (C_{dload}) is important since T_{load} drain (amplifier output) experiences large voltage variations. C_{dload} is used as the capacitive feedback of CSA. We sum C_{dload} and the parasitic capacitance of line outamp to n-well into the equivalent feedback capacitance C_f. The CSA includes also a resistive feedback circuit R_f which will be explained in the next section. R_f is driven by an NMOS based source follower B. C_o is the capacitance of the output node (outamp). Deep n-well is modelled with its capacitance C_i and the signal current source i_{signal}.

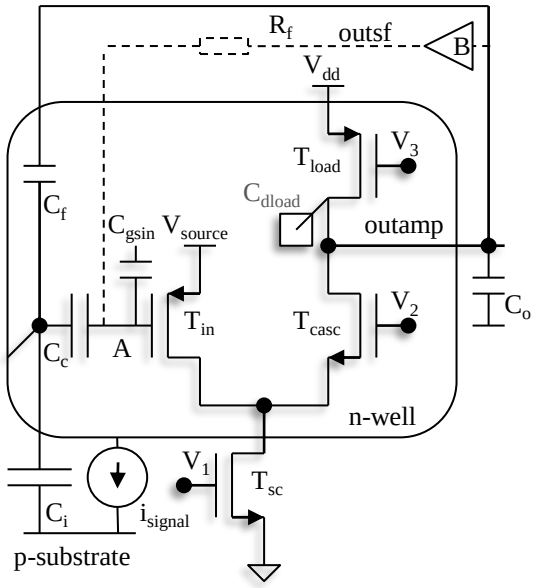

Fig. 6 Schematic of the charge sensitive amplifier. Voltages V_1, V_2 and V_3 are generated at the chip periphery. V_{dd} = 1.8 V and V_{source} = 1.2 V are power supply voltages. On-chip regulator can be used to generate V_{source}.

If we consider only the short time scale, where the current through R_f can be neglected, C_c influences CSA solely through the reduction of the open loop gain. It is caused by the voltage divider consisting of C_c and C_{gs} of T_{in} (C_{gsin}). If C_c is sufficiently large, the maximum output signal voltage is $V_{max} \approx - Q/C_f$. Q is the negative input signal charge.

The charge sensitive amplifier is affected by thermal and 1/f noise of its transistors and by shot noise of the sensor leakage current I_{leak} [29]. In the case of the not irradiated chip I_{leak} is small (~10 pA) and it does not contribute significantly to overall noise. In this case, the main noise source is the input transistor with its thermal noise. The contribution of T_{in} to total noise simulated with the analog simulator is about 50%, followed by the noise contribution of T_{sc} with 25%. Contributions of other devices are significantly smaller.

After life time fluence, we expect I_{leak} to increase to ~10 nA at room temperature or ~1 nA at operational temperature of - 25 °C [16].

B. Resistive Feedback Circuit

After signal amplification, the capacitances of the CSA should be discharged (reset) to the original voltages, otherwise consecutive particle signals would cause the amplifier to saturate. This is achieved with device T_{fb1} acting as a resistive feedback with equivalent resistance R_f, as shown in Fig. 7. The gate voltage for T_{fb1} (V_{gfb}) is generated in each pixel locally by the diode connected transistor T_{fb2} that is biased with current I_{fb2}. A similar bias circuit was used in [30]. Current I_{fb2} is small (60 pA) and T_{fb1} and T_{fb2} operate in weak inversion. $C_{filterfb}$ keeps V_{gfb} at a constant level. T_{fb1} behaves as a nearly linear

resistance $R_f = U_T/I_{fb2}$ for signal amplitudes at the amplifier output smaller than the thermal voltage ($U_T = kT/e \approx 25$ mV). For larger amplitudes, the current of T_{fb1} saturates at the value I_{fb2}. Capacitances are discharged with a nearly constant current until the voltage across T_{fb1} decreases to U_T. Afterwards, the discharge follows an exponential decay. To avoid signal loss, the discharge time should be sufficiently longer than the rise time of the amplifier (1). The formula for the discharge time will be derived in the next section.

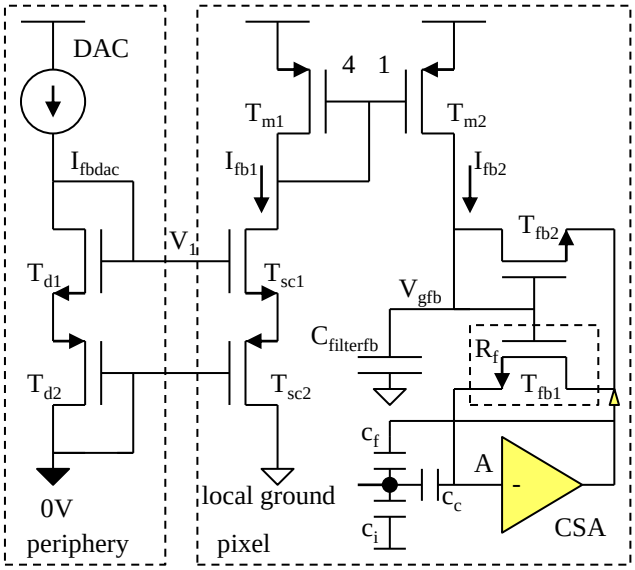

Fig. 7 Implementation of the resistive feedback circuit with bias network.

C. Time Constants of the Output Signal

The difference between the AC-coupled CSA and the standard CSA is the usage of C_c. If C_c is short circuited the AC-coupled CSA takes the form of the standard one. The standard CSA has an impulse response described with the exponential function with two time constants: rise time T_r and discharge time T_f, [29]:

$$T_r \approx \frac{C_{o,s}\, C_{i,s}}{C_{f,s}\, g_m};\ T_f = R_f\, C_{f,s}; \quad (1)$$

g_m is the transconductance of T_{in} and subscript s denotes the capacitances of the standard CSA. In order to estimate time constants of the AC-coupled CSA, we can analyze its simplified schematics for the case $I_{signal} = 0$. By using the formulas for Y to Δ conversion, we can rearrange the capacitances in the way that the AC-coupled CSA (for $I_{signal} = 0$) takes the form of the standard CSA as shown in Fig. 8. It holds:

$$C_{i,s} = \frac{C_i C_c}{C_{sum}};\ C_{f,s} = \frac{C_f C_c}{C_{sum}};\ C_{o,s} = \frac{C_f C_i}{C_{sum}};\ C_{sum} = C_i + C_f + C_c \quad (2)$$

By substituting (2) in (1), we obtain the time constants for the AC-coupled CSA:

$$T_r \approx \frac{C_o\, C_i}{C_f\, g_m};\ T_f = R_f \frac{C_f C_c}{C_i + C_f + C_c} \quad (3)$$

We assumed $C_c >> C_{gsin}$ and $C_o >> C_{o,s}$.

According to (3) the rise time is equal as in the case of the standard CSA. The discharge time is smaller if $C_c < C_i$.

As mentioned in the previous section, R_f has been implemented using transistor T_{fb1}. For signals across T_{fb1} with amplitudes larger than U_T, $C_{f,s}$ is discharged with the constant current.

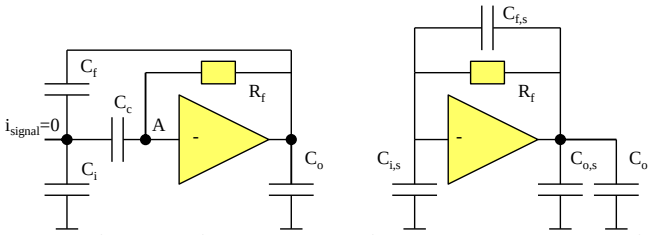

Fig. 8 Transformation of the capacitances of the AC-coupled CSA using of Y to Δ conversion. The case $I_{signal} = 0$ is considered. Left: original circuit. Right: transformed circuit.

Table II summarizes the simulated amplifier parameter values. N_i is the input referred r. m. s. value of temporal noise determined as the noise at the input of the comparator (line outac from Fig. 3) divided by the corresponding gain.

TABLE II

I_{bias}	C_i	T_r	C_f	g_m	C_c	T_f	N_i
2.6 µA	250 fF	22 ns	1.6 fF	59µS	600 fF	0.63 µs	79 e^-

Simulated values of the amplifier parameters.

D. Small Current Sources

The current I_{fb} is generated by means of a series of NMOS T_{sc1} and PMOS T_{sc2}, as can be seen in Fig. 7. The bias voltage V_1 is generated at the chip periphery by a current steering DAC I_{fbdac} and distributed over the pixel matrix. The use of PMOS transistor T_{c2} which operates in saturation, assures that the replicated bias current I_{fb} is independent of the local ground potential, since the ground line is connected to the *drain* of T_{c2}. If we used a single NMOS transistor to generate I_{fb}, a small voltage drop at its source would affect the current significantly. In our case, the voltage drops in the ground- and power rails can be in the order of 50 mV.

Radiation induced damage, particularly total ionizing dose effects may influence the current source and the pixel electronics. To make the pixel electronics more robust, we have implemented all NMOS transistors that operate in subthreshold region with annular gates. The channel region of such transistors is not adjacent to the field oxide where positive space charge is generated by radiation. Radiation tolerance of transistors with annular gate have been investigated in [31].

The simulated I_{fb1} current change caused by local ground variation of 50 mV is about 1%.

We have simulated the influence of the additional PMOS transistor in the current source to the mismatch of currents. Simulated precision of the current source, defined as sigma over mean value of the Monte-Carlo-sampled I_{fb1} values for a constant voltage V_1, is 8.95%. As comparison, a standard NMOS-based current source would have precision of 7.50%.

Simulated I_{fb2} for $V_1 = 0$ is about 5.3 pA (I_{fb1} = 6.7 pA) when cascaded current source is used. For the standard NMOS-based current source, we simulate I_{fb2} = 27 pA (I_{fb1} = 86 pA) for $V_{GS} = 0$.

E. N-well Bias Circuit

Since the CSA is connected to the n-well only capacitively, it cannot define its DC potential. The purpose of the bias circuit is to hold the DC potential of the n-well in the pixel at nearly

1.8 V. The dynamic resistance of the bias circuit r_{bias} should be high enough that the time constant caused by it is larger than the maximum discharge time of the amplifier. This leads to $r_{bias} > 10$ MΩ. The difficulty is that the sensor leakage current I_{leak} may increase to values ≈ 10 nA after radiation damage. Simpler circuits like a diode connected transistor would have a dynamic resistance ≈ U_T/I_{leak} which is lower than required. A polysilicon resistor would be too large in layout. The schematic of the bias circuit we used is shown in Fig. 9. R_{bias} can be decomposed to the contributions of T_1 and T_2:

$$r_{bias} = r_1 \,||\, r_2 = r_{ds1} \,||\, \frac{1}{g_{m2}} \quad (4)$$

with r_{ds1} being the drain source resistance of T_1 and g_{m2} the trans-conductance of T_2. || is the symbol for parallel connection. Since T_1 is in saturation, r_{ds1} is large. Since T_2 is biased with a small current I_{bias} of typically 10 pA, $1/g_{m2}$ and r_{bias} are large as well. The sensor leakage current flows through T_1 and does not influence r_{ds1} significantly. Since T_2 conducts a current independent of sensor leakage, which leads to a constant g_m, r_{bias} remains nearly independent of leakage current. The current source I_{bias} is implemented in the same way as I_{fb} source in Fig. 7.

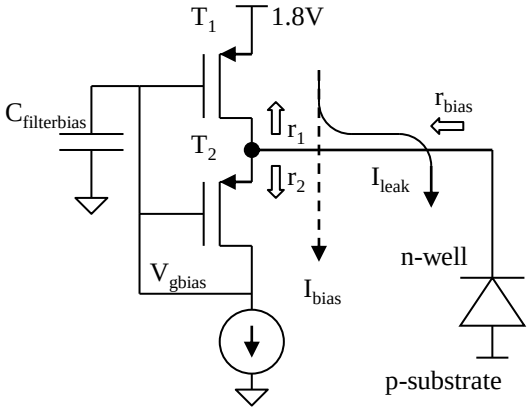

Fig. 9 Bias circuit. $C_{filterbias}$ keeps V_{gbias} at a constant level.

F. Comparator

The amplifier output and the non-inverting comparator input are AC coupled with C_{ac}, as shown in Fig. 3. The DC voltage at the comparator input is defined by the resistance R_{ac} connected to a voltage BL. The inverting comparator input is connected to a threshold voltage TH. The purpose of the AC coupling is to eliminate influence of voltage drops, temperature and low frequency noise. Analog signals at the positive comparator input above the value TH - BL cause signals at the comparator output and are recorded as particle events in the digital periphery. The leading edge of the comparator output signal contains the time information regarding the particle hit. Due to saturation of the feedback current, the signal length is nearly linearly proportional to the pulse amplitude for signal amplitudes larger than one thermal voltage.

To avoid crosstalk to the n-well, the comparator uses only NMOS transistors since they are isolated from the deep n-well by its p-well. The schematic of the comparator is shown in Fig. 10. It is based on two differential stages with the diode connected NMOS transistors T_{load1} and T_{load2} as active load. The gain of one stage is defined by the g_m ratio of the load- and input transistors (T_{in}). Two stages are used to provide sufficient gain. There is a driver transistor T_d attached to the comparator that generates a negative signal on the signal line outcomp when a particle signal is detected. A pull-up transistor T_{pullup} is placed in the hit digitizer. The source voltage for the driver transistor V_{driver} is generated by an on-chip linear regulator. The gates of the load transistors are connected to a bias voltage V_{gate} that is about 300 mV larger than the main power supply voltage of 1.8 V, in order to increase the high output level at node o_p and assure low on-resistance of T_d. V_{gate} must be provided externally. The comparator DC-gain defined as V_{op2} / V_{inp1} was simulated to be 17. The gain of the full circuit that includes T_d and T_{pullup} is $V_{outcomp}/V_{inp1}$ ≈ -590.

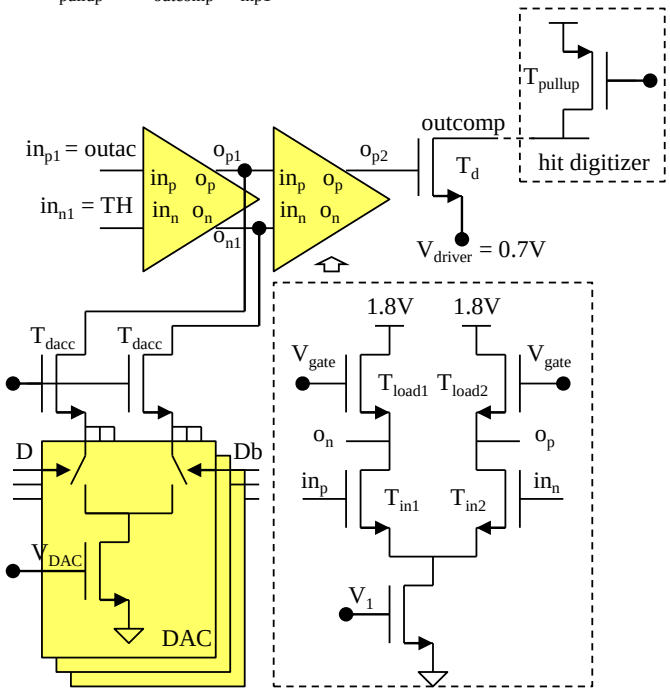

Fig. 10 Comparator with 3-bit DAC. Voltages V_1, V_{driver}, V_{gate} and V_{DAC} are generated at the chip periphery. Digital inputs of the DAC D and Db are stored in SRAM cells placed in the pixel. Transistors T_{dacc} are introduced to reduce the capacitive load of nodes o_{p1} and o_{n1}.

AC-coupling between CSA and comparator prevents that base line variations at the amplifier output influence threshold. According to Monte-Carlo simulations, the comparator offset causes threshold voltage mismatch of r. m. s. 4.3 mV. The simulated CSA gain variation is r. m. s. 2.9%. These variations contribute to the measured input referred threshold mismatch.

The outputs of the 3-bit differential current steering DAC are connected to o_n and o_p outputs of the first stage as shown in Fig. 10. Non equal DAC output currents introduce a programmable voltage offset. By adding a programmable offset we act against threshold variations. The tune-DAC current step can be adjusted using a 6-bit bias-DAC placed at the chip periphery that generates voltage V_{DAC}. Simulated programmable offset range for the settings we used in the measurements is up to ~115 mV.

In order to verify the timing requirement from Table I, we have simulated the minimum ratio between signal and threshold that leads to a time walk below 15 ns when signal amplitude is

increased from S_{min} to 20 ke$^-$ (S_{max}). 15 ns has been chosen based on measurement results: The delay dispersion contributes with an additional 10 ns (6 sigma value) to the timing error that should be smaller than 25 ns. The simulated ratio is $S_{min}/Th_i \approx 2.06$, as shown in Fig. 11 ($Th_i$ is the minimum signal that causes comparator response, the input referred threshold). According to the simulation, the contributions of the comparator and the amplifier to time walk are nearly equal.

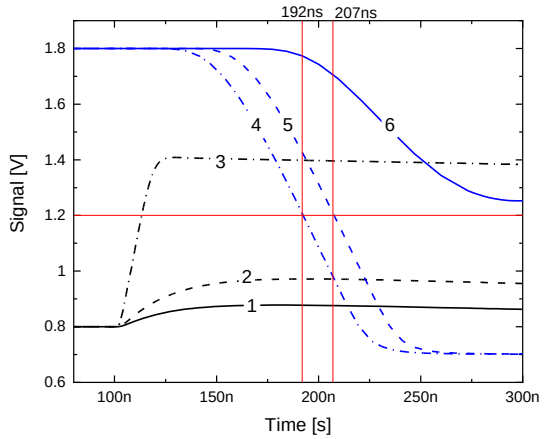

Fig. 11 Simulated time walk. Waveforms 1, 2 and 3 are the amplifier responses (signals outac) for input signal charge of Th_i = 1125 e$^-$, S_{min} = 2.312 e$^-$ and S_{max} = 20 ke$^-$ respectively. Waveforms 4, 5 and 6 are the corresponding comparator output signals (outcomp). Signal Th_i = 1125 e$^-$ is the minimum signal that causes comparator response, the input referred threshold. The time walk between outcomp signals for input signals of S_{min} = 2.312 e$^-$ and S_{max} = 20 ke is 15 ns. The ratio $S_{min}/Th_i \approx 2.06$.

IV. Digital Circuits

Digital circuits in ATLASpix3 perform several tasks, for instance, they digitize arrival time and amplitude of particle hits, they filter the hits using a trigger signal, format the data and transmit it off the chip. Hit time is measured with a digital 10-bit time stamp signal.

ATLASpix3 supports two readout modes – *continuous* and *triggered* readout as illustrated in Fig. 12. In the case of continuous readout, all data are transmitted. Triggered readout is useful for data reduction. Many particle experiments (among them ATLAS) use trigger signals to filter data. These signals are generated by dedicated detectors (calorimeters, muon detectors) and their data processing electronics when a signal signature of a particle interaction of interest is recognized. Since data processing takes time, the trigger signal can only be generated with a relatively long and fixed *trigger delay*. As mentioned, in LHC, the particle collisions occur during particle bunch crossings every 25 ns. Time stamp and trigger signals are synchronized with 25 ns clock that is in phase with the bunch crossing frequency. The trigger delay can be expressed as the number of clock periods and can be up to ~1000 clock cycles. The trigger is distributed to the tracking detectors. These detectors keep all particle hit data for the duration of the trigger delay. A hit will be transmitted only if the difference between hit- and trigger time stamp equals the trigger delay. This assures selective readout of the data from the bunch crossings with particle interactions of interest.

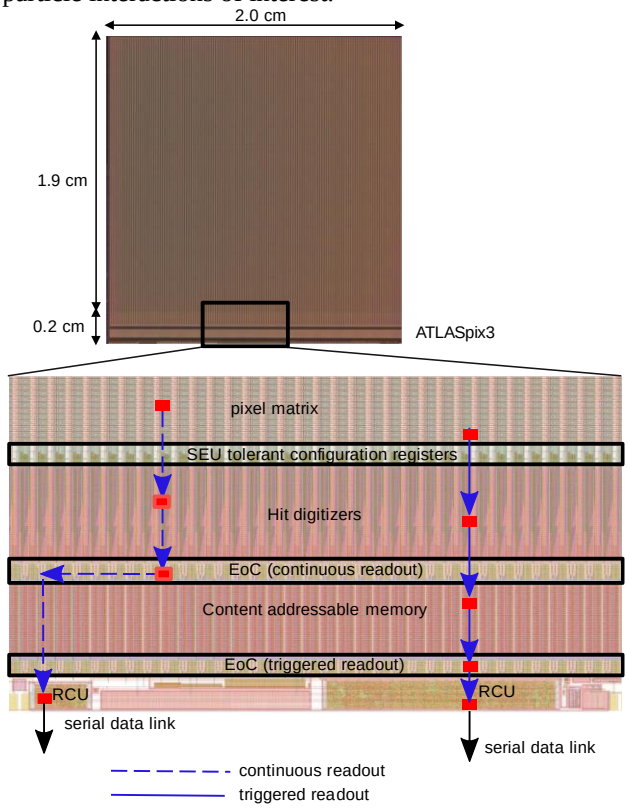

Fig. 12 Readout electronics in ATLASpix3 and signal flow in the case of continuous- and triggered readout.

As mentioned, the main chip part is organized in columns. One column consists of 372 pixels, 372 hit digitizers (HD), a pool of 80 content addressable memory cells (CAM) and two end-of-column multiplexers (EoC). The readout control unit (RCU) performs several tasks: it controls data readout, receives and performs commands including the trigger command. The RCU generates three time stamp signals: the main time stamp (TS), the delayed time stamp (TSdel) and the trigger time stamp (TTS).

TS is generated by a 10-bit counter with the nominal clock period of 25 ns. TS should be in phase with the bunch crossings. TS is used to measure the arrival time of the particle signal. When a signal is detected, the current TS-value is stored as a part of the hit data word. TSdel is equal to TS reduced by the Counter Delay Setting (CDS). CDS is programmable and it should be equal to the trigger delay expressed as the number of 25 ns clock periods. TTS is the stored value of TSdel in the moment when the trigger signal is received. It is used for addressing of the hit data words from the memory.

Fig. 13 shows the block diagram of the digital parts.

The hit digitizer is an asynchronous digital circuit, designed as full custom block. It comprises a hit flag (sr-latch), control logic, dynamic memory cells. The HD works as follows: The hit flag is set when a pixel comparator signal is received. At its leading and trailing edge TS value is stored. The pulse length can be reconstructed by using these time stamps. The data from the HDs are transferred to EoC1 (continuous readout) or to the CAM cells (triggered readout). The data word includes the stored time stamp values and the pixel address.

In the following, we will focus on the triggered readout. This readout mode has been used in the presented measurements. The CAM cell [32] comprises hit flags, control logic, memory cells and two digital comparators. One comparator compares the hit time stamp with TSdel. Another comparator compares the hit TS with TTS and allows content addressing. The CAM cell performs the following tasks: Data from the HDs are stored in the first empty cell. Output signal of the first comparator marks the clock cycle when the age of the hit equals CDS and therefore the trigger delay. If a trigger is received, the hit is selected for readout by setting a flag. Otherwise the CAM cell is emptied. After a while, the CAM block may contain data that originate from many triggers. The second comparator is used for readout of these data words in the order their triggers arrived.

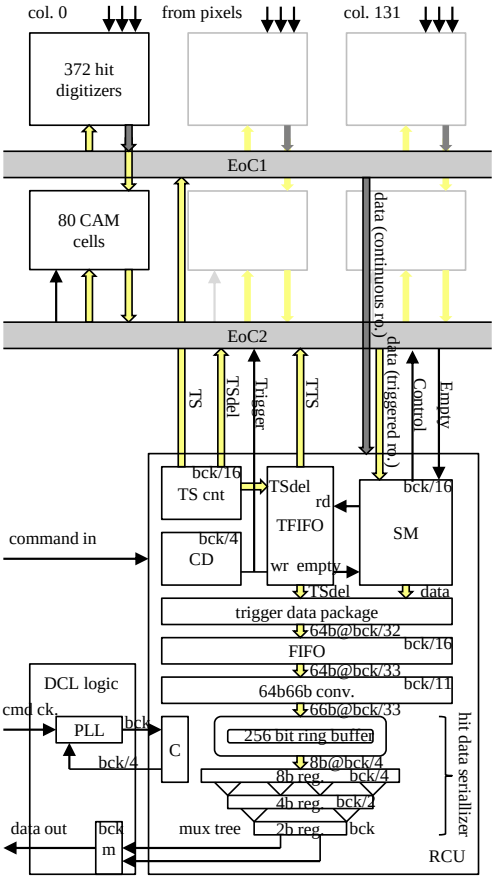

Fig. 13 Digital parts of ATLASpix3. Label *bck/n* indicates clock frequency of the corresponding block. Label mb@bck/n indicates that m bits are transferred at the frequency bck/n.

The RCU is the most complex digital part and it has been synthesized. The block diagram of the RCU is shown in Fig. 13.

Its function can be briefly described as follows: Upon receiving of the trigger command, the RCU stores TSdel-value into the trigger FIFO memory (TFIFO). This FIFO is necessary because sometimes a burst of triggers arrives which is processed with delay. The state machine of the RCU (SM) reads the entries from TFIFO and uses stored TSdel-numbers (referred to as TTS) for addressing of CAM cells that contain the data of these triggers. The data are read out via EoC2-multiplexer. The SM groups the data in the trigger data-packages. They are encoded according to the 64 bit to 66 bit conversion scheme described in [33]. The words are serialized by the block called *hit-data serializer* and sent off the chip at a rate of up to 1.28 Gbit/s. The RCU includes a command decoder (CD) as well. The CD receives commands made of 16-bit command-, address- or data-words at a rate of up to 160Mbit/s. Customized encoding described in [34] is used.

ATLASpix3 has a clock generator based on a ring oscillator and a phase locked loop (PLL). This full custom block is implemented with differential current-mode logic (DCL) gates. The clock generator receives an externally generated command clock and generates the fast bit clock (bck) used by the RCU, as shown in Fig. 13. The hit-data serializer operates in double data rate (DDR) mode. The last stages of the serializer use a binary tree structure made with 2→1 multiplexers (mux tree) and registers to perform 8→1 multiplexing. The last multiplexer (m) is placed outside the RCU and implemented with DCL gates. The RCU has several clock domains with the clock signals derived from bck by block C.

The chip contains several configuration registers. Every register cell contains a triple redundant data latch followed by majority logic. Triple redundancy makes the register tolerant to single bit flips that can be caused by ionization (single event upset). The cells have an *auto-refresh* feature. When a logic detects a single flip in 3 data latches, the majority output is reloaded into the latches. These registers store settings for the DACs that generate bias-, threshold-, base line- and injection-voltages. The registers are also used to control the injection and the pixel RAM.

V. Experimental results

A modular characterization setup has been developed. The setup can be configured for single chip tests or for particle tracking operation with up to four planes. It is based on chip carrier PCBs, main PCB, FPGA development board and PC. Lab measurements and measurements at high energy beam facilities were performed.

The main goal of the lab studies was to verify full functionality of the sensor. These measurements were performed by means of the test injection circuit based on C_{inj} shown in Fig. 3. Capacitance C_{inj} was estimated by using the parasitic capacitance extraction tool. It was additionally verified by measuring the output signal amplitudes when the sensor is irradiated with a ^{55}Fe radioactive source that generates X-ray photons with known energies and comparing them with the injection response.

An S-curve measurement is a simple way to investigate both signal and noise, even of a large pixel matrix for every individual pixel. To obtain an S-curve, test signals of variable amplitudes are injected into a pixel and the detection probability is determined. The starting value of injected charge is chosen to be significantly above the threshold resulting in a probability of one. The injected charge is then gradually reduced and the probability is measured for every step until it reaches zero. Plotting probability over injected charge results in the S-curve which can be fitted by a Gaussian Error Function. Triggered readout has been used. The trigger signal has been issued with

a fixed delay with respect to the injection. Two parameters can be extracted from an S-curve: Firstly, the input referred detection threshold is the point of an S-curve with 50% detection probability. It depends on the signal amplification (amplifier gain) and on the threshold value in the measured pixel. The second parameter is the transition width of the S-curve. It is a measure for the input referred noise. Measured S-curve is shown in Fig. 14.

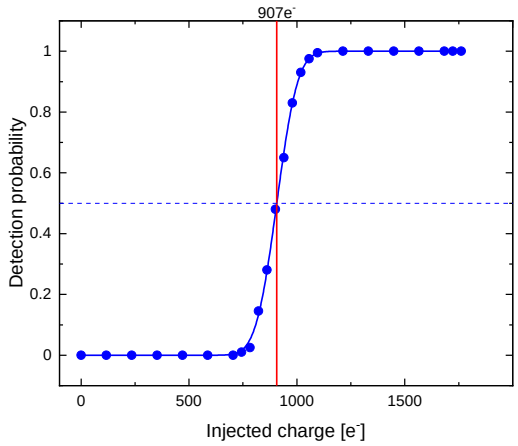

Fig. 14 Detection probability versus injected charge. The error function fit to data has mean value μ = 907 e⁻ and sigma value σ = 76.3 e⁻.

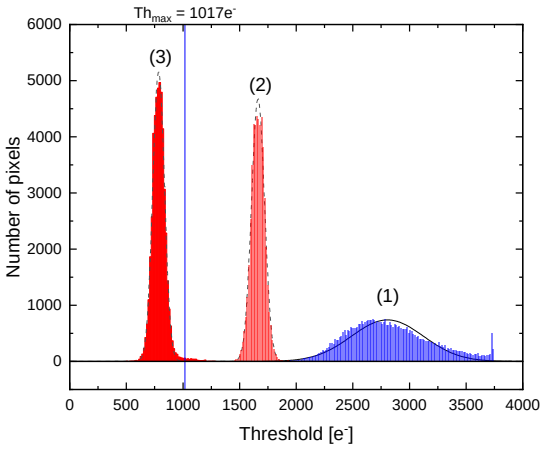

Fig. 15 Histograms of the threshold values for every pixel obtained from S-curve measurements with the test injection circuit. High voltage bias was - 50 V. Histogram 1 shows untuned threshold values (all tune DACs at maximum setting). Histograms 2 and 3 show tuned thresholds with high and low target mean values respectively. Gaussian fit to untuned thresholds has mean value μ = 2806 e⁻ and sigma value σ = 318 e⁻. Gaussian fits to tuned thresholds have μ = 1663 e⁻/ μ = 785 e⁻ and σ = 58 e⁻/ σ = 52 e⁻ for histograms 2/3 respectively.

Fig. 15 shows the histograms of the measured pixel thresholds. Transistor mismatch renders the distribution Gaussian. The mean value of the distribution of untuned thresholds (histogram 1) is 2806 e⁻ and the sigma value is 318 e⁻. For optimal operation with an acceptable noise rate the detection threshold should be set as small as possible. Consequently, a reduced threshold distribution width improves the detector performance because a lower threshold can be set. As already mentioned, ATLASpix3 has a compensation mechanism installed: the local comparator threshold can be adjusted by a value stored in RAM for every pixel individually. This process called tuning is used to reduce threshold distribution width. S-curves based on test signal injections are a convenient way to tune the pixel matrix. Fig. 15 shows the histograms of tuned thresholds. Histograms 2 and 3 show tuned thresholds with high and low target mean values respectively. Corresponding Gaussian fits have mean values μ = 1663 e⁻ / μ = 785 e⁻ and σ = 58 e⁻ / σ = 52 e⁻ for histograms 2 and 3 respectively.

The average noise value for all pixels in the matrix obtained by S-curve measurements is about 71 e⁻ r. m. s., which matches well with simulated 79 e⁻.

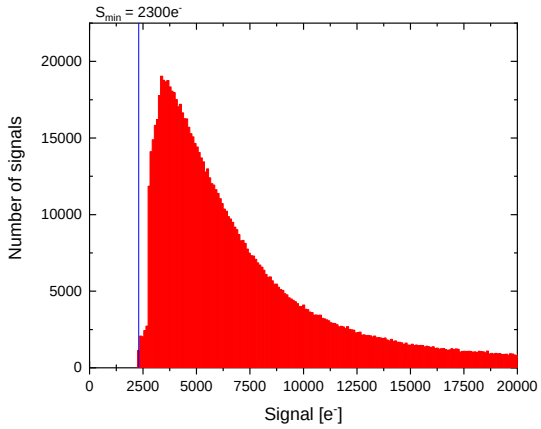

Fig. 16 ATLASpix3 tested in 3 GeV electron beam. Signal spectrum obtained by measuring ToT and by calibrating ToT with the injection circuit. High voltage bias was -50 V.

The signals produced by charged particles are Landau-distributed. The mean value of energy loss can be calculated from the Bethe equation [35]. The most probable value (MPV) of energy loss is below the mean. The energy loss depends on particle type, particle energy and the thickness of the active detector volume. There is a minimum of energy loss for particles with a certain energy. Particles with this energy are referred to as minimum ionizing particles (MIPs). The MPV of the energy loss of MIPs is used as the standard signal for a SNR calculation. In our case, signal values were measured at the test beam facility at DESY, Hamburg, Germany in the 3 GeV electron beam. 3 GeV electrons generate signals sufficiently close to the ones of MIPs. The signal spectrum can be measured by recording time over threshold (ToT) which can be translated to signal amplitudes. Fig. 16 shows the electron spectrum obtained by measuring ToT. The x-axis was calculated by using a calibration curve of ToT vs input signal obtained with the injection circuit. The MPV is about 3660 e⁻. The MPV signal to average noise ratio is 52.

The depleted region depth estimated by TCAD simulations is about 32 μm for - 50 V bias voltage and 300 Ωcm substrate resistivity.

Fig. 17 shows the number of signals for every pixel during

one measurement session. The position of the beam can be recognized.

A detailed study of time resolution is beyond the scope of this publication. It will require additional measurements at beam facilities. As mentioned in I.C, time resolution is to a large extent limited by time walk (TW), an effect caused by the fluctuation of the input signal, as shown in Fig. 16. Since amplified signal has a finite rise time T_r (3), the threshold crossing occurs later for weaker signals.

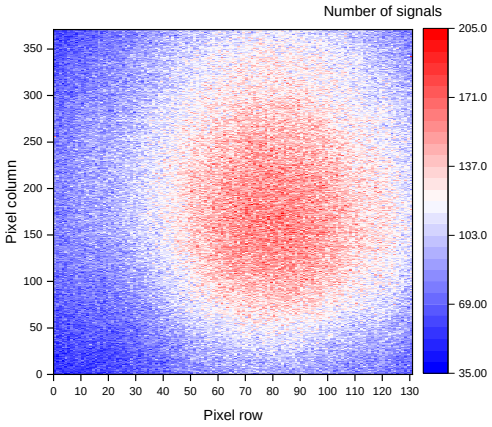

Fig. 17 ATALSPX3 tested in 3 GeV electron beam. Number of signals for every pixel during one measurement run. Position of the beam can be recognized. High voltage bias was - 50 V.

TW can be estimated by measuring the relation of the injection pulse delay and generated time stamp value for different injection amplitudes. Average time walk for all pixels between the injected signal of 3500 e^-, which corresponds to the MPV of the spectrum in Fig. 16, and the signal of 7000 e^- is about 7.5 ns. Tuned delay distribution for all pixels has sigma of 1.7 ns. The average input referred threshold during this measurement was about 980 e^-. Reducing of rise time constant T_r would diminish TW. A smaller T_r can be achieved by reduction of the n-well capacitance C_i. A large part of this capacitance is caused by the metal shield, which can be optimized in the next chip version. Nevertheless, the time walk achieved in this measurement is within the value specified for ATLAS (< 25 ns).

As mentioned in section I.C, one figure of merit for the time resolution is the ratio between signal S and threshold Th: S/Th should be larger than 2.06 for 99% of signals and pixels. Instead measuring the ratio S/Th for each pixel and signal, we will examine the input referred threshold- and signal distributions shown in Fig. 15 and Fig. 16 respectively. The maximum tuned threshold for 99% pixels with smallest thresholds (99% quantile) is $Th_{i,max} \approx 1.02$ ke (histogram 3, Fig. 15). The minimum signal from Fig. 16 is $S_{min} = 2.30$ ke. The ratio $S_{min}/Th_{i,max}$ is 2.25, which is greater than required 2.06.

Typical current consumption of the chip is 230 mA from 1.8 V and 130 mA from 1.2 V power supply voltage. The corresponding power dissipation is 570 mW. Measured substrate current at - 50 V bias voltage was 60 nA for the whole chip. This value can increase significantly after irradiation.

A. *Comparison with Measurements on similar Sensors*

This simulated value for depleted region depth roughly matches to the measurement results in [13] [14] [15]. These measurements have been performed on passive deep n-well in p-substrate diodes, some of them implemented in a 350 nm HVCMOS technology on the same substrate as used for ATLASpix3. (The substrates have been acquired by us and used by both foundries.) Publications [13] [14] [15] show radiation tolerance of the passive diodes. References [11] [12] investigate radiation tolerance of the active HVCMOS pixels. A smart diode detector implemented in a similar 180 nm process as ATLASpix3 provided by different foundry on the same substrate was found to be tolerant with detection efficiency of 99.4% to radiation damage (ionizing and non-ionizing effects) up to fluences in the order of 10^{15} n_{eq}/cm^2.

VI. Conclusion

ATLASpix3 is an active pixel sensor designed for detection and tracking of high energy charged particles. It is a system on a chip which consists of a matrix of 132 × 372 pixels, each 150 µm × 50 µm in size and a periphery with complex digital circuits, voltage generators and IO pads. The chip area is 20.2 mm × 21 mm. The pixels use deep n-well in p-substrate sensor diodes with the pixel electronics embedded in the deep n-wells. The diodes are depleted by biasing the substrate with a negative voltage of typically - 50 V with respect to the n-wells. ATLASpix3 has been implemented in a 180 nm HVCMOS process and produced within an engineering run. Lowly doped (high resistivity) substrates of 200 – 400 Ωcm have been used. The use of high voltage and high resistivity substrates leads to a depleted region depth of at least 30 µm. The design was described and measurements presented. The chip was tested by means of electrical signals and at a high energy electron beam facility. Signal to noise ratio of > 50 was measured when electrons of 3 GeV are detected. Input referred threshold distribution can be tuned down to σ ≈ 58 e^- and average input referred noise r. m. s. is 71 e^-.

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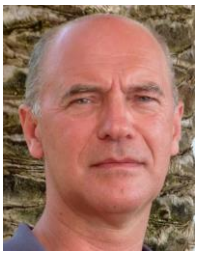
His research interests include HVCMOS sensor development and their characterization, comprising development of hardware, firmware and software, and data analysis.



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Since 2009, he is professor for experimental physics at Heidelberg University. His research group is studying proton-proton collisions at highest energies at the Large Hadron Collider at CERN and contributing to the development and construction of the Mu3e experiment at the Paul-Scherrer Institute (Switzerland). Since 2011 the research group is also developing monolithic pixel sensors for the instrumentation of particle detectors.

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