Lecture 9

The theme of this lecture are differential amplifiers. We will describe:

Applications

Classification

Differential and common mode gain, CMRR

Fully differential amplifier

- Common mode feedback

Operational amplifier

- Variant with R_{load}
- Variant with current mirror

Differential amplifiers

In the previous lectures we had the amplifiers with one input and an output, precisely single ended input and single ended output. These amplifiers are called single-ended amplifiers.

Single-ended means that the signals are measured with respect to ground. A simple realization is the common source amplifier. Figure 1 shows the symbol of a single-ended amplifier and its small signal model.

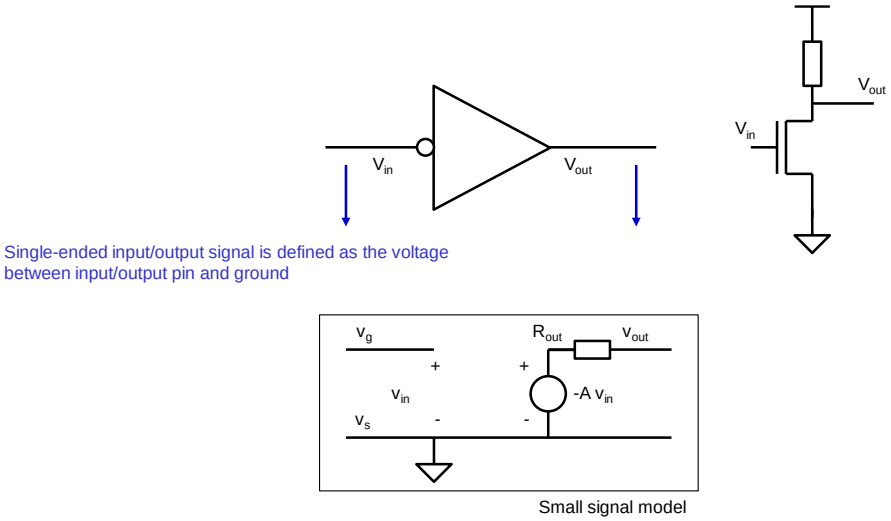


Fig 1: Single ended amplifier

In the case of differential amplifiers, at least the input is a differential signal. V_{out} is either a single-ended (Figure 2, left) or differential (Figure 2, right).

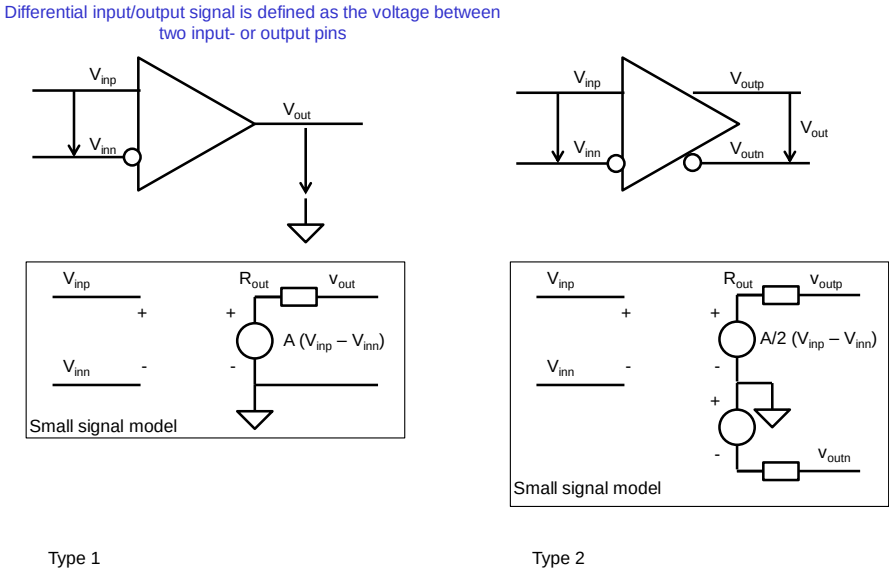
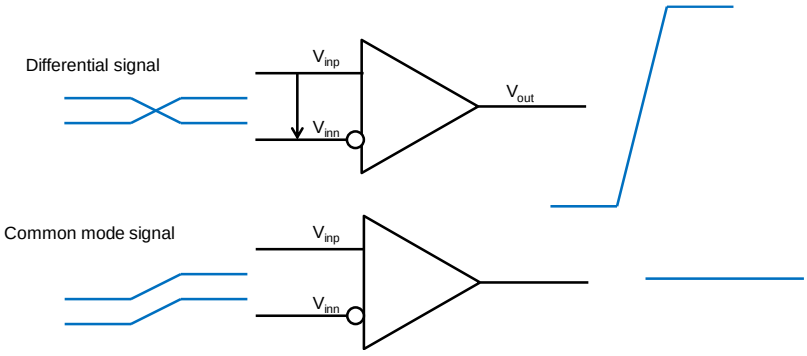


Fig 2: Differential Amplifier

It holds:

$$V_{out} = A\,(V_{inp} - V_{inn})$$

A differential amplifier should not amplify "common mode" signals. If the two input signals increase by the same contribution, the output should remain unchanged.



Differential amplifier

Applications of differential amplifiers

Measurement of two signals relative to each other

The first application of differential amplifiers is the measurement of two signals relative to each other.

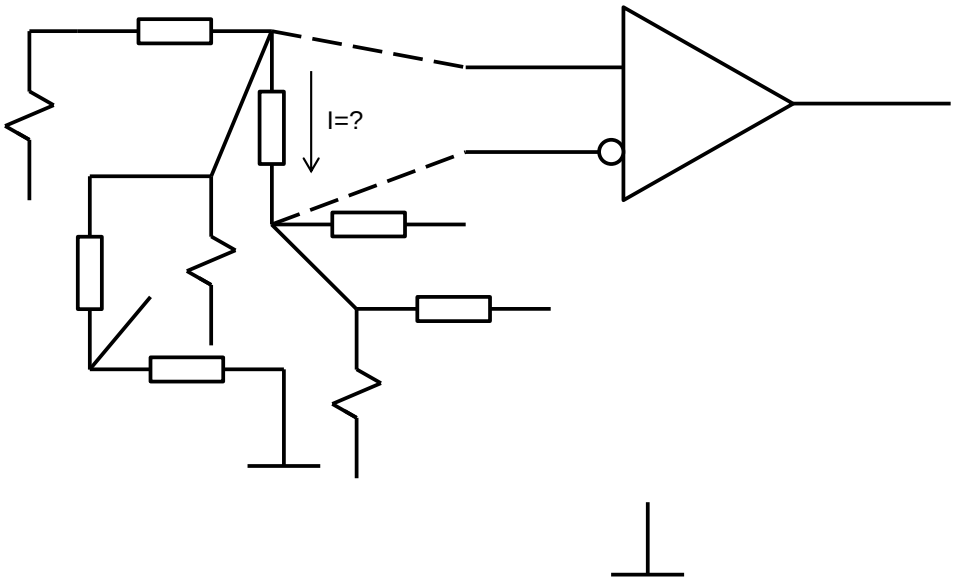


Fig 3: Applications: measurements of voltage differences

Assume that we develop an amplifier that measures the currents flowing through resistors (Fig 3). The device should only measure the voltages across resistances and not the potentials with respect to ground. We use differential amplifier for this purpose.

Differential signal processing

Another application of differential amplifiers is **differential signal processing**. The idea is that a signal is not transmitted as a voltage referenced to ground on a single line, but rather as a potential difference between two symmetrical lines. Ideally, the two line voltages have a constant sum, that is, they are 180 degrees out of phase. This concept is illustrated in Fig 4.

This type of signal transmission has several advantages.

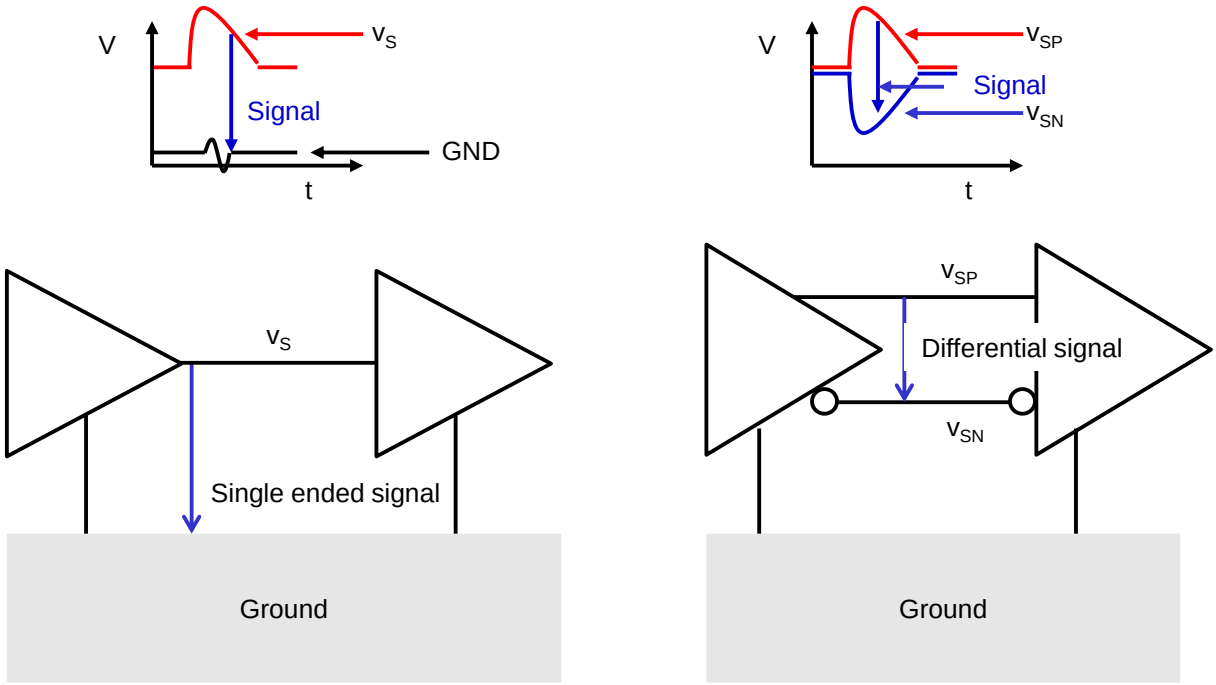


Fig 4: Single ended and differential signal

First, the amplitude of the differential signal is twice as large as the amplitude of each individual voltage (see Fig 5). A larger amplitude also implies a higher signal-to-noise ratio.

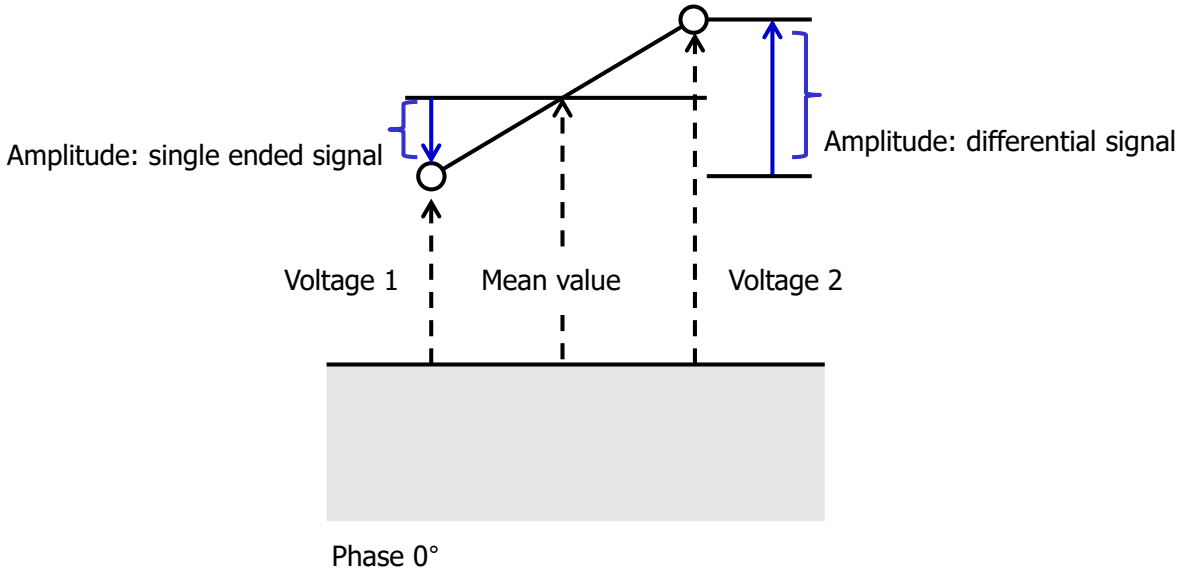


Fig 5: The amplitude of the differential signal is two times larger than the amplitude of each voltage when individually considered

Consider a circuit designed in modern chip technology, where the supply voltage is only about 1.0 V. A single-ended signal can therefore have a maximum peak-to-peak amplitude of 1 V. A differential signal, on the other hand, can have a maximum peak-to-peak amplitude of 2 V. For the same signal-to-noise ratio, twice as much noise can be tolerated in the case of differential signalling. Fig 6 illustrates this.

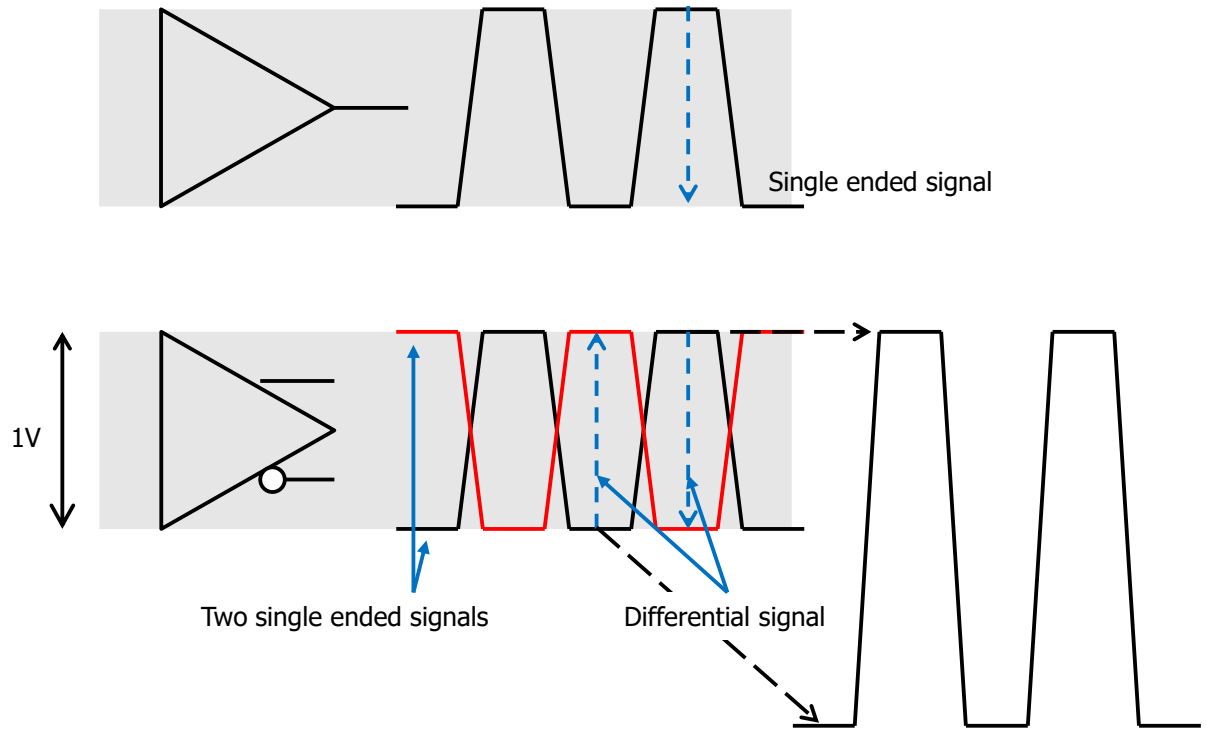


Fig 6: The amplitude of the differential signal is twice as large as the amplitude of each individual voltages

If the two voltages of a differential pair have a constant sum, they generate very little electromagnetic interference at a distance. Furthermore, capacitive or inductive crosstalk from external sources has only a small influence on a differential signal. This is illustrated in Fig 7.

Imagine that a single-ended signal line (for example, a CMOS line) is routed above a differential pair of lines. Both voltages of the differential pair are slightly disturbed by capacitive crosstalk from the CMOS line. These disturbances are in phase. If the receiver amplifies only the voltage difference, such disturbances do not affect signal reception and are therefore not amplified.

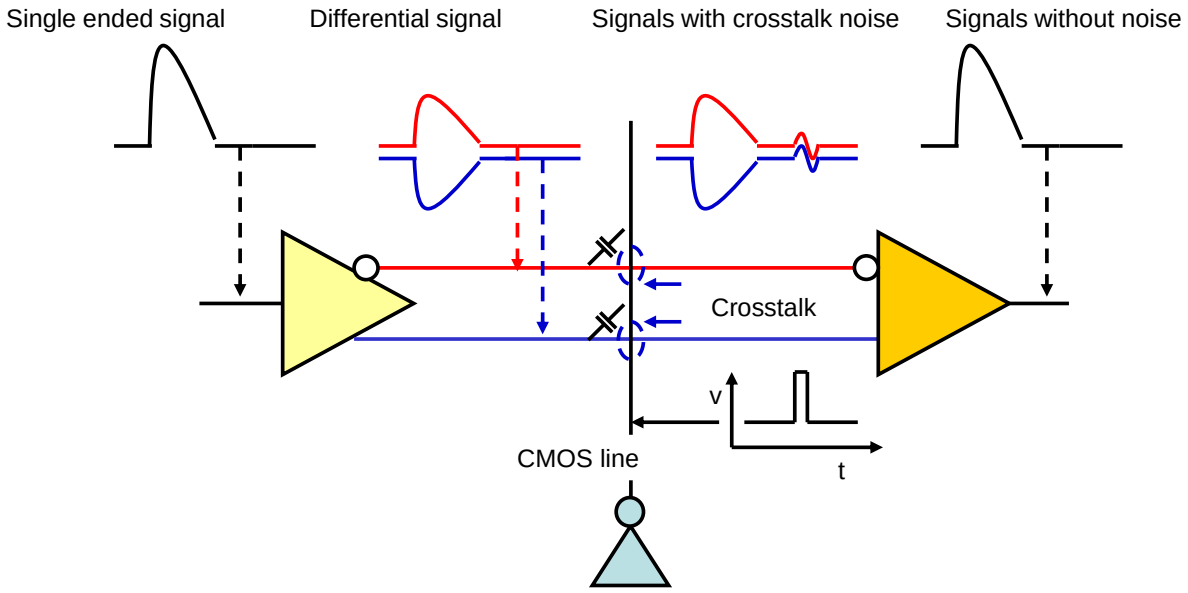


Fig 7: Capacitive or inductive crosstalk from externals has a small influence to a differential signal

Operational Amplifier

The differential amplifier is used as a basic electronic component, the operational amplifier. Various circuits can be realized using the operational amplifier, such as the feedback amplifiers, filters, oscillators and different mathematical operations (integrator, differentiator). Hence the name operational amplifier.

Fig 8 shows the inverting and the non-inverting amplifier.

Notice that we can also implement an inverting amplifier with a single ended amplifier, while a non-inverting amplifier requires a differential amplifier.

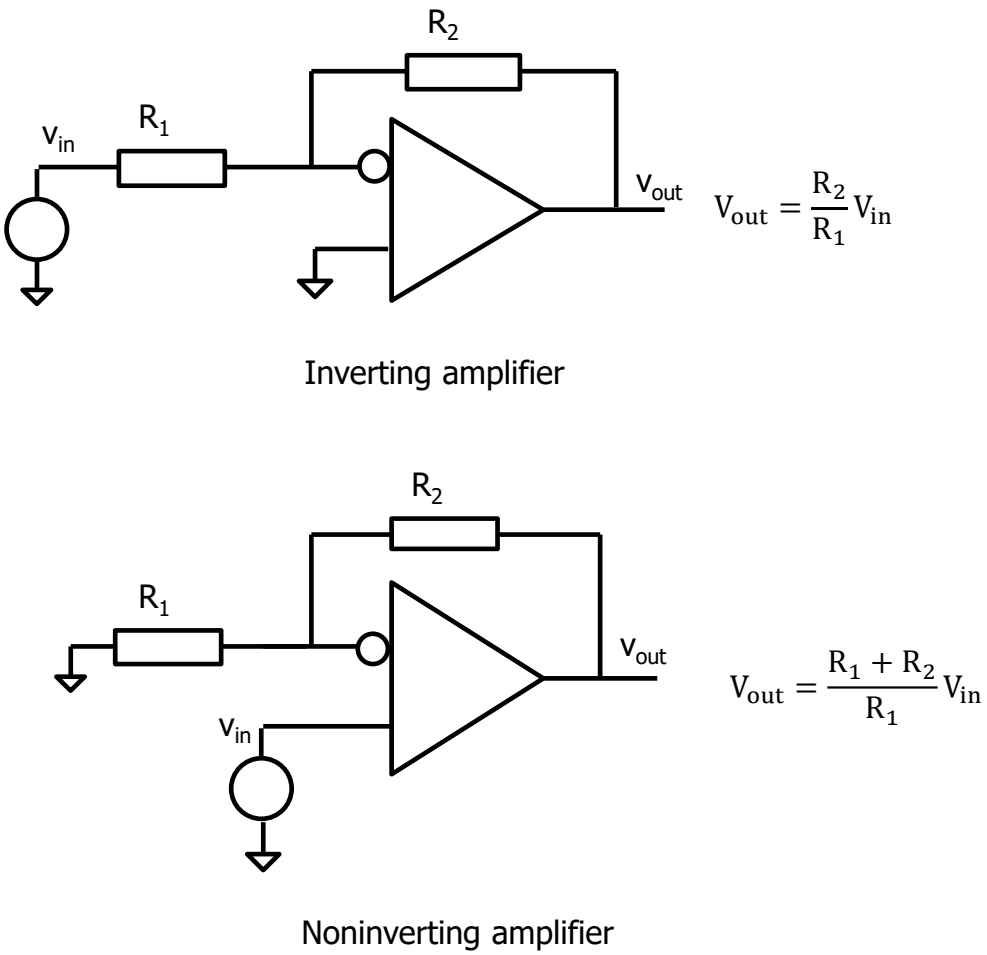


Fig 8: Inverting and noninverting amplifier

Comparator

Another application is the comparator. Fig 9 shows an analogue comparator and its input and output signals. The output signal changes between VDD and GND, depending whether V_{inp} is larger or smaller than V_{inn}.

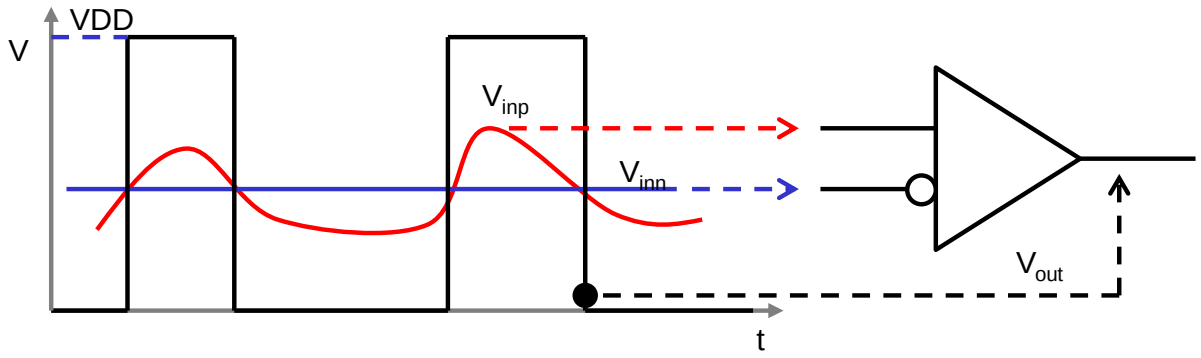


Fig 9: Differential amplifier as comparator

Digital Circuits

Differential amplifiers can also be used in digital circuits. Typical examples are receivers and drivers for differential data transmission (Fig 10). The advantage of this type of transmission is that the amplitude of the differential signal is twice as large as the amplitude of each individual voltage of the line pair. As a result, logical levels (bits) can be reliably transmitted using a smaller voltage swing on each line. Low-Voltage Differential Signaling (LVDS) operates based on this principle.

Logical components such as gates or flip-flops can also be implemented using differential amplifiers. This type of logic always consumes a constant current. As a result, it does not cause voltage fluctuations on the supply lines, even if these lines have significant resistance. Fig 11 shows an SR latch, a D latch, and a ring oscillator.

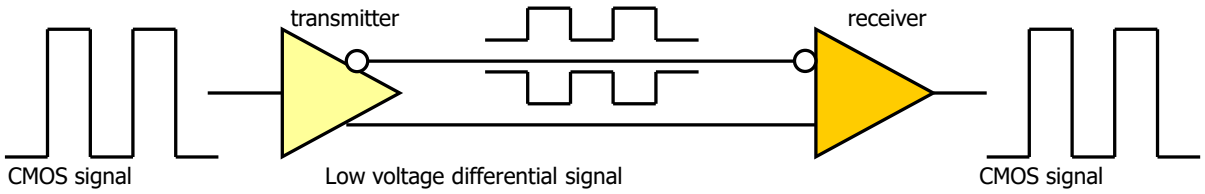


Fig 10: Low voltage differential signalling

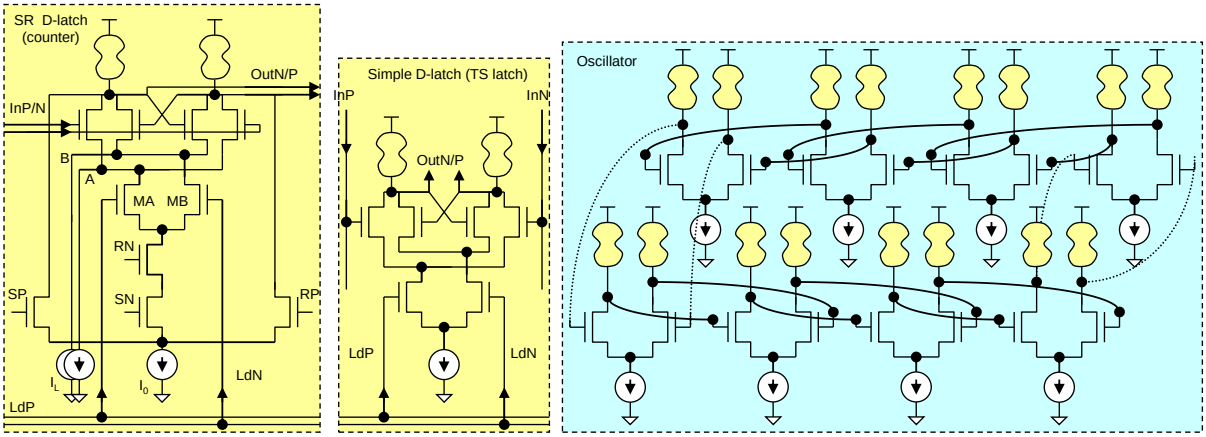


Fig 11: Differential logic gates

Classes of differential amplifiers

Differential amplifiers can be classified according to their input and output types (single-ended or differential), Fig 12.

For example, an operational amplifier typically has a differential input (two input pins) and a single-ended output. The output voltage is referenced to ground.

There are also differential amplifiers with differential outputs. In this case, the two output voltages have opposite phases, and their sum remains constant. Such amplifiers are referred to as fully differential amplifiers.

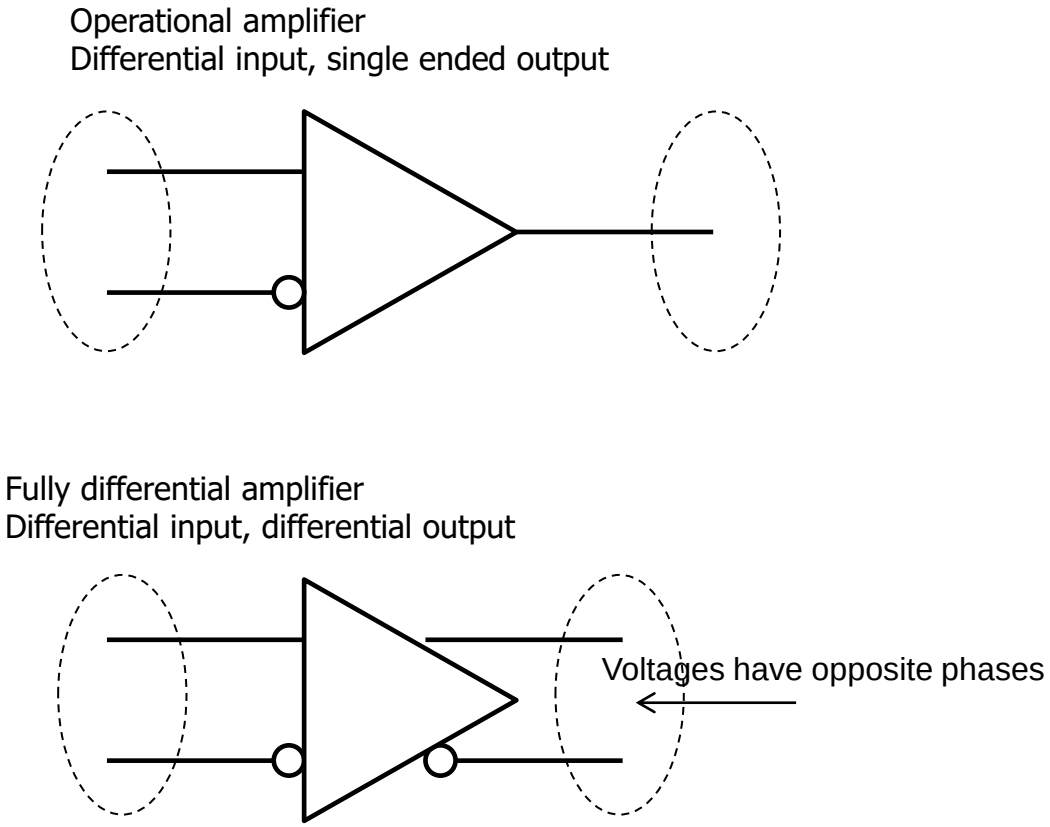


Fig 12: Different types of differential amplifiers

The main application of fully differential amplifiers is precise analog signal processing. For example, such amplifiers are widely used in switched-capacitor amplifiers. (Fig 13).

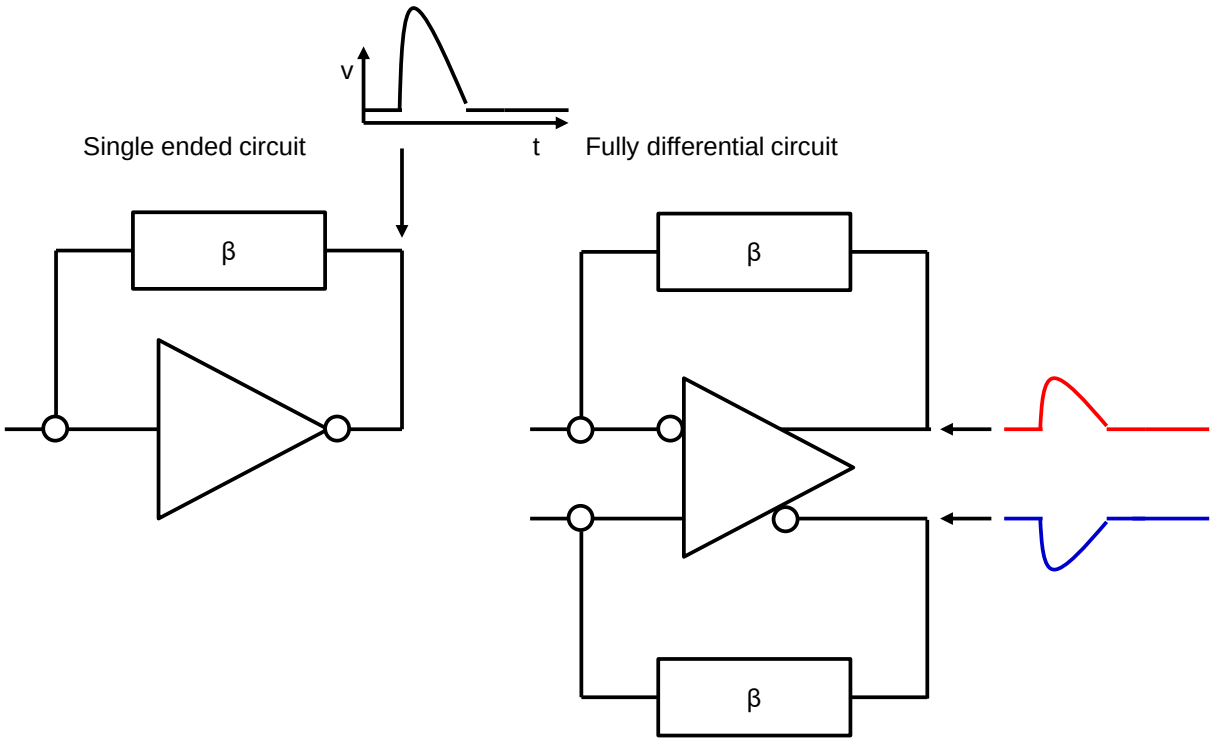


Fig 13: Single ended- and differential analogue signal processing

Transistor implementation

The basic building block of a differential amplifier is the **differential pair**. The pair consists of two identical transistors, T_{in1} and T_{in2} that share one bias current (Fig 14). This bias current is generated either by a current source I_{bias} or by a large resistor R_{bias}. The source electrodes of T_{in1} and T_{in2} are usually connected together. An increase in the current through one transistor of the pair leads to an equal decrease in the current through the other transistor. Therefore, the following relation holds: $I_{ds1} + I_{ds2} = I_{bias}$

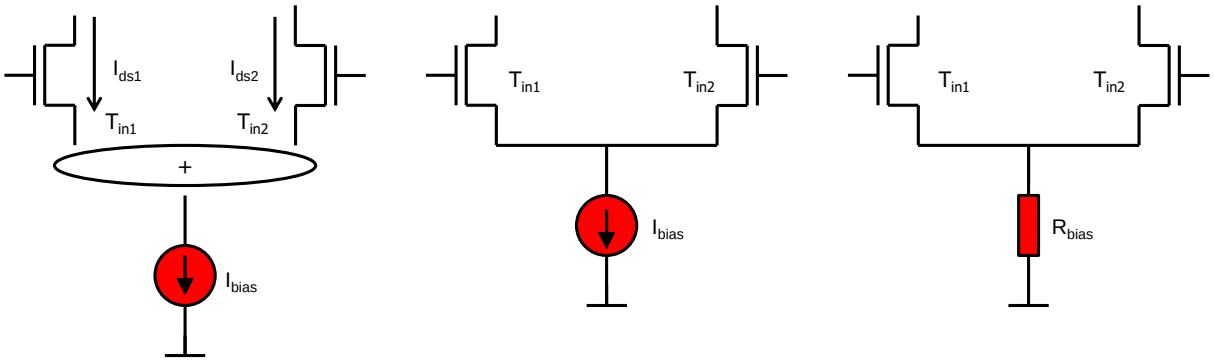


Fig 14: Differential pair

V-I Converter

To explain the operation of the differential pair, we first introduce a simpler building block: a **voltage-to-current (V–I) converter**. It is based on a transistor with a resistor connected between the source electrode and ground (see Figure 15). The drain of the transistor serves as the current output and is connected to a constant voltage V_{out}, which ensures that the transistor operates in the saturation region.

The current gain can be derived as follows.

It holds:

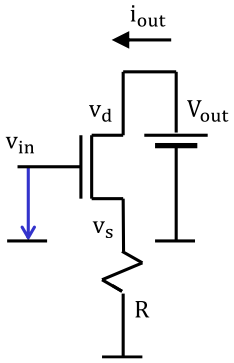


Fig 15: V-I Convertor

$i_{out}R = v_s$ und $v_g = v_{in}$

It follows (we neglect r_{ds} of the transistor):

$$i_{out} = g_m v_{gs} = g_m v_{in} - g_m i_{out} R$$

and

$$i_{out}(1 + g_m R) = g_m v_{in}$$

and

$$i_{out} = \frac{g_m}{(1+g_m R)} v_{in}$$

The current gain is:

$$G = \frac{i_{out}}{v_{in}} = \frac{g_m}{1+g_m R} \qquad (1)$$

Let us calculate the output resistance. Fig 16 shows the small signal circuit for calculating R_{out}.

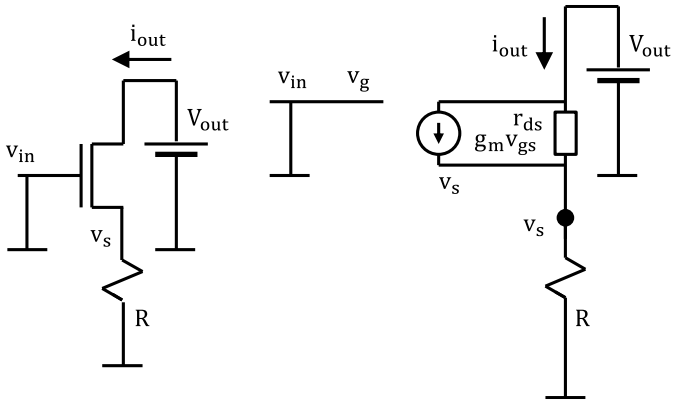


Fig 16: Kleinsignalschaltung für Berechnung von R_{out}

Output resistance is defined as $\frac{v_{out}}{i_{out}} = R_{out}$.

If we know v_s, we can calculate i_{out} as follows:

$$i_{out} = \frac{v_s}{R}$$

To calculate v_s, we use the method of nodal potentials. We write the equation for all currents that flow into the node v_s. The sum of the currents is 0:

$$0 = -\frac{v_s}{R} + \frac{(v_{out} - v_s)}{r_{ds}} + g_m v_{gs}$$

It follows

$$v_s = \frac{v_{out}}{r_{ds}\left(\frac{1}{R} + \frac{1}{r_{ds}} + g_m\right)}$$

therefore

$$i_{out} = \frac{v_s}{R} = \frac{v_{out}}{r_{ds} R\left(\frac{1}{R} + \frac{1}{r_{ds}} + g_m\right)}$$

and

$$R_{out} = (r_{ds} + R)(1 + g_m(r_{ds}||R)) \quad (2)$$

Summary

The current gain of the U-I converter is:

$$G = \frac{i_{out}}{v_{in}} = \frac{g_m}{1 + g_m R} \qquad (3)$$

The output resistance is:

$$R_{out} = (R + r_{ds})[1 + g_m(R||r_{ds})] = (1 + R g_m) r_{ds} \qquad (4)$$

Fully differential amplifier

We can obtain a fully differential amplifier by taking two single-ended amplifiers (in simplest case two common source amplifiers), by connecting the sources of two input transistors and by biasing of such common source (node S in Fig 17) using a resistor R_{bias} or a current source.

The output is defined as $\Delta V_{out} = V_{out1} - V_{out2}$.

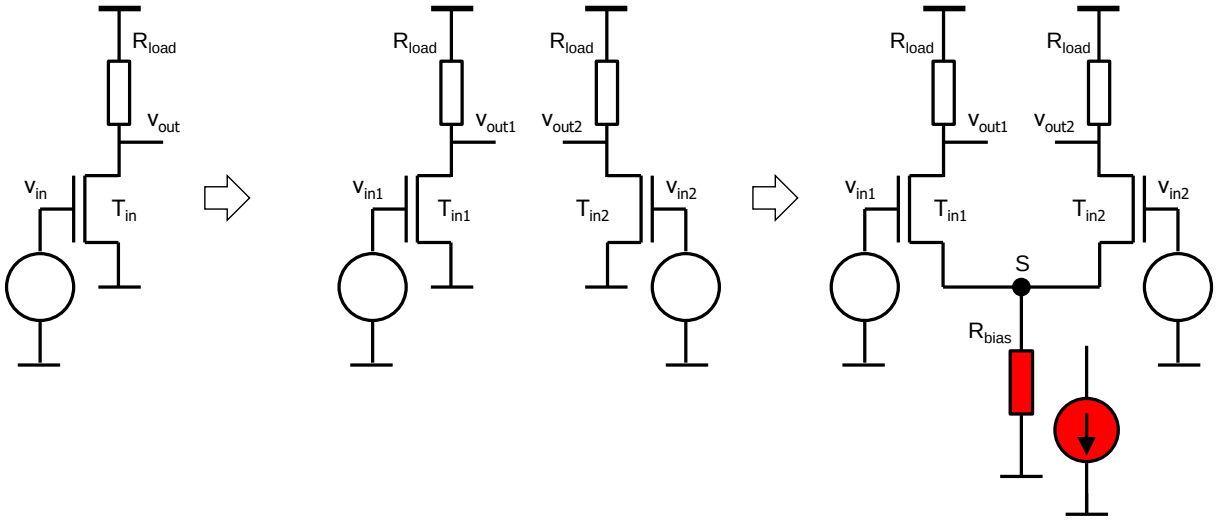


Fig 17: Fully differential amplifier

Let us calculate the voltage gain.

Since we have two output voltages (V_{out1} and V_{out2}) we can for each of them define amplifications.

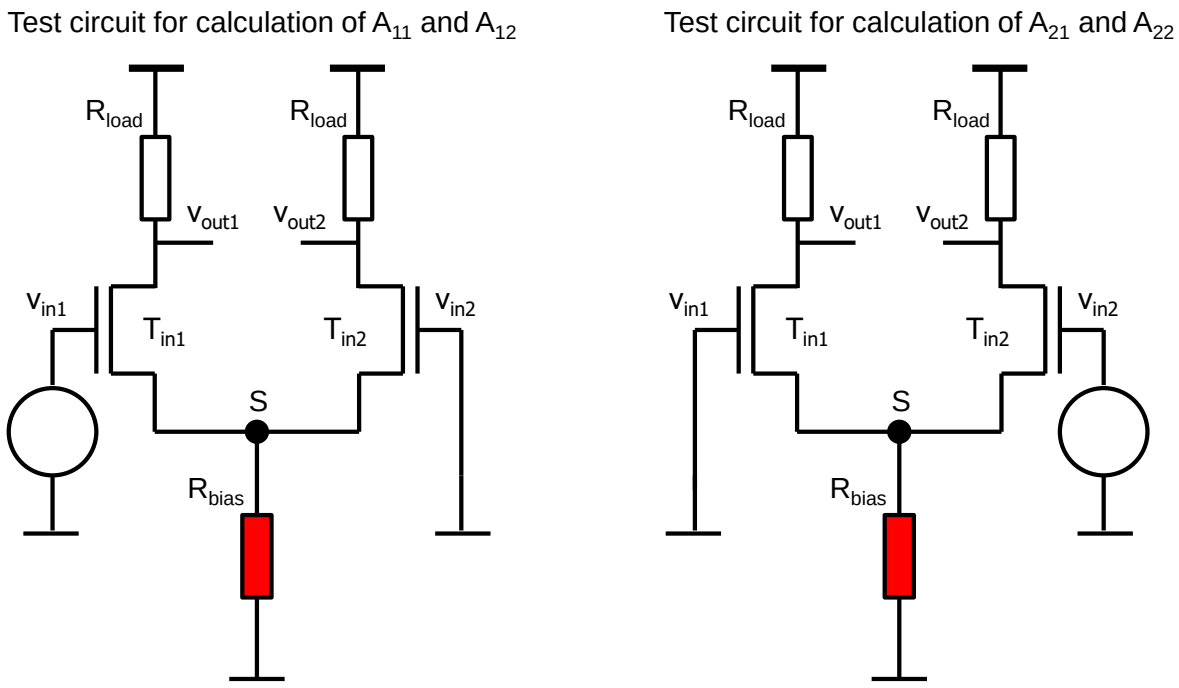


Fig 18: Fully differential amplifier: Test circuits for the calculation of different gains

We could further apply the principle of superposition and consider the two input voltage sources individually. We switch off source V_{in2} by replacing it with a short circuit to ground and calculate the outputs as a function of V_{in1}. In this way we obtain the gains: $A_{11} = V_{out1}/V_{in1}$ and $A_{12} = \Delta V_{out2}/V_{in1}$ (Fig 18, left).

Then we repeat the calculation for the second source and calculate A_{21} und A_{22} (Fig 18, right).

We will calculate the gain in a bit different way:

It is possible to express two input voltages as a sum of its mean value (referred to as the common mode voltage) and the difference voltage (Fig 19).

We define the difference voltage as:

$$v_{diff} = v_1 - v_2$$

The common mode voltage is defined as:

$$v_{cm} = \frac{v_1 + v_2}{2}$$

It holds:

$$v_1 = v_{cm} + \frac{v_{diff}}{2}$$

$$v_2 = v_{cm} - \frac{v_{diff}}{2}$$

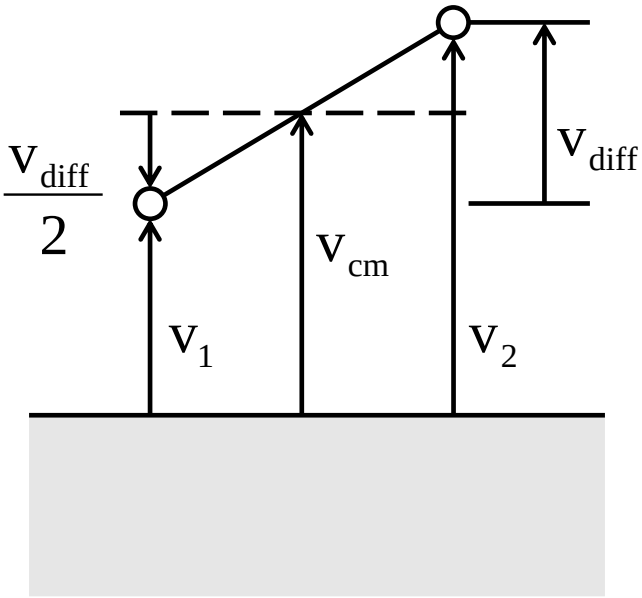


Fig 19: Representation of two voltages v_1 and v_2 as sum of voltage difference v_{diff} and common mode voltage v_{cm}

Therefore we can replace the voltage sources v_{in1} and v_{in2} with voltage sources v_{cm} and v_{diff} (Fig 18).

$$v_{diff} = v_{in1} - v_{in2} \qquad (5)$$

$$v_{cm} = \frac{v_{in1} + v_{in2}}{2} \qquad (6)$$

We define the differential gain as:

$$A_{diff} = \frac{v_{out,diff}}{v_{diff}} \qquad (7)$$

And the common-mode gain as:

$$A_{cm} = \frac{v_{out,diff}}{v_{cm}} \qquad (8)$$

Why did we replace v_{in1} and v_{in2} with v_{diff} and v_{cm}?

Firstly, the test circuits for the calculation of A_{diff} and A_{cm} (Fig 20) are more symmetrical than the circuits for calculation of $A_{11} – A_{22}$ (Fig 18). We can make use of this symmetry to simplify the circuits. Secondly, it holds often $A_{cm} \sim 0$ and we need to calculate only one gain A_{diff}.

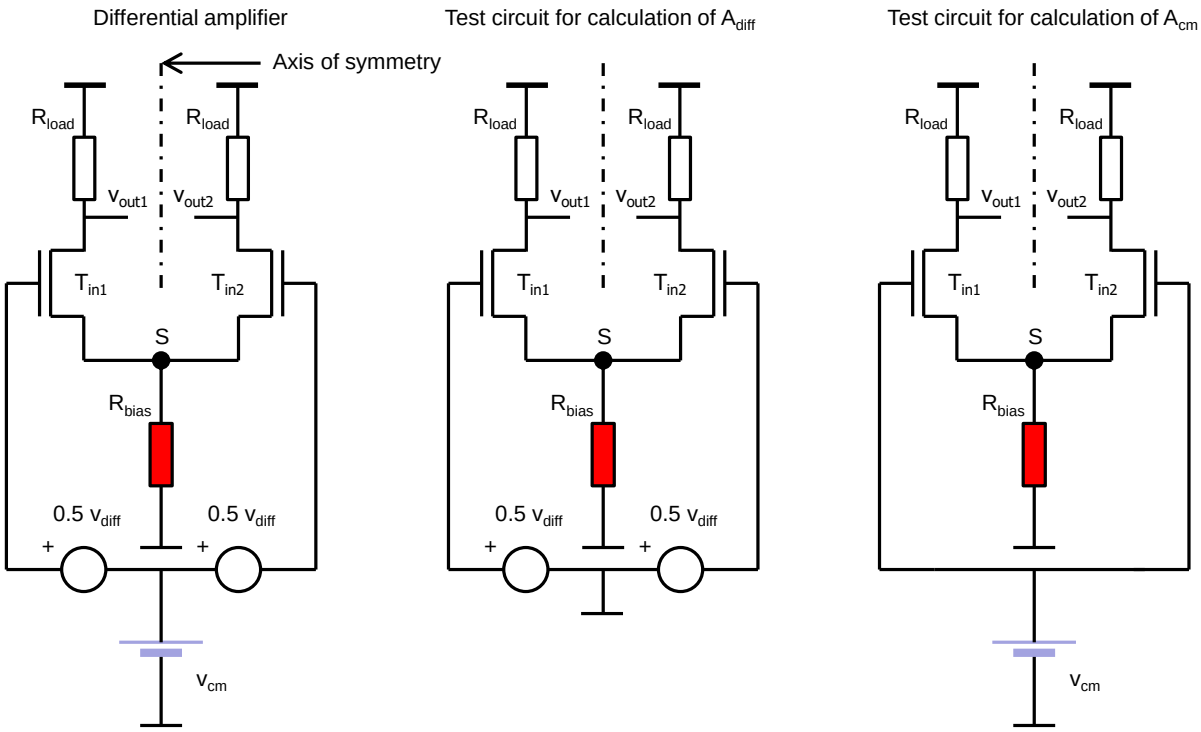


Fig 20: Symmetrical differential amplifier with differential and common mode voltage at the input. Middle figure: test circuit for A_{diff}. Right figure: test circuit for A_{cm}.

Differential gain

Let us first calculate the output voltages as function of v_{dff} and the differential gain A_{diff}.

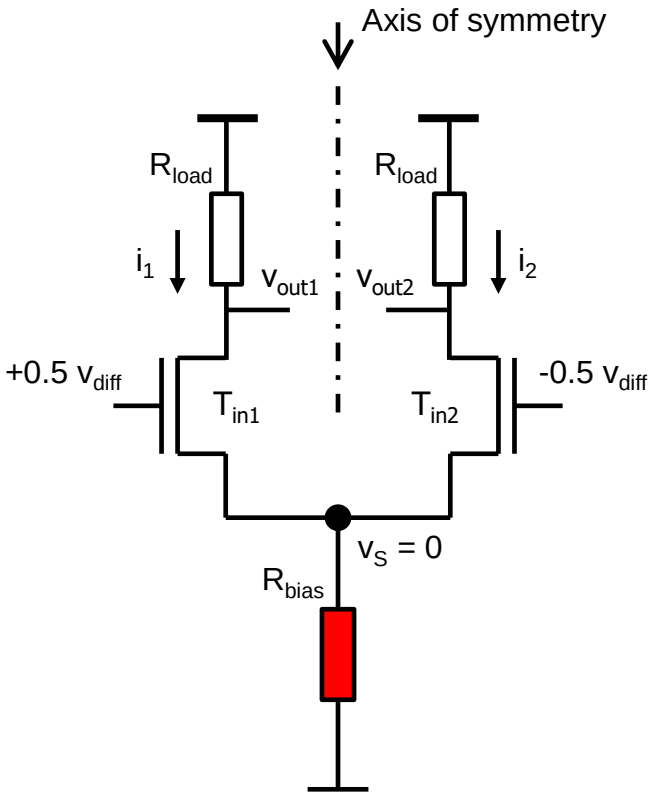


Fig 21: Test circuit for the calculation of the differential voltage gain

Since we perform AC-analysis we set v_{cm} and all DC voltage sources to zero (Fig 21).

The circuit is symmetrical in the sense that it remains unchanged when rotated by 180° about the symmetry axis. Since this rotation only changes the sign of the input voltages (while their magnitudes remain the same), the voltages at all other nodes also change only in sign. The node potentials along the symmetry axis are therefore zero, because zero is the only value for which a = -a. Note that this analysis is performed for small-signal (AC) operation. In the case of large-signal operation, the node potentials along the symmetry axis are constant, but not necessarily zero. Therefore, it follows that $v_s = 0$. We obtain:

$$i_1 = g_m \frac{v_{diff}}{2}$$

$$i_2 = -g_m \frac{v_{diff}}{2}$$

g_m is the transconductance of T_{in1} and T_{in2}.

The voltages v_{out1} and v_{out2} are:

$$v_{out1} = -g_m R_{load} \frac{v_{diff}}{2} \qquad (9)$$

$$v_{out2} = g_m R_{load} \frac{v_{diff}}{2}$$

The differential gain is:

$$A_{diff} = \frac{v_{out1} - v_{out2}}{v_{diff}} = -g_m R_{load} \qquad (10)$$

Common mode gain

Let us now calculate the output voltage as a function of the common-mode input voltage v_{cm} and the common-mode gain A_{cm}.

We set the differential input voltage v_{diff} to zero and apply only v_{cm}, as shown in Fig 22.

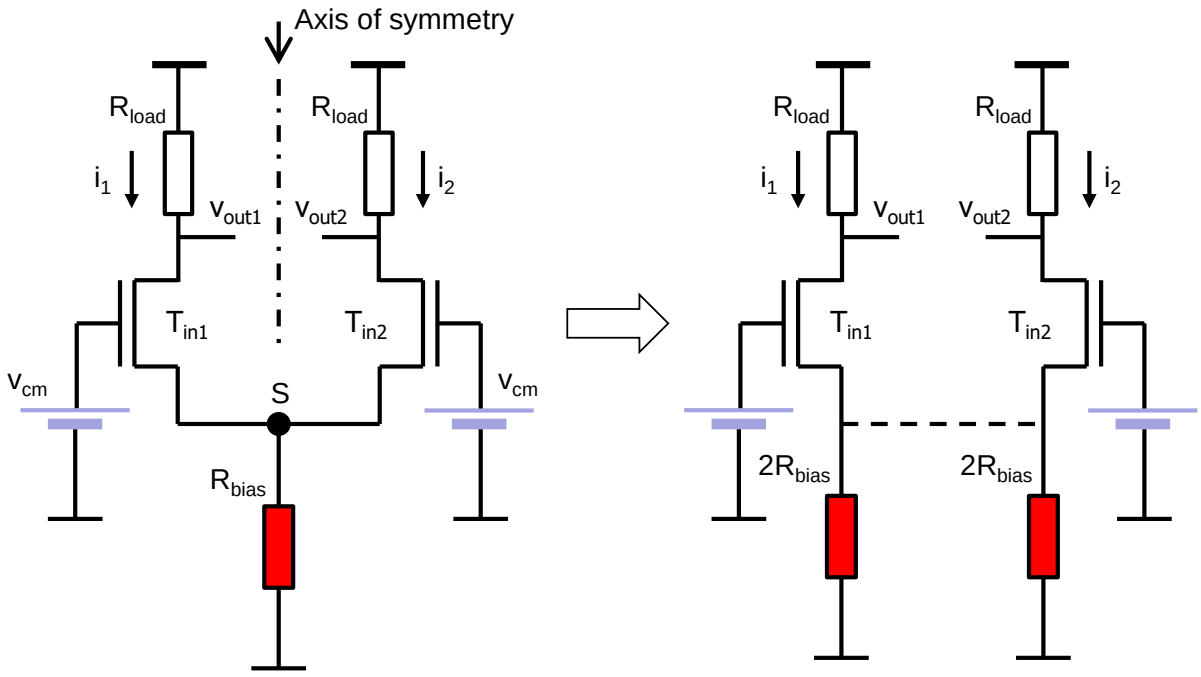


Fig 22: Test circuit for the calculation of the common mode gain

In this case, the circuit is symmetrical under a 180° rotation about the symmetry axis. When the circuit is rotated, the input voltages remain unchanged, as do all other node voltages. Since the node potentials on the left and right sides of the symmetry axis are equal, no current flows through the connections that intersect the symmetry axis. This allows us to split the circuit into two identical halves (Fig 22, right).

The resistances $2R_{bias}$ introduce feedback in each half of the circuit in the same way as in a V–I converter, thereby reducing the drain currents.

It holds:

$$i_1 = i_2 = v_{cm} \frac{g_m}{1+2g_m R_{bias}}$$

It holds for the voltages at the output:

$$v_{out1} = v_{out2} = -v_{cm} \frac{g_m R_{load}}{1+2g_m R_{bias}} \qquad (11)$$

Let us now calculate the common mode gain.

$$A_{cm} = \frac{v_{out1}-v_{out2}}{v_{cm}} = 0 \qquad (12)$$

We define a common mode rejection ratio (CMRR) as A_{diff}/A_{cm}. CMRR is in our case very large:

$$\mathrm{CMRR} = \frac{\mathrm{A_{diff}}}{\mathrm{A_{cm}}} = \infty \quad (13)$$

Fully differential amplifier based on folded cascade amplifiers

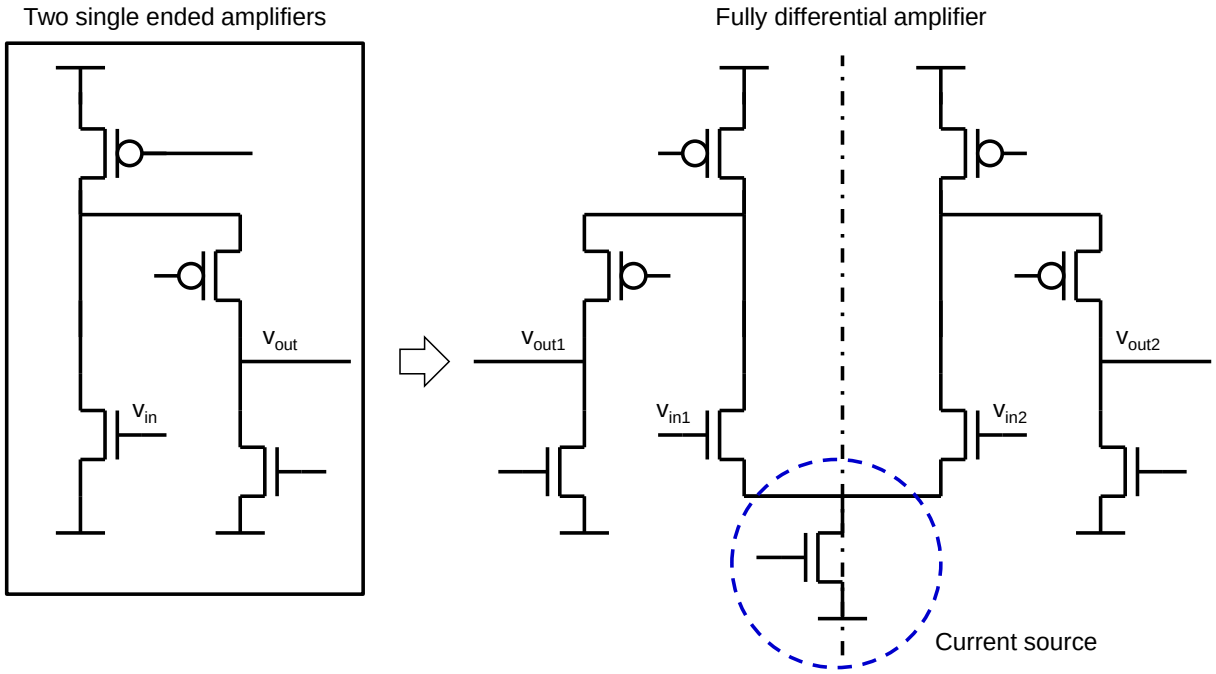


Fig 23: Fully differential amplifier based on two amplifiers with folded cascode

In the first example (Fig 17), we built a fully differential amplifier from two simple single-ended amplifiers (two common-source amplifiers). Instead of these simple stages, more complex single-ended amplifiers—such as folded-cascode amplifiers—can also be used to build a differential amplifier. Fig 23 shows a fully differential amplifier based on folded-cascode stages.

Fig 24 shows the complete circuit, including the biasing elements.

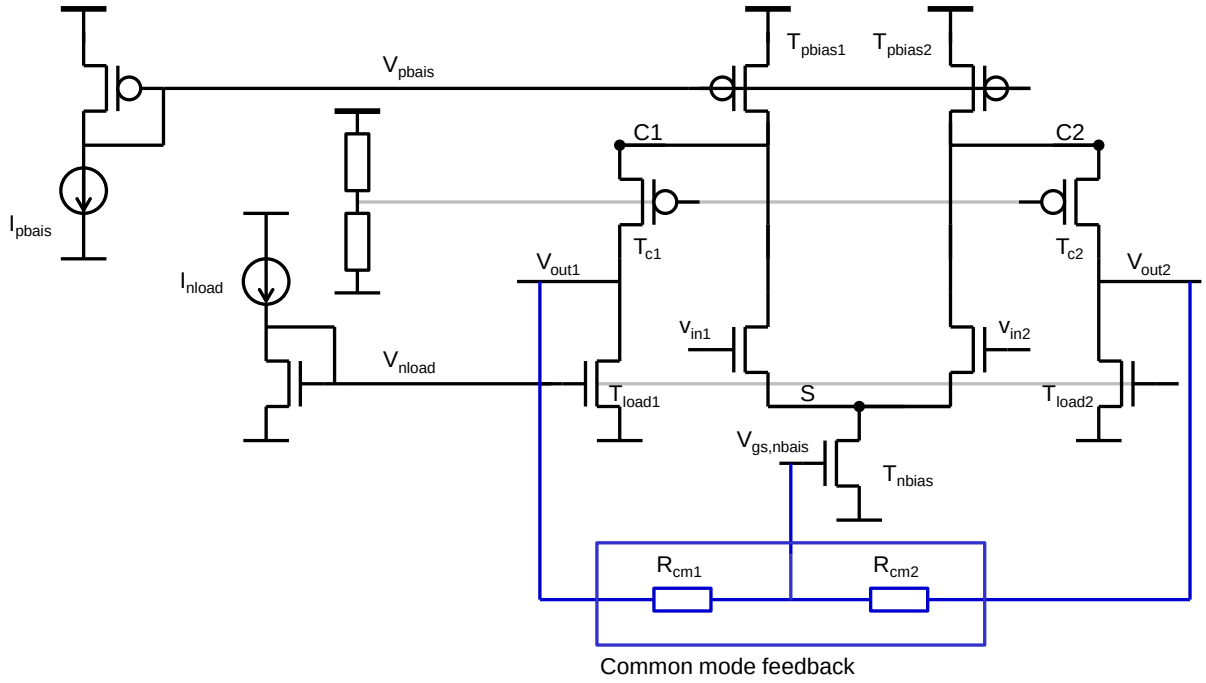


Fig 24: Fully differential amplifier with common mode feedback

Common mode feedback

A fully differential amplifier often requires **common-mode feedback (CMFB)**. We briefly discuss this concept here.

Without a common mode feedback, the following problem may occur.

If the sum of bias currents through T_{pbias1} and T_{pbias2} (sum of all currents through VDD) is different then the sum of bias currents through T_{load1}, T_{load2} and T_{nbias}, (sum of all currents to GND), the potentials of nodes C1, C2, Out1, Out2 and S will drift towards VDD or GND. This drift continues until either T_{pbias1} and T_{pbias2} or T_{load1}, T_{load2} and T_{nbias} enter the triode region.

As a consequence, the DC levels at Out1 and Out2 become too high or too low, which significantly reduces the amplifier gain.

To prevent this behavior, an active regulation of the gate voltage of T_{nbias} (V_{nbias}) is introduced.

This regulation ensures that the DC voltages at nodes Out1 and Out2 nodes remain approximately ½ VDD, so that all transistors operate in saturation.

We call this regulation the common mode feedback.

One of the simplest implementations uses two resistors, R_{cm1} and R_{cm2} as shown in the Fig 24.

Working principle

Assume that the currents through T_{pbias1} and T_{pbias2} are too large. In this case, more current flows into nodes C1 and C2 from VDD through T_{pbias1} and T_{pbias2} than flows to ground through T_{nbias},

T_{load1} and T_{load1}. As a result, the voltages at nodes C1 and C2 increase. This increases the $|v_{gs}|$ of transistors T_{c1} and T_{c2}, and consequently raises the output voltages Out1 and Out2.

The resistors $R_{cm1/2}$ ensure that:

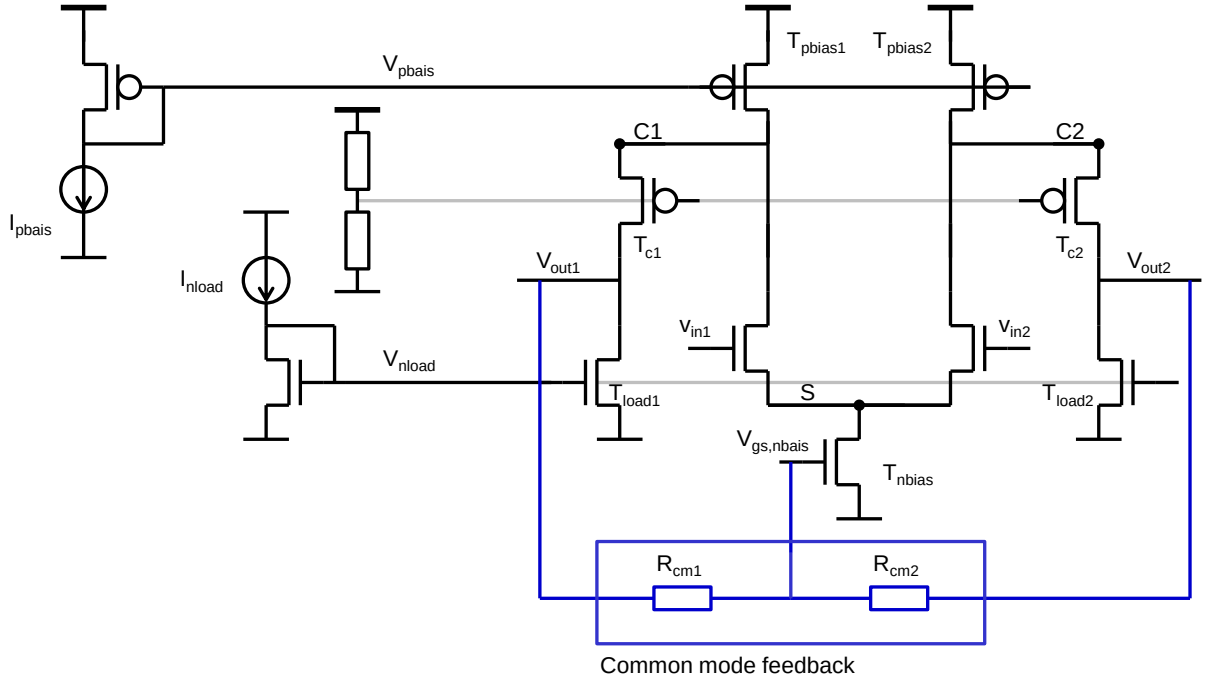
$$V_{gs,nbias} = \frac{V_{out1}+V_{out2}}{2}.$$

An increase in $V_{out1} + V_{out2}$ therefore increases $V_{gs,nbias,}$ which raises the current through T_{nbias}. In this way the equilibrium state is achieved:

$I_{ds,pbias1} + I_{ds,pbias2} = I_{ds,nbias} + I_{ds,nload1} + I_{ds,nload2}$

Once this balance is achieved, the output voltages V_{out1}, V_{out2} no longer increase.

When an input signal is amplified, the voltages v_{OUT1} und v_{OUT2} change such that their sum $v_{OUT1} + v_{OUT2}$ remains constant. The result of small gains v_{out1}/v_{cm} and v_{out2}/v_{cm} (11) is, that the small signals v_{out1} und v_{out2} have opposite signs and equal absolute values. Consequently, the voltage $v_{GS,NBIAS}$ and the current $i_{DS,NBIAS}$ stay constant.



Operational amplifier

We will now introduce the differential amplifier with the single ended output, i.e. an operational amplifier.

Simple operational amplifier

The simplest possibility to make an operational amplifier would be to take the fully differential amplifier from Fig 17 and use V_{out1} as output. This is shown in Fig 25.

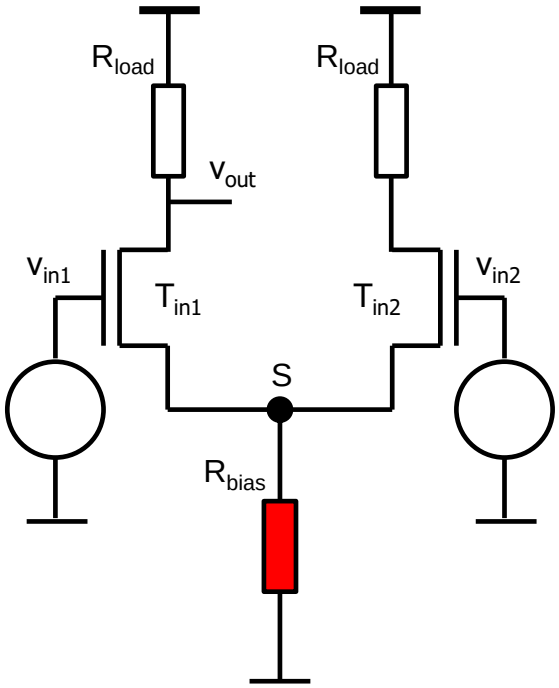


Fig 25: Simple differential amplifier with single ended output (operational amplifier)

The differential and common mode gain is: (it follows from (9) and (11)):

$$A_{diff} = \frac{V_{out1}}{v_{diff}} = -\frac{1}{2} g_m R_{load} \quad (14)$$

$$A_{cm} = \frac{V_{out1}}{v_{cm}} = -\frac{g_m R_{load}}{1+2g_m R_{bias}} \quad (15)$$

The CMRR is:

$$CMRR = \frac{A_{diff}}{A_{cm}} = \frac{1+2g_m R_{bias}}{2} \quad (16)$$

CMRR (16) relatively large, however not as large as in the case of the fully differential amplifier (13). The differential gain (14) is one half of the gain of the fully differential amplifier (10).

Operational amplifier with current mirror

If we extend the circuit from Fig 25 with an active current mirror (Fig 26), we achieve similarly good properties like in the case of the fully differential amplifier. We will explain this briefly:

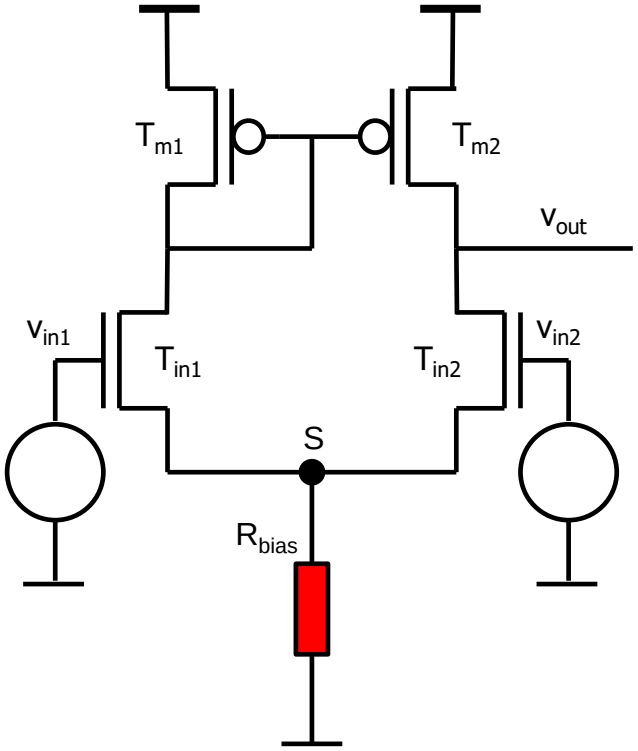


Fig 26: Operational amplifier with current mirror

The new circuit consists of a differential pair (T_{in1} and T_{in2}), a bias resistance R_{bias} or a current source and a current mirror (T_{m1} und T_{m2}).

Differential current gain

Let us now calculate the differential gain. Fig 27 shows the test circuit.

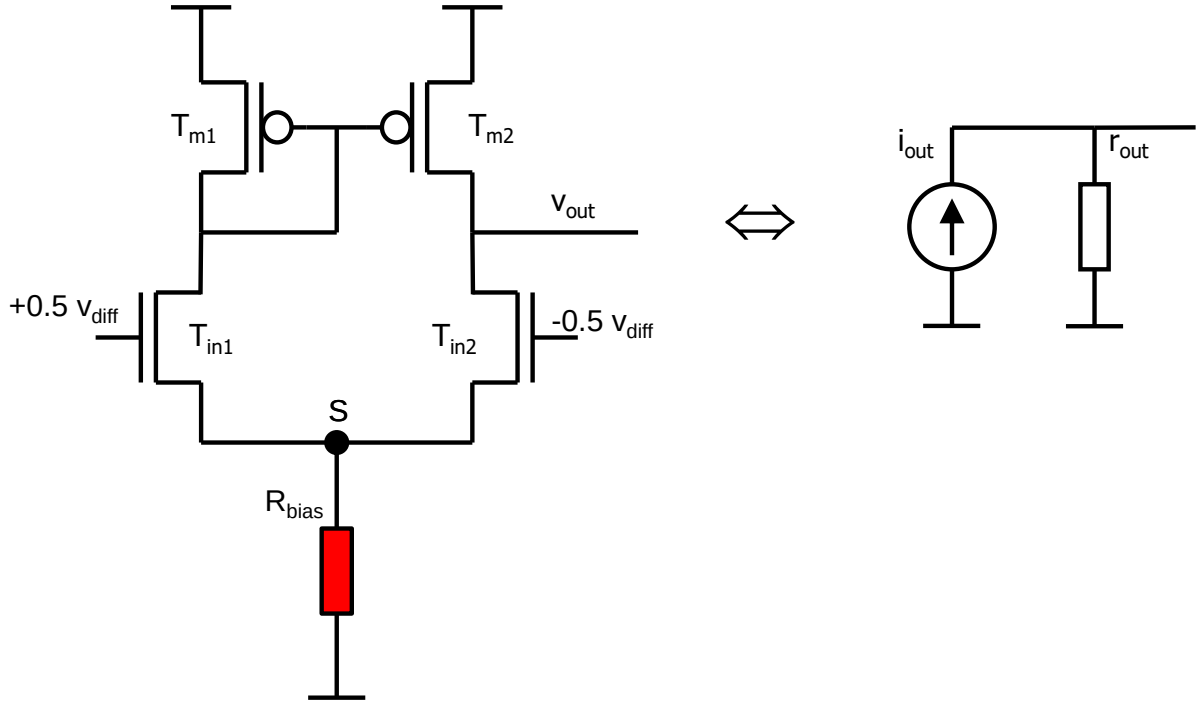


Fig 27: Small signal test circuit for the calculation of the differential gain. The amplifier can be represented as a current source.

We will proceed in the following way. We will not calculate the voltage gain directly then we will represent the differential amplifier as real current source – the Norton's current source. We will as first calculate the parameters of this current source: the short circuit current i_{out} and the internal resistance r_{out}. After this, we will calculate the voltage gain.

Let us first calculate i_{out} as function of v_{diff}. Fig 28 shows the test circuit.

If we let v_{out} open, no current can flow. Therefore we have to set v_{out} to 0 V for AC signals. This is illustrated with ground symbol in Fig 28. Only in this case the current that flows out of the circuit i^*_{out} is equal to the short circuit current of the Norton's current source i_{out}.

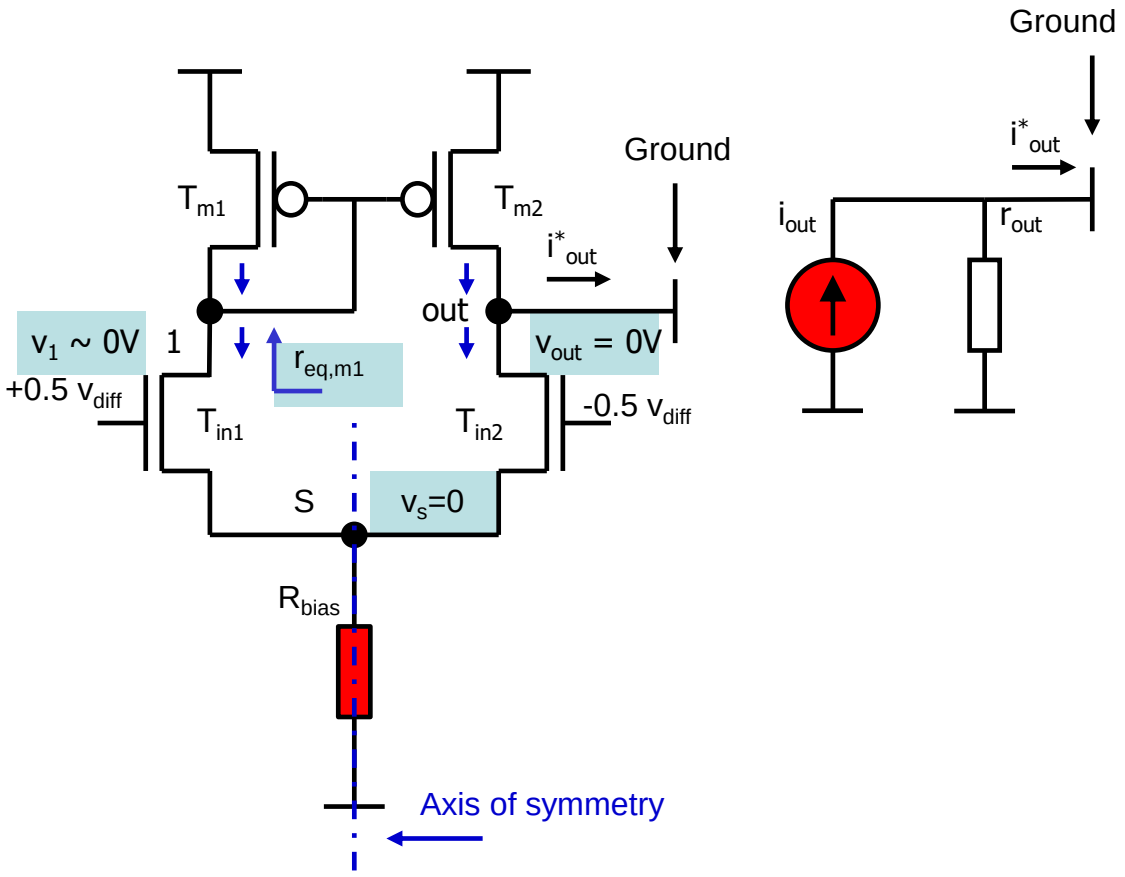


Fig 28: Small signal test circuit for the calculation of the short circuit current i_{out} as function of v_{diff}

The node out is now grounded, its potential v_{out} is equal to 0. The potential of the node 1 varies only a little, since the resistance of this node towards T_{m1} drain is small:

$$r_{eqm1} = \frac{1}{g_{m,m1}}$$

Transistor T_{in1} has a large drain resistance – a small voltage change at its drain does not influence its current. For this reason, when we can assume that the drain potential of T_{in1} is $v_1 = 0$ V. Since it is also $v_{out} = 0$, the both transistors T_{in1} and T_{in2} hate equal drain voltages. The lower half of the circuit is symmetrical (Fig 28) and the small signal voltages at the gates of T_{in1} and T_{in2} have equal absolute values and different signs. Therefore it holds for the voltage at the symmetry axis: $v_s = 0$. The currents are given by the following equations:

$$i_{ds,in1} = g_m v_{gs,in1} = g_m \frac{v_{diff}}{2} \qquad (10b)$$

$$i_{ds,in2} = g_m v_{gs,in2} = -g_m \frac{v_{diff}}{2} \qquad (10c)$$

Symbol g_m is the transconductance of T_{in1} und T_{in2}.

The current mirror copies the current: $i_{ds,m1} = i_{ds,in1}$.

The output current is:

$$i^*_{out} = i_{ds,m2} - i_{ds,in2} = i_{ds,in1} - i_{ds,in2} \qquad (10d)$$

When we substitute (10b) and (10c) in (10d), we obtain:

$$i^*_{out} = g_m \, v_{diff}$$

The short circuit current of the Norton's current source is:

$$i_{out} = i^*_{out} = g_m \, v_{diff} \qquad (17)$$

We define the differential current gain as follows:

$$G_{diff} = \frac{i_{out}}{v_{diff}} \qquad (17b)$$

with

$$G_{diff} = g_m \qquad (17c)$$

Common mode current gain

Fig 29 shows the test circuit for the calculation of i_{out} as function of v_{cm}.

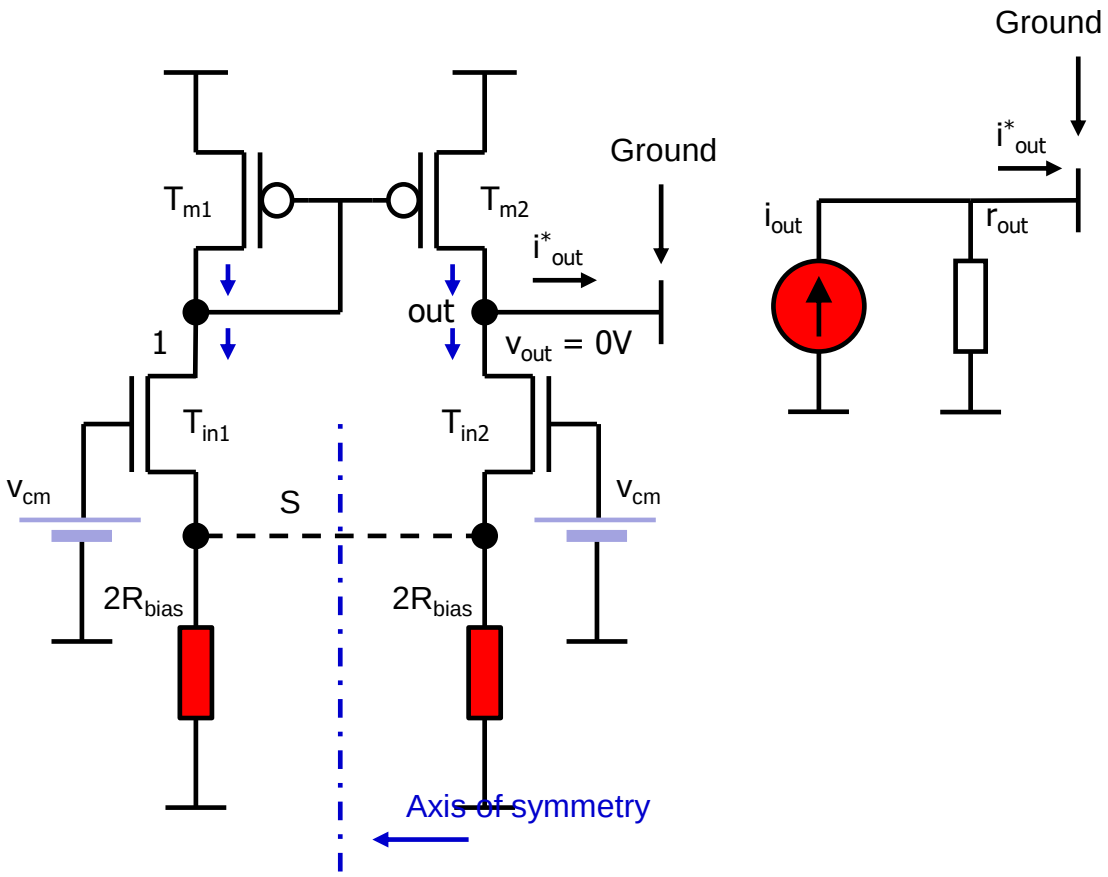


Fig 29: Small signal test circuit for the calculation of the short circuit current i_{out} as function of v_{cm}

Due to symmetry, the currents $i_{ds,in1}$ and $i_{ds,in2}$ are nearly equal. Because of (10d), it holds:

$$i^*_{out} = i_{out} = i_{ds,m2} - i_{ds,in2} \sim 0$$

The common mode current gain is:

$$G_{cm} = \frac{i_{out}}{v_{cm}} \sim 0 \qquad (17b)$$

Output resistance (optionally)

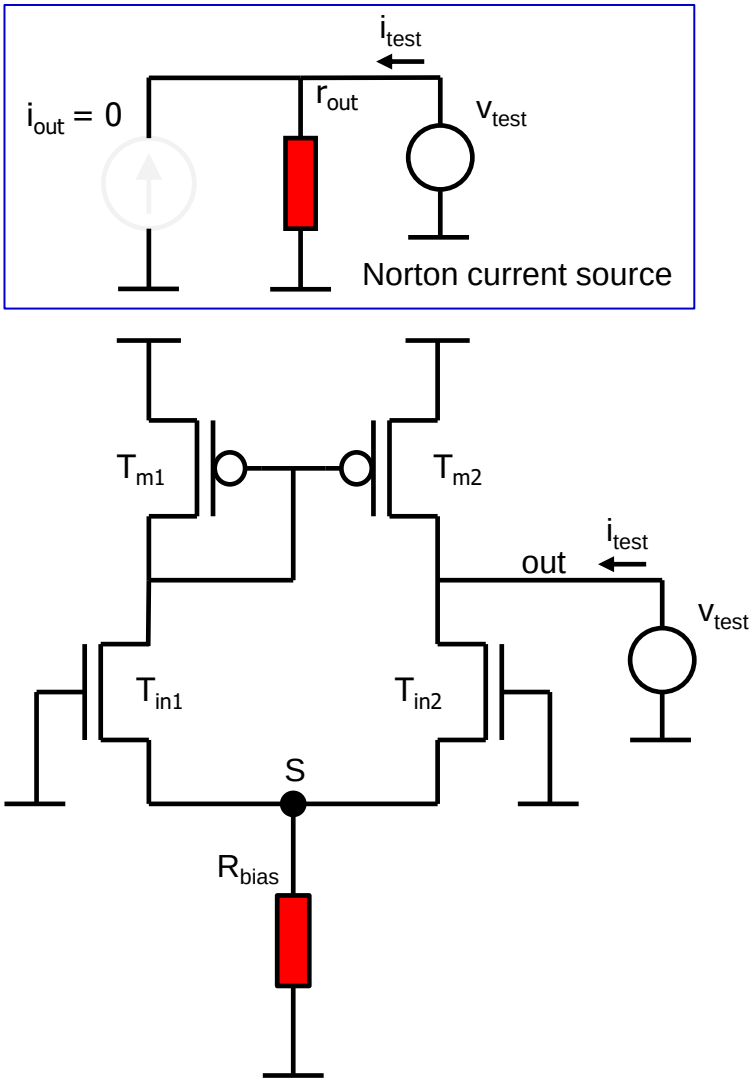


Fig 30: Small signal test circuit for the calculation of output resistance

Let us now calculate the output resistance. Fig 30 shows the test circuit. The voltage sources at the inputs of the amplifier are off ($i_{out} = 0$). The output resistance is calculated by assuming a test voltage source:

$$r_{out} = \frac{v_{test}}{i_{test}} \quad (18)$$

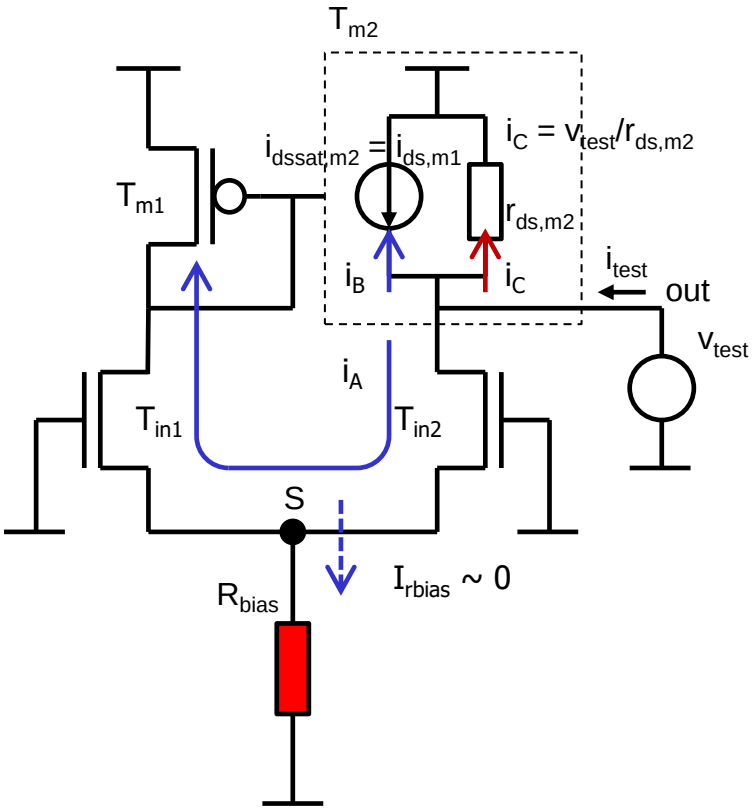


Fig 31: Small signal test circuit for the calculation of output resistance, T_{m2} is replaced with its small signal model

Fig 31 shows a more detailed schematics, where transistor T_{m2} is replaced by its small signal model. The transistor model consists of the current source $i_{dsssat,m2} = g_{m,m2}\, v_{gs,m2}$ and the resistance $r_{ds,m2}$. Since T_{m1} and T_{m2} make a current mirror, it holds:

$$i_{dssat,m2} \sim i_{ds,m1} \qquad (19)$$

The current i_{test} gets split into three currents $i_A = i_{ds,in2}$, $i_B = -\, i_{ds,m1}$ and i_C (Fig 31).

$$i_{test} = i_A + i_B + i_C \qquad (19b)$$

Let us as first calculate i_A. Transistor T_{in2} sees the following resistance at its source:

$$r_s = \frac{1}{g_{m,in1}} || R_{bias} \sim \frac{1}{g_{m,in1}} \qquad (20)$$

Notice that the current i_A splits in the node S into current through T_{in1} (r_s) and the current through R_{bias}. Since $R_{bias} >> r_s$, we can neglect the current through R_{bias}.

The circuit can be further simplified as is Fig 32.

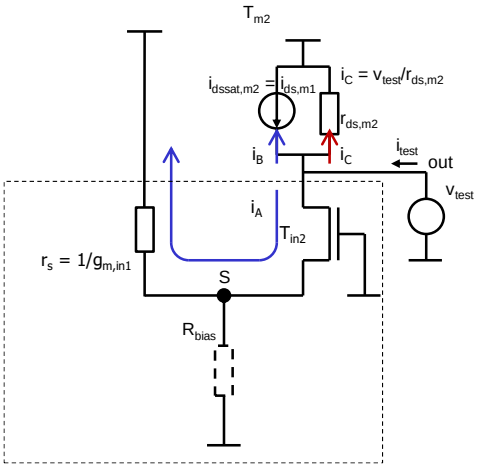


Fig 32: Simplified test circuit for the calculation of the output resistance

T_{in2} and r_s make the same circuit as V-I converter as in Fig 15. The output resistance of the V-I converter is given by (4). The resistance at the drain of T_{in2} is:

$$r_d = \left(1 + g_{m,in2}\, r_s\right) r_{ds,in2} = 2r_{ds,in2} \qquad (21)$$

We assumed $g_{min1} = g_{min2} = g_m$. The current i_A is:

$$i_A = \frac{v_{test}}{2r_{ds,in2}} \qquad (22)$$

Notice that the current i_A splits in the node S into current through T_{in1} (r_s) and the current through R_{bias}. Since $R_{bias} >> r_s$, we can neglect the current through R_{bias}.

The current i_A is copied by the current mirror. It holds:

$$i_B \sim i_A \qquad (23)$$

The current i_C is:

$$i_C = \frac{v_{test}}{r_{ds,m2}} \qquad (24)$$

We obtain the total current when we substitute (24), (22) and (23) in (19b):

$$i_{test} = \frac{v_{test}}{r_{ds,in2}} + \frac{v_{test}}{r_{ds,m2}} \qquad (26)$$

The output resistance (i.e. the internal resistance of the Norton's current source) is (Fig 33):

$$r_{out} = \frac{v_{test}}{i_{test}} = \frac{1}{\left(\frac{1}{r_{ds,in2}} + \frac{1}{r_{ds,m2}}\right)} = r_{ds,in2} \,||\, r_{ds,m2} \qquad (27)$$

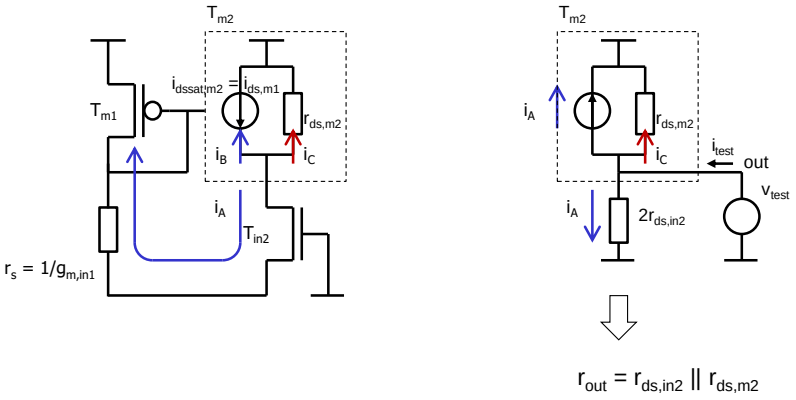


Fig 33: Simplified test circuit for the calculation of the output resistance

Voltage Gain

When we leave the output of the Norton current source open, the following voltage is generated:

$v_{out} = i_{out}\, r_{out}$. The differential voltage gain is:

$$A_{diff} = \frac{v_{out}}{v_{diff}} = r_{out}\frac{i_{out}}{v_{diff}} = r_{out}G_{diff} \quad (28)$$

Because of (17c) it holds

$$A_{diff} = g_m\, r_{out} \quad (29)$$

Because of (17b) we obtain

$$A_{cm} \sim 0 \quad (30)$$

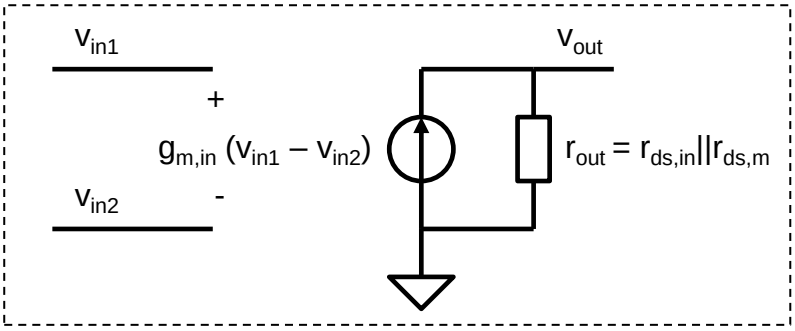
It holds:

$$CMRR = \frac{A_{diff}}{A_{cm}} \sim \infty \quad (31)$$

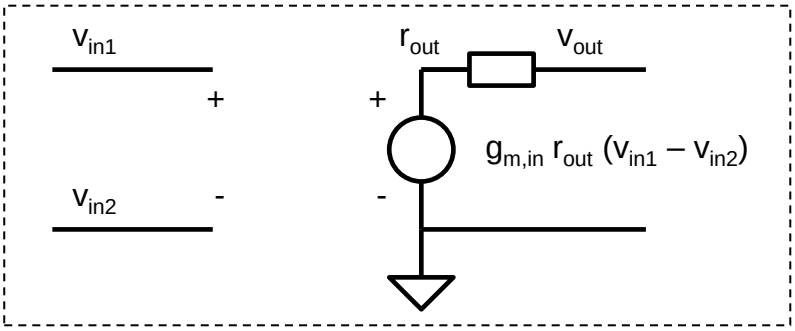
The differential amplifier with current mirror has a good CMRR. It is much better that the CMRR of the simple operational amplifier (16). Also the voltage gain (29) is assuming the same r_{out} better than (14).

The operational amplifier with a current mirror is commonly used. It has the same voltage gain as a single-ended common-source amplifier. However, the operational amplifier is more flexible in applications, since either positive or negative gain can be obtained by swapping the input pins, and because the input pins are electrically isolated from the output.

The small-signal models of the operational amplifier with a current mirror are shown in Fig 34. We assume $A_{cm} = 0$, meaning that the output current (and thus the output voltage) depends only on the difference between the input voltages.



Small signal model as current source



Small signal model as voltage source

Fig 34: Small signal model of the operational amplifier