## Lecture 8

### Themes

Optimization of the common source amplifier

Cascode Circuit

1. Calculation of input and output resistances
2. Blackman's formula

Amplifier with cascode

3. Amplifier with a cascode
4. Amplifier with two cascodes
5. Folded cascode

Cascode as Current Receiver

### Introduction

In this lecture, we present a method for increasing the gain of an amplifier.
When is a large gain important?
To answer this question, let us consider the voltage amplifier introduced in Lecture 6 as an example.

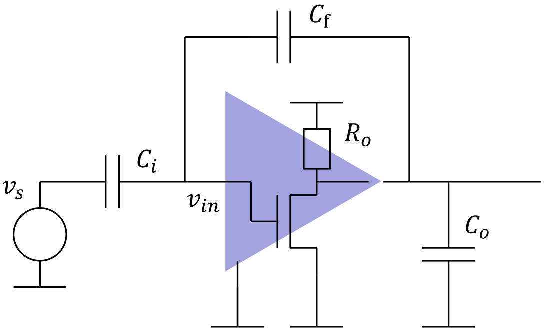


*Figure 1: Voltage amplifier*

The voltage amplification can be described with the following formula:

$$A_{fb} = -\frac{C_i}{C_f}\frac{v_s}{(sT_r+1)}$$

Factors α and β are:

$$\alpha \equiv \frac{\beta \times A}{1+\beta \times A}$$

$\beta = \frac{C_f}{C_i^{+} + C_f}$

Factor A is the open-circuit voltage gain, in the case of the common source amplifier.

$A = g_m R_{out}$

We would like to achieve a gain with feedback of -100.

$A_{fb} = 100$

We also want $A_{fb}$ to be almost entirely dependent on $C_i$ and $C_f$:

$A_{fb} \sim \frac{C_i}{C_f}$

In this case, the factor $\alpha$ must be ~ 1.

$\alpha \sim 1$

We choose the following values:

$C_i = 1\text{pF},\ C_{fb} = 10\text{fF}$

From this we calculate:

$\beta = 0.01$

For $\alpha \sim 1$, the following must apply: $A \gg \frac{1}{\beta} = 100$

As we can see, an open loop gain significantly more than 100 ($A_{fb}$) is necessary.

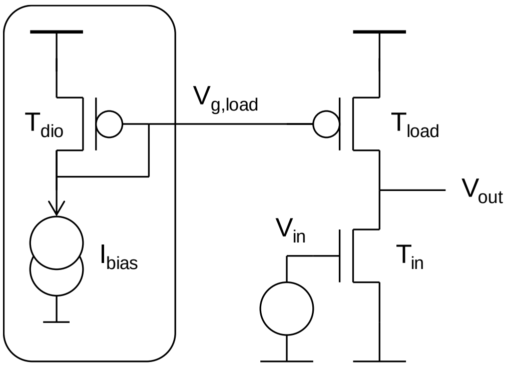


*Figure 2: Common source amplifiers with active load*

## Optimisation of the voltage gain

Let us optimize the simple common-source amplifier with an active load (Figure 2) in order to achieve the maximum possible gain and a large transconductance $g_m$. To do so, we will determine the optimal values of the following parameters: the bias current $I_{bias}$, the channel width W and length L of the input transistor Tin and the load transistor $T_{load}$.

In the following text, we will use the simplified expressions listed below.

The drain–source resistance in saturation is given by:

$$r_{ds} = \frac{LE_{sat}}{I_{dssat}} \quad (1)$$

This expression applies to strong inversion (see Lecture 3), where the saturation drain current is:

$$I_{dssat} = \frac{1}{2}\frac{W}{L}\mu C'_{ox}\left(V_{gs} - V_{th}\right)^2 \quad (2)$$

The saturation drain–source voltage is

$$V_{dssat} = V_{gs} - V_{th} = \sqrt{I\frac{L}{W}\frac{2}{\mu C'_{ox}}} \quad (3)$$

From these relations, the transconductance can be written as

$$g_m = \frac{W}{L}\mu C'_{ox}(V_{gs} - V_{th}) = \sqrt{2\mu C'_{ox}\frac{W}{L}I_{dssat}} \qquad (4)$$

or

$$g_m = 2\frac{I_{dssat}}{V_{gs}-V_{th}} = 2\frac{I_{dssat}}{V_{dssat}} \qquad (5)$$

For a 65 nm technology we have the following values:

$E_{sat}$ of PMOS ~ 10.4 V/µm and $E_{sat}$ of NMOS ~ 9.7 V/µm

µ(NMOS) = $2.64 \times 10^{-2}$ $m^2$/Vs and µ(PMOS) = $1.45 \times 10^{-2}$ $m^2$/Vs

$C'_{ox}$ = 13.28 fF/$\mu m^2$ or 0.01328f/$m^2$

$V_{th}$ ~ 0.4 V (regular $V_{th}$ transistors)

If we increase the channel length L of the input transistor $T_{in}$ while keeping all other parameters constant, the output resistance $r_{ds}$ increases according to (1), but the transconductance $g_m$ decreases according to (4). Since we do not want to reduce $g_m$, this approach is not desirable.

To increase both $g_m$ and the output resistance rout, we must scale up both the width W and the length L of the input transistor.

The disadvantage of this approach is that it increases the transistor area and its gate–source capacitance $C_{gs}$. A large input capacitance is undesirable, as it can reduce the amplification and slow down the amplifier, as discussed at the end of Lecture 6.

As a result, optimizing $T_{in}$ alone is challenging. We therefore recommend the following optimization method:

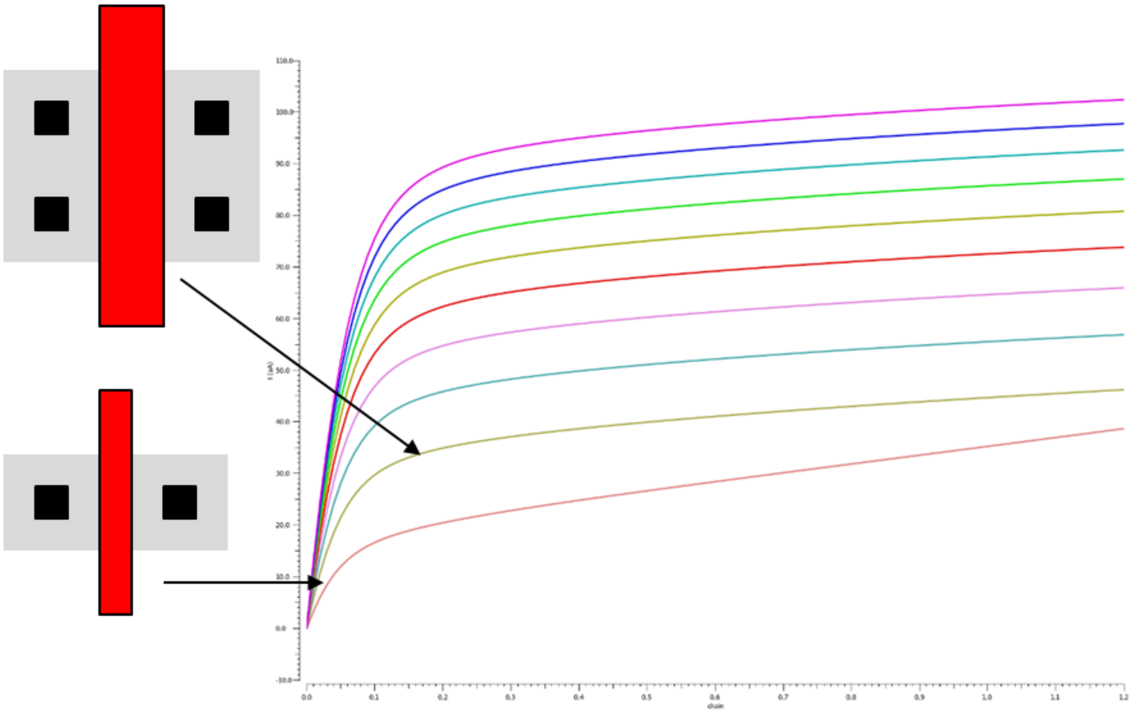
Optimisation of $T_{in}$:

We begin with the power-consumption specification and set the drain–source current $I_{DS}$ accordingly, since the static power consumption is given by $I_{ds}$ × VDD. Let us assume $I_{ds}$ = 40 µA.

Next, we select the channel length. In analog circuit design, the channel length is typically chosen to be at least three times the minimum length $L_{min}$ , because short-channel devices exhibit poor output resistance ($r_{ds}$ is small). We therefore define

$L_{in} = m \times L_{min}$ (m=3).

For a 65-nm technology $L_{min}$ = 65 nm this gives $L_{in}$ = 200 nm.



*Simulated $I_{ds}$ - $V_{ds}$ characteristics for NMOS transistors with different channel lengths L andidentical W/L ratios.*

We now set a target value for the saturation voltage.

From

$$g_m = 2\frac{I_{dssat}}{V_{gs}-V_{th}} = 2\frac{I_{dssat}}{V_{dssat}}$$

it follows that a small $V_{DS,sat}$ results in a large transconductance $g_m$, provided the transistor operates in strong inversion.

Small $V_{dssat}$ requires large W:

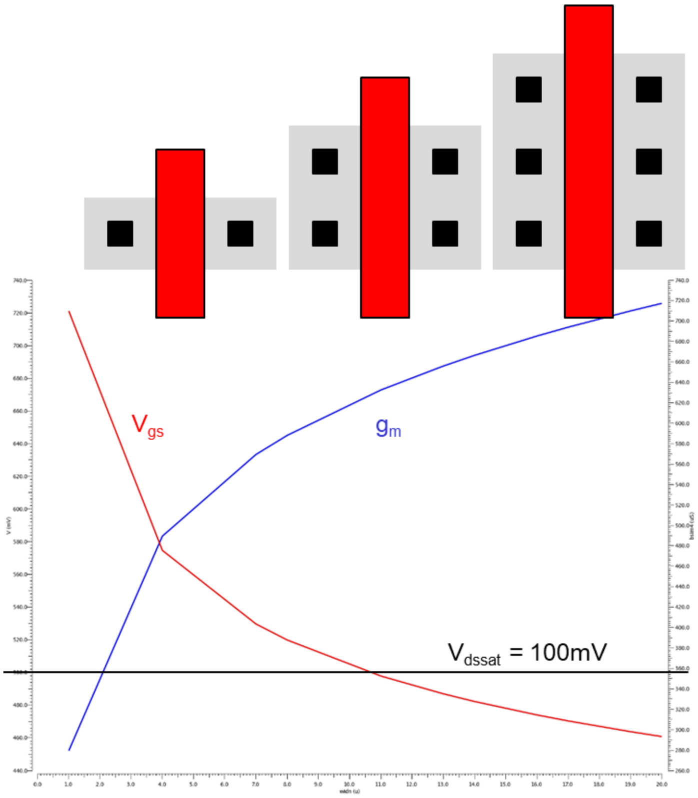
$$V_{dssat} = V_{gs} - V_{th} = \sqrt{I\frac{L}{W}\frac{2}{\mu C'_{ox}}}$$

Our goal is to obtain a large $g_m$ without making the transistor excessively large. As a compromise between transconductance, area, and capacitance, we therefore choose

$V_{DS,sat} = 100$ mV.

Notice also that the value $V_{gs} – V_{th} = 100$ mV indicates approximately the beginning of weak inversion (lecture 4). Further increase of W does not increase $g_m$.

W of the input transistor is scaled up starting from $W_{min}$ until the saturation voltage $V_{dssat}$ drops to 100 mV.



*SImulated $V_{gs}$ (blue line) and $g_m$ (red line) as functions of transistor width W.*

Optimisation of $T_{load}$

The load source $T_{load}$ is easier to optimize because its $g_m$ is not so important. (Actually, a small $g_m$ is better as it lowers noise.) We should only maximise $r_{ds}$. Therefore, we choose $L_{load}$ large.

Note, however, that by a given current, an increase of L leads to a larger $|V_{gs}|$. This follows from equation (3).

$$V_{dssat} = V_{gs} - V_{th} = \sqrt{I \frac{L}{W} \frac{2}{\mu C'_{ox}}}$$

For this reason, the saturation voltage $|V_{dssat}| = |V_{gs}| - |V_{th}|$ also increases.

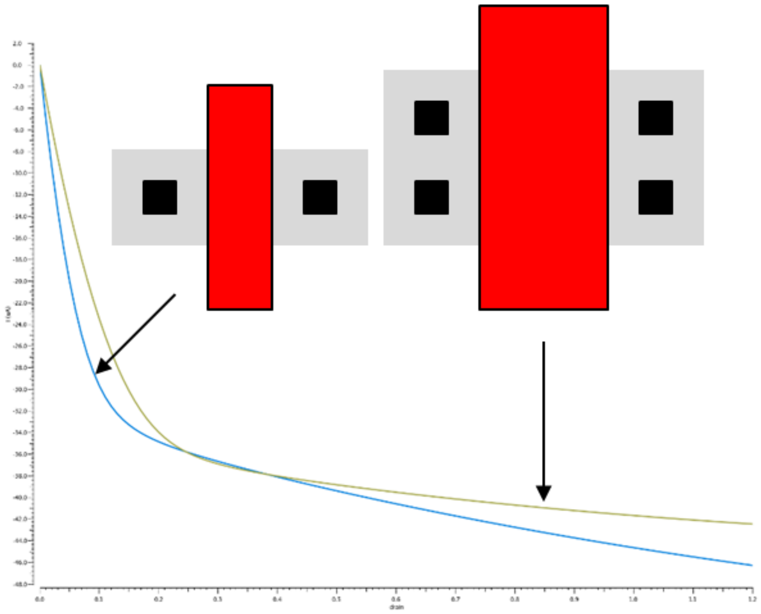
The signal range at the output, for which $T_{load}$ is in saturation, gets smaller. We can therefore proceed as follows:

First, we chose a $V_{dssat}$ that leads to acceptable signal range, e. g. $V_{dssat} = 200$ mV.

Then we choose a $L_{load}$ of about $2 \times L_{in}$.

We then scale up $W_{load}$ until we achieve $V_{dssat} = 200$ mV.

Since a PMOS transistor has about 2× smaller μ then NMOS transistor, and since $V_{dssat,load} = 2\times V_{dssat,in}$, we expect $W_{load} \sim W_{in}$.



*Simulated $I_{ds}$ - $V_{ds}$ characteristics for PMOS transistors with different channel lengths L andidentical W/L ratios.*

After such optimization we obtain $r_{ds,in} < r_{ds,load}$ because $L_{load} = 2\ L_{in}$.

Amplification is:

$$A = \ -g_{m,in}(r_{ds,in}||r_{ds,load}) \sim -\ g_{m,in}r_{ds,in}$$

Let us calculate a typical voltage gain:

It holds for strong inversion:

$$g_{m,in} = \frac{2I_{dssat}}{V_{dsssat}} = \frac{2\times 40\mu A}{0.1V} = 800\mu S$$

$$r_{ds,in} = \frac{E_{sat}L_{in}}{I_{dssat}} = \frac{\frac{9.7V}{\mu m}\ \times 200\ nm}{40\ \mu A} = 48.5\ k\Omega$$

$$A = -\frac{2I_{dssat}}{V_{dsssat}}\frac{E_{sat}L_{in}}{I_{dssat}} = -\frac{2E_{sat}L_{in}}{V_{dsssat}} = \frac{2\times\frac{9.7V}{\mu m}200\ nm}{0.1V} - 38.8$$

It is difficult to obtain a higher gain than 50 in such a way.

## Cascode

Cascode is a circuit consisting of a MOSFET (the cascode transistor $T_{casc}$) having a constant voltage at its gate and an input current source $I_{in}$ connected to the source of $T_{casc}$, as shown in Fig 3.

The word *cascode* is abbreviation from "cascaded anode". The anode is the positive electrode of the electron tube, which plays similar role as drain of a MOSFET. We will normally refer to the entire circuits made of the current source and the transistor $T_{casc}$ as the cascode. However, sometimes we will call $T_{casc}$ alone the cascode. For instance we may say that Fig 3 shows a current source with a cascode.

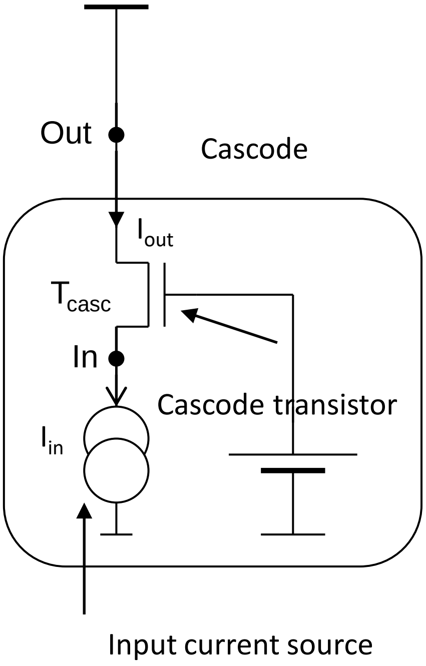


*Fig 3: Cascode*

The cascode transistor works like an impedance converter. It conducts the input current (the signal current) ($I_{out} = I_{in}$).

The AC resistance of the source of $T_{casc}$, that we also call the input resistance ($r_{in}$) of the cascode, is small. The resistance at the drain of $T_{casc}$ (the output resistance $r_{out}$) is large.

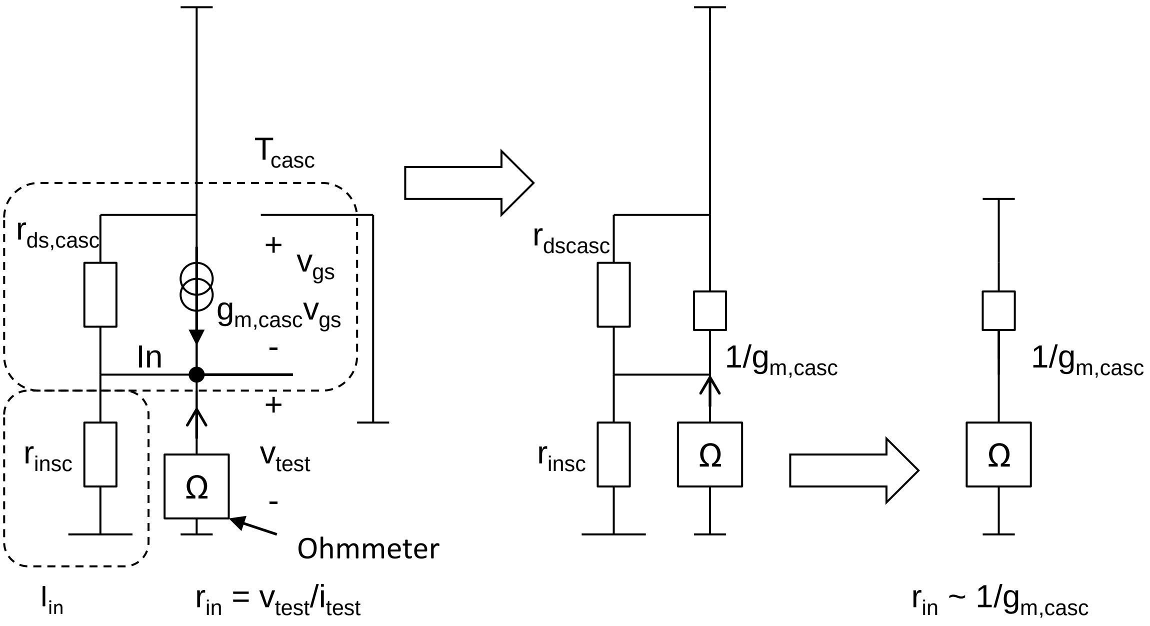


*Fig 4: Input resistance of the cascode transistor*

**Input resistance of the cascode transistor**

Fig 4 shows a test circuit for the calculation of $r_{in}$.

Let us first state the result:

$R_{in} \sim 1/g_{m,casc}$

where $g_{m,casc}$ is the transconductance of the transistor $T_{casc}$.

To derive this result, imagine an ohmmeter connected to the source of $T_{casc}$ (node In). The ohmmeter applies a small test voltage $v_{test}$ and measures the current $i_{test}$.

The applied voltage $v_{test}$ produces the following small-signal gate–source voltage for the cascode transistor:

$v_{gs} = - v_{test}$.

As a result, the controlled current source of $T_{casc}$ conducts a current

$i = g_{m,casc} \times v_{test}$.

The input resistance seen by the ohmmeter is therefore

$v_{test}/i_{test} = 1/g_{m,casc}$ (1B)

In addition to this resistance, the ohmmeter also sees the parallel combination of the drain–source resistance $r_{ds,casc}$ ($r_{ds}$ of $T_{casc}$) and the input resistance ($r_{insc}$). However these resistances are larger than $1/g_{m,casc}$ and they can be neglected.

$1/g_{m,casc}$ is relatively small —typically of the order of 1 kΩ or less. Consequently, any voltage variation at the source of $T_{casc}$ is small compared to the voltage variation at its drain. This property is fundamental to the operation of the cascode, as it helps suppress channel-length modulation and increase the output resistance.

## Output resistance of the cascode transistor

How large is the output resistance $r_{out}$?

The following figure shows the test circuit used to determine the output resistance.

### Derivation of $r_{out}$ using Kirchhoff's laws

The derivation using Kirchhoff's laws is relatively straightforward. Fig 5 shows the test circuit used to determine the output resistance with an ohmmeter.

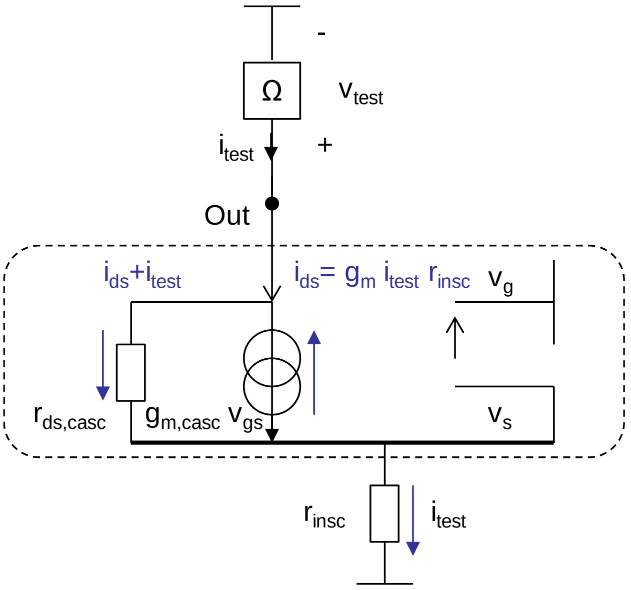


*Fig 5: Test circuit for calculation of output resistance of $T_{casc}$*

We apply a small test voltage $v_{test}$ at the output node and measure the resulting current $i_{test}$. The output node sees:

the drain–source resistance of the cascode transistor $r_{ds,casc}$,

the input resistance of the lower transistor $r_{insc}$,

and the dependent current source $g_{m,casc}\, v_{gs}$ of the cascode device.

The voltage across $r_{insc}$ is

$$v(r_{insc}) = i_{test} r_{insc}$$

Current of the dependent current source is

$$-g_{m,casc} i_{test} r_{insc}$$

Current flowing through $r_{ds,casc}$ is

$$i_{test} + g_m i_{test} r_{insc}$$

The voltage $v_{test}$ can be written as the sum of the voltage drops across $r_{insc}$ and $r_{ds,casc}$:

$$v_{test} = v(r_{insc}) + v(r_{ds,casc}) = i_{test}\, r_{insc} + r_{ds,casc}(i_{test} + g_{m,casc} i_{test} r_{insc})$$

Combining terms:

$$v_{test} = i_{test}\, (r_{insc} + r_{ds,casc} + r_{insc} g_{m,casc} r_{ds,casc})$$

Therefore, the output resistance is

$r_{out} = v_{test}/i_{test} = r_{insc} + r_{ds,casc} + r_{insc} g_{m,casc} r_{ds,casc}$ (2B)

Equation shows that the cascode structure **multiplies the output resistance**

$R_{out}$ is much larger than both $r_{ds,casc}$ and $r_{insc}$.

The large output resistance of the cascode stage can also be explained by the effect of **negative feedback**.

## Effect of negative feedback

Circuit B in Fig 6 is obtained from circuit A by replacing the cascode transistor $T_{casc}$ with its small-signal model. In this representation, the feedback mechanism becomes easier to recognize. When the ohmmeter is connected, it applies a small test voltage $v_{test}$ at the output node. As a result, an initial current $i_{test0}$ flows through the drain–source resistance $r_{ds,casc}$ and the input resistance $r_{insc}$. This current raises the source voltage $v_S$ of the cascode transistor. The increase in $v_s$ creates a **negative gate–source voltage** $v_{gs} = - v_S$. Consequently, the controlled current source of the transistor generates an AC drain current $i_{ds}$ that flows **opposite** to the direction of the original test current. This feedback-induced current partially cancels the test current supplied by the ohmmeter. As a result, the ohmmeter measures a smaller current for the same applied voltage, which corresponds to a **larger output resistance**.

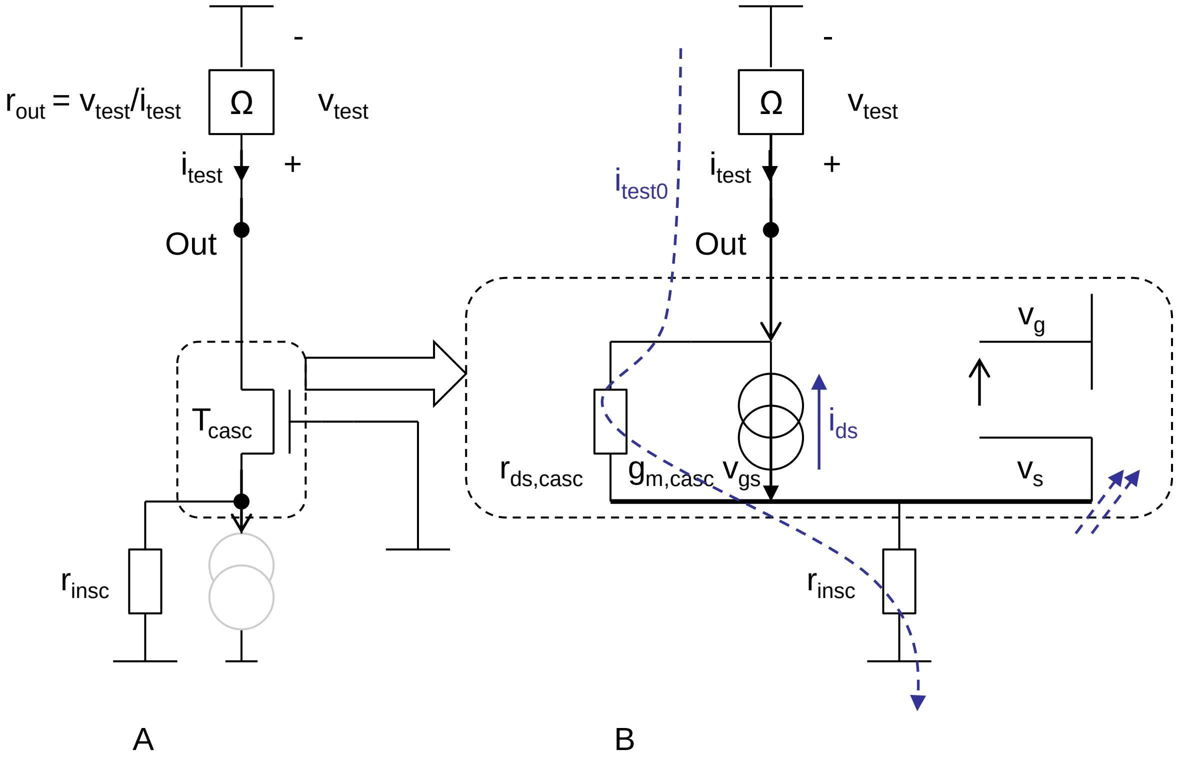


*Fig 6: Because of negative feedback, the ohmmeter measures a reduced current for a given applied voltage.*

## Summary

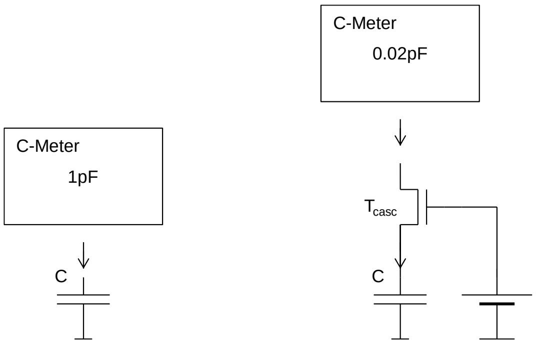
The **cascode transistor** has a **small input resistance** and a **large output resistance**.

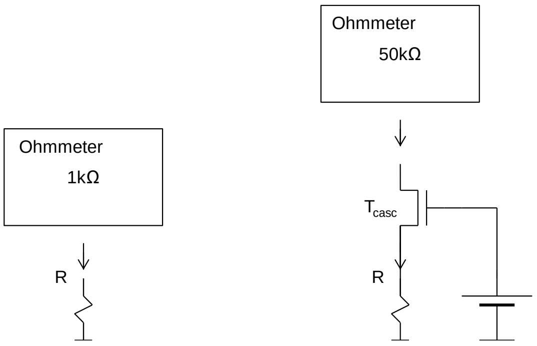
The **small-signal output resistance** is increased by the factor $g_{m,casc}\, r_{ds,casc}$ and is therefore much larger than the resistor **R** connected to the source of $T_{casc}$

The same principle applies if a **complex impedance Z** is connected to the source.

$z_{out} = Z\, g_{m,casc}\, r_{ds,casc} = Z \times a$

As a result, a **capacitance connected to the source of** $T_{casc}$ appears **significantly smaller when observed from the drain side**. This is illustrated in the two following figures:





We introduce the following symbol for the cascode: The new cascode symbol reflects a small input resistance, a large output resistance, and the fact that $I_{in} = I_{out}$.

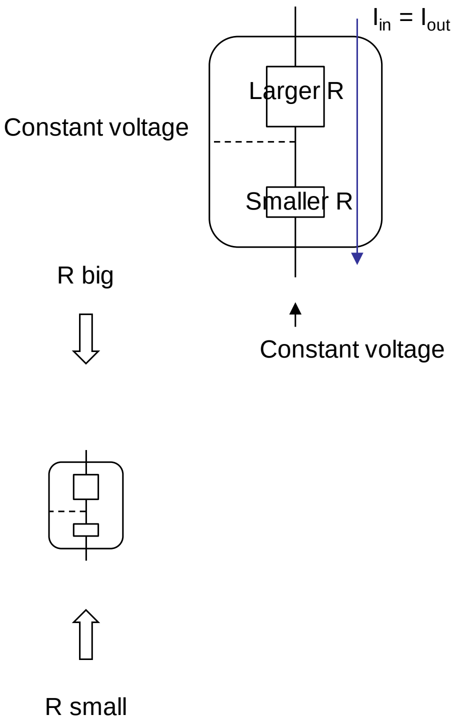


*Fig 7: The new cascode symbol reflects a small input resistance, a large output resistance, and the fact that* $I_{in} = I_{out}$.

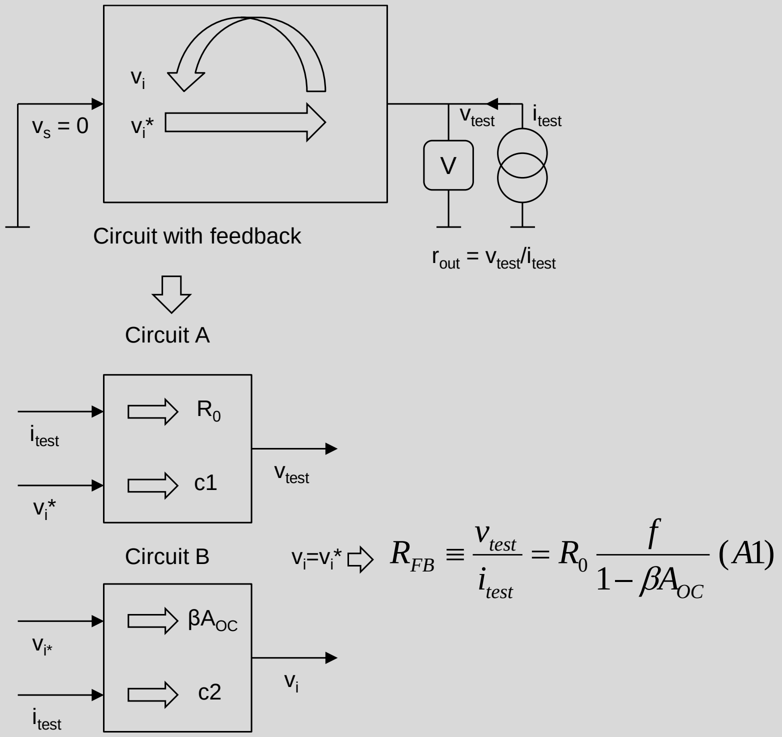
## Derivation of $r_{out}$ using Blackman's formula (optionally)

Let us calculate the output resistance $r_{out}$ using feedback analysis. As we have discussed, feedback influences the resistance of the circuit. Blackman's formula provides a method for this calculation.

### Blackman's formula

Fig 8 and Fig 9 show two test circuits for determining the output resistance with feedback, $R_{FB}$.

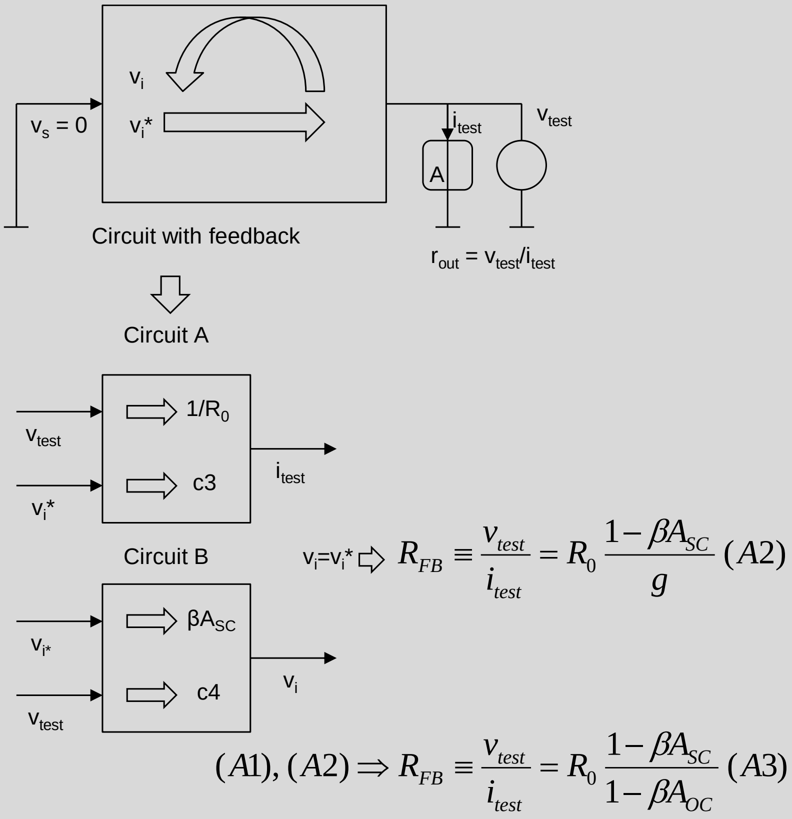
In the first circuit (Fig 8), a voltage source $v_{test}$ is applied, and the resulting current $i_{test}$ is measured (or calculated) to determine $R_{FB}$.



$$R_{FB} \equiv \frac{v_{test}}{i_{test}} = R_0 \frac{f}{1-\beta A_{OC}} \quad (A1)$$

*Fig 8: First test circuit for the derivation of $R_{FB}$. The resistance is "measured" with a current source*

In the second circuit (Fig 9), a current source $i_{test}$ is applied, and the resulting voltage is measured.



$$v_i = v_i^* \Rightarrow R_{FB} \equiv \frac{v_{test}}{i_{test}} = R_0 \frac{1-\beta A_{SC}}{g} \quad (A2)$$

$$(A1), (A2) \Rightarrow R_{FB} \equiv \frac{v_{test}}{i_{test}} = R_0 \frac{1-\beta A_{SC}}{1-\beta A_{OC}} \quad (A3)$$

*Fig 9: First test circuit for the derivation of $R_{FB}$. The resistance is "measured" with a voltage source*

In both cases, the output resistance with feedback is given by:

$R_{FB} = v_{test} / i_{test}$.

Both test circuits must yield the same value of $R_{FB}$. When the original circuit is divided into circuits A and B, and the condition $v_i = v_i^*$ is applied, formulas (A1) and (A2) can be derived, as shown in Fig 8 and Fig 9. From (A1) and (A2), formula (A3) follows (Fig 9), which is known as Blackman's formula

$$r_{outFB} = r_{out0} \frac{1-\beta A_{SC}}{1-\beta A_{OC}} \qquad (1C)$$

$r_{out0}$ is the resistance that we had if we switched off the feedback. (By setting the input voltage of the amplifier to 0.)

$\beta A_{SC}$ is the loop gain, calculated from a test circuit where the nodes are short circuited, the ohmmeter was placed between.

$\beta A_{OC}$ is the loop gain, calculated from a test circuit where the nodes are opened, the ohmmeter was placed between.

The resistance of a circuit with feedback can be calculated using Blackman's formula. The corresponding test circuit is shown in Fig 10. For this analysis, the feedback loop is opened (cut).

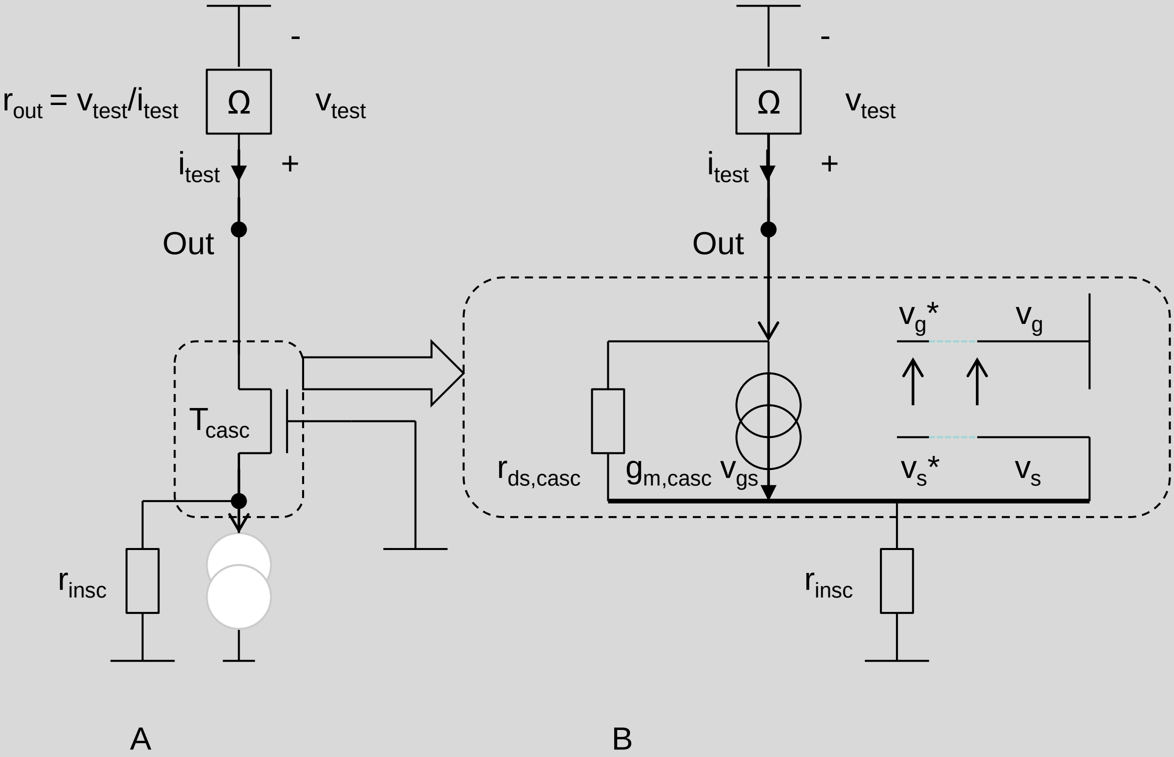


*Fig 10: Test circuit for calculation of output resistance of $T_{casc}$*

Let us calculate as first the resistance without feedback $r_{out0}$.

Fig 11 shows the test circuit.

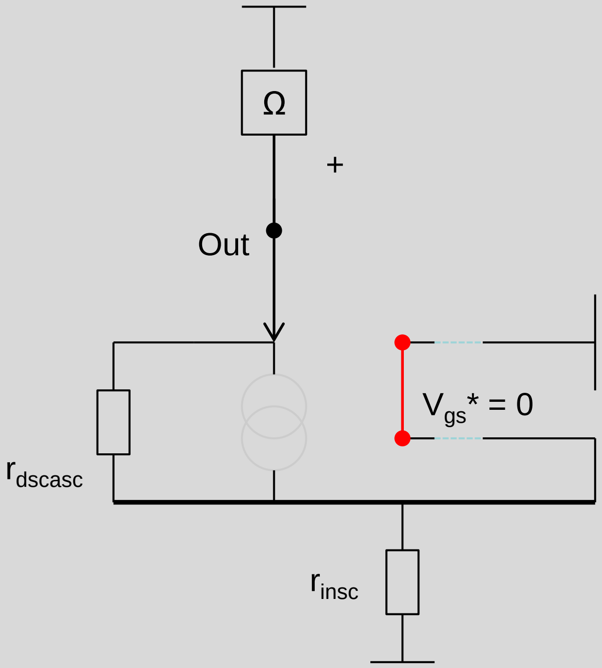


*Fig 11: Test circuit for calculation of $r_{out0}$*

The feedback is switched off by shorting $v_g$* and $v_s$*. In this way the current source in the transistor model is deactivated. The ohmmeter sees only the series combination of $r_{ds,casc}$ und $r_{sig}$:

$r_{out0} = r_{ds,casc} + r_{sig}$

Fig 12 shows the test circuit for $\beta A_{OC}$. The line where the ohmmeter was connected is now open. $A_{OC}$ is defined as follows:

$\beta A_{OC} = (v_g - v_s)/v_{test}$

Note that the current flowing into the encircled network ($i_{in}$) is zero. Therefore, the current flowing from the network to the resistance must also be zero ($i_{out}$). Therefore: $v_s = 0$. Since $v_g$ is also zero, it holds $v_g - v_s = 0$ and

$\beta A_{OC} = 0$.

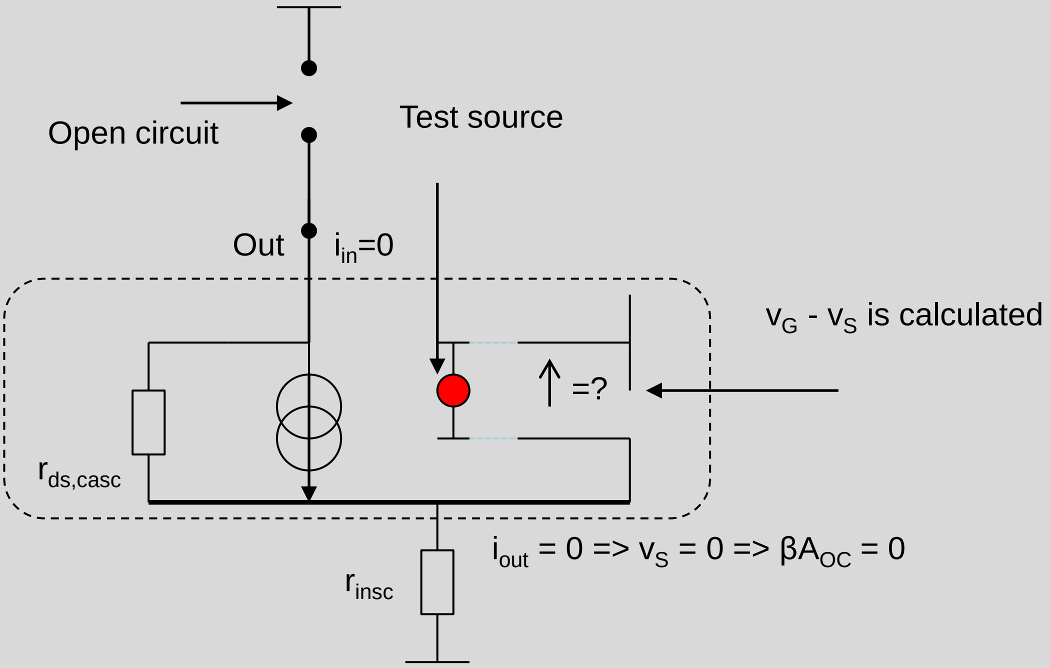


*Fig 12: Test circuit for calculation of $\beta A_{OC}$*

Fig 13 shows the test circuit for the calculation of $\beta A_{SC}$. It can be easily derived:

$$\beta A_{SC} = -\frac{r_{insc}\, r_{ds,casc}}{r_{insc} + r_{ds,casc}}\, g_{m,casc}$$

When we substitute the results for $r_{out0}$, $\beta A_{OC}$ and $\beta A_{OC}$ in the Blackman's formula (1C), we obtain:

$$r_{out} = (r_{insc} + r_{ds,casc})\left(1 + \frac{r_{insc}\, r_{ds,casc}}{r_{insc}+r_{ds,casc}}\, g_{m,casc}\right) \sim r_{insc}\, r_{ds,casc}\, g_{m,casc} \gg r_{insc} \quad (2C)$$

The product $g_m\, r_{ds}$ is in the case of the circuit from the exercises ~ 40.

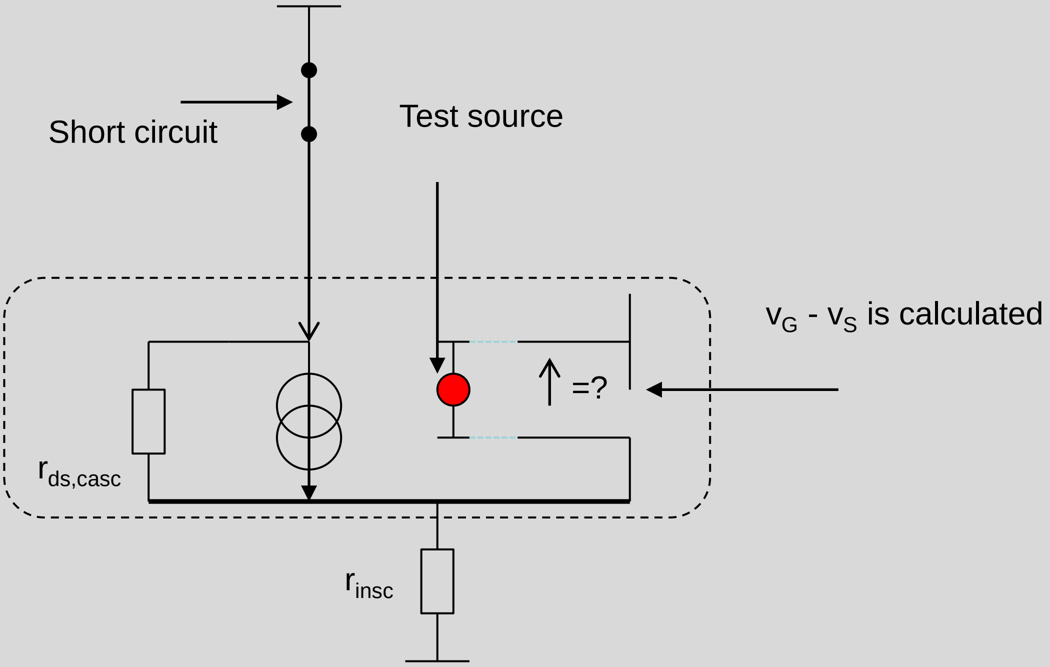


*Fig 13: Test circuit for calculation of $\beta A_{SC}$*

### Voltage amplifier with cascode

We will now show how to increase the gain of the common-source using a cascode transistor (Figure 14).

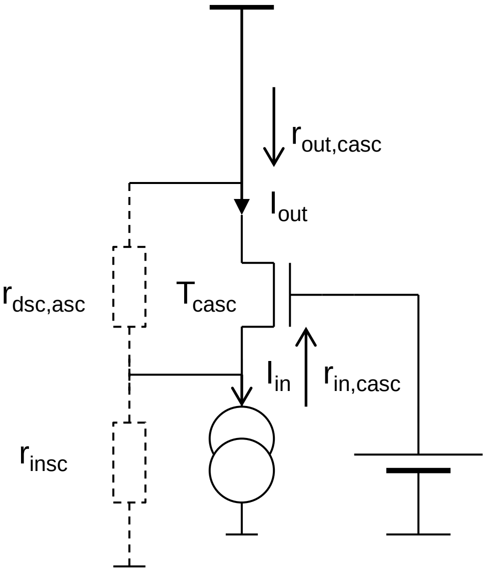


*Fig 14: Cascode transistor*

As mentioned earlier, the cascode transistor ($T_{casc}$) acts as an impedance converter, such that

$I_{out} = I_{in}$.

The input impedance $r_{in,casc}$ is small, while the output impedance $r_{out,casc}$ is large:

$r_{in,casc} = 1/g_{m,casc}$ (1D)

$r_{out,casc} = g_{m,casc} r_{ds,casc}\, r_{insc}$ (2D)

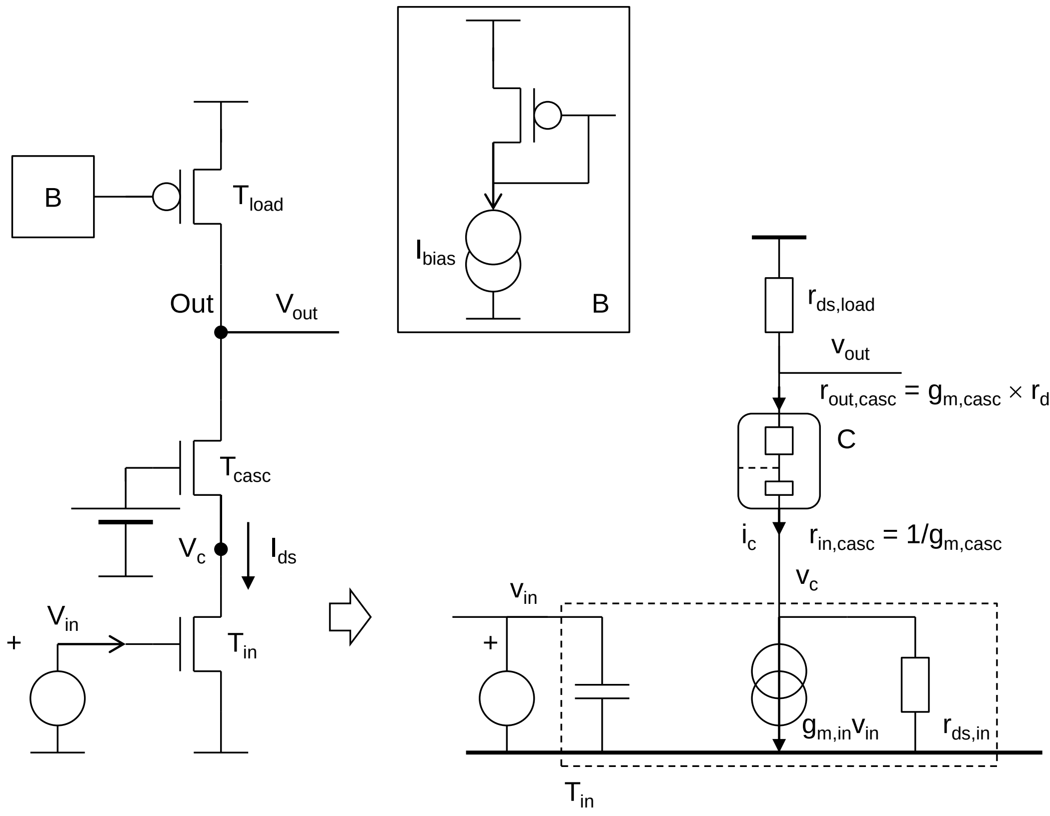


*Fig 15: Common source amplifier with cascode transistor*

Fig 15 shows the voltage amplifier with a cascode transistor (also referred to a *cascode amplifier* or an *amplifier with cascode*). The circuit now consists of three transistors connected in series: the input transistor $T_{in}$, the cascode transistor $T_{casc}$ , and the load transistor $T_{load}$ .

Fig 15 (right) shows the small-signal schematic. The small-signal current generated by $T_{in}$ flows almost entirely through $T_{casc}$ to the output node *Out*.

The current generated by the controlled current source of transistor $T_{in}$ ,

$i = g_{m,in} v_{in}$

splits to the current through $r_{dsin}$ and the current flowing through $T_{casc}$ (denoted with C in Fig 15, right).

The current through $T_{casc}$ is calculated by the current divider formula:

$$i_c = \frac{r_{ds,in}}{r_{ds,in} + r_{in,casc}} g_{m,in} v_{in}$$

Since $r_{in,casc}$ is much smaller than $r_{ds,in}$, it follows that:

$$i_c \sim g_{m,in} v_{in}$$

The current $i_c$ flows to the node Out.

The total resistance seen at node *Out*, denoted by $r_{out}$, is the parallel combination of the drain–source resistance of the load transistor $r_{ds,load}$ and the output resistance of the cascode stage $r_{out,casc}$.

The output resistance of the cascode stage is given by:

$$r_{out,casc} \sim r_{ds,in} g_{m,casc} r_{ds,casc}$$

Thus, the total output resistance becomes

$$r_{out,casc} = r_{ds,load} || r_{out,casc} = r_{ds,load} || (r_{ds,in} g_{m,casc} r_{ds,casc}) \quad (3D)$$

The voltage gain of the cascode amplifier is therefore

$$A_{casc} = -g_{m,in}\, r_{out,casc} = -g_{m,in}\, [r_{ds,load} || (r_{ds,in} g_{m,casc} r_{ds,casc})] \quad (4D)$$

Let us compare the output resistance and the voltage gain of amplifiers without and with cascode.

The output resistance without cascode was:

$$r_{out,nocasc} = r_{ds,load} || r_{ds,in} \quad (5D)$$

When we optimize the amplifier following the method we described before ($L_{load} = 2L_{in}$), we obtain

$$r_{ds,load} \sim 2\, r_{ds,in}$$

It follows:

$$r_{out,nocasc} \sim r_{ds,load} || r_{ds,in} \sim r_{ds,in} \quad (6D)$$

The voltage gain is:

$$A_{nocasc} = -r_{out,casc} g_{m,in} \sim -\, g_{m,in} r_{ds,in} \quad (7D)$$

Let us now consider the amplifier with cascode:

The product $g_{m,casc}\, r_{ds,casc}$ can be estimated using the formulas (1) und (5):

$$g_{m,casc} r_{ds,casc} = 2 \frac{I_{dssat}}{V_{dssat}} \frac{L_{casc} E_{sat}}{I_{dssat}} = 2 \frac{L_{casc} E_{sat}}{V_{dssat}}$$

Let us assume that the cascode transistor has equal dimensions as $T_{in}$: $L_{casc} = L_{in} = 200$ nm. Since the same DC current flows through $T_{casc}$ and through $T_{in}$, we obtain:

$$g_{m,casc} r_{ds,casc} = 2 \frac{L_{casc} E_{sat}}{V_{dssat}} = 2 \frac{200\ \mathrm{nm} \times 9.7 \frac{\mathrm{V}}{\mu\mathrm{m}}}{0.1} \sim 38.8$$

The output resistance with cascode is:

$r_{out,casc} = r_{ds,load}||r_{out,casc} = (2\ r_{ds,in})||(28.8 r_{ds,in}) \sim 2r_{ds,in}$ (8D)

The voltage gain with cascode is:

$A_{casc} = -\frac{r_{out} i_c}{v_{in}} \sim -r_{out,casc} g_{m,in} = 2 g_{m,in} r_{ds,in}$ (9D)

It follows from (7D) and (9D) that the voltage gain of cascode amplifier is by factor 2 larger than of the amplifier without cascode since $r_{out,casc}$ is 2 times larger than $r_{out,nocasc}$.

There are several ways to further increase the voltage gain.

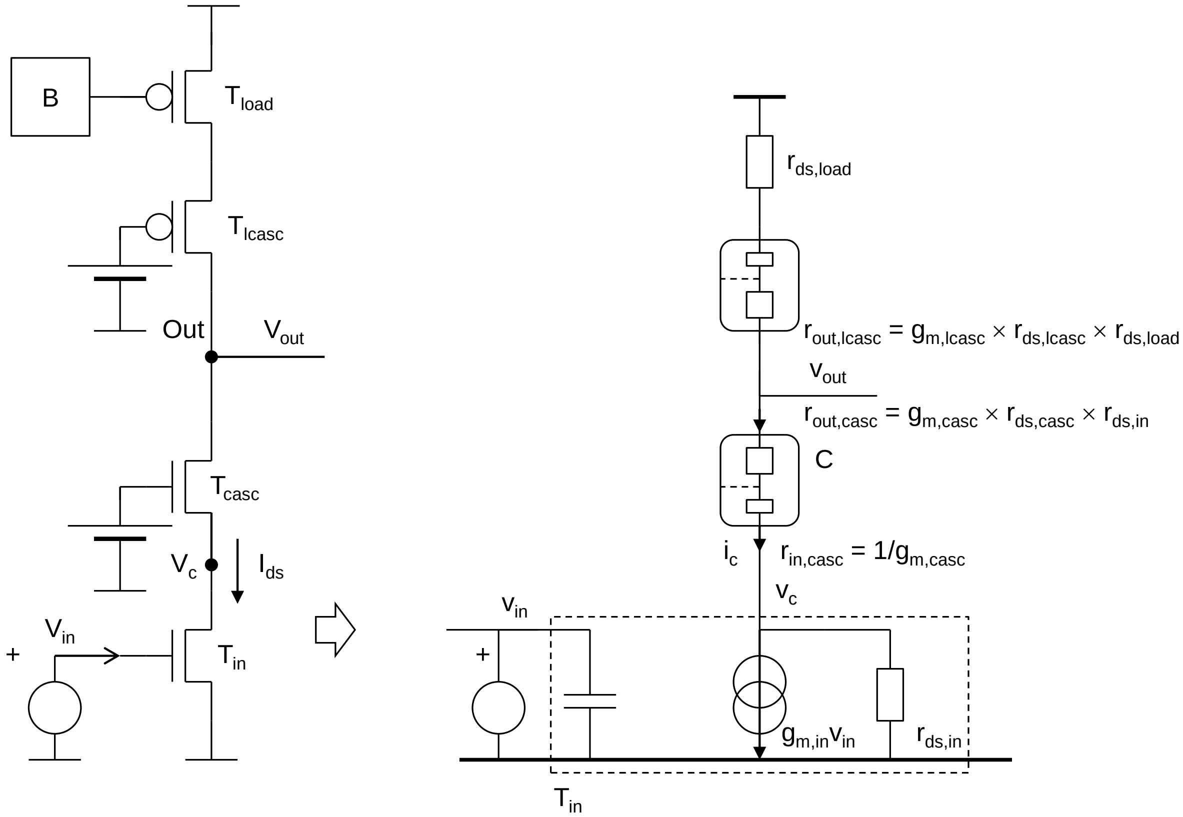


*Fig 16: Common source amplifier with double cascode*

One possibility is to add an additional PMOS cascode transistor $T_{lcasc}$ to the load current source $T_{load}$, as shown in Fig 16.

By doing so, the output resistance of the load current source is increased from $r_{ds,load}$ (the value without $T_{lcasc}$) to approximately

$$r_{ds,load}\, g_{m,lcasc}\, r_{ds,lcasc}$$

For a cascode transistor with channel length L=400 nm and saturation voltage $V_{DS,sat}$=200 mV, this corresponds to an increase of roughly

$$r_{ds,load}\, g_{m,lcasc}\, r_{ds,lcasc} \sim 42\, r_{ds,load}$$

It holds:

$$g_{m,casc} r_{ds,casc} = 2\frac{L_{casc}E_{sat}}{V_{dssat}} = 2\frac{400\ \mathrm{nm} \times 10.4\frac{\mathrm{V}}{\mu\mathrm{m}}}{0.2} \sim 41.6$$

The voltage gain is:

$$A_{doblecasc} = -g_{m,in}\left(\left(r_{ds,load} g_{m,lcasc} r_{ds,lcasc}\right) \middle\| \left(r_{ds,in} g_{m,casc} r_{ds,casc}\right)\right) \sim g_{m,in}\, r_{ds,in}\, g_{m,casc}\, r_{ds,casc} \quad (10D)$$

The voltage gain with two cascode transistors (10D) is about 20 × larger than with one transistor (9D).

## Dynamic range

An important property of amplifiers is the maximum allowable signal range at the output, which is referred to as the **dynamic range**.

It is important to note that the small-signal model is only valid when all transistors operate in the saturation region. This condition must be satisfied not only at the DC operating point, but also when signal variations are superimposed on the DC voltages.

Voltage amplifiers are often used with feedback. When using the feedback configuration described in Lecture 5 (the inverting amplifier), a *virtual ground* is present at the input of the amplifier. As a result, the input potential $v_{IN}$ remains essentially constant.

The amplified signal therefore appears primarily at the output, where the variation of $v_{OUT}$ can be large. Consequently, particular care must be taken to ensure that the output voltage swing does not become so large that it drives any transistor out of the saturation region.

This is illustrated in Fig 17.

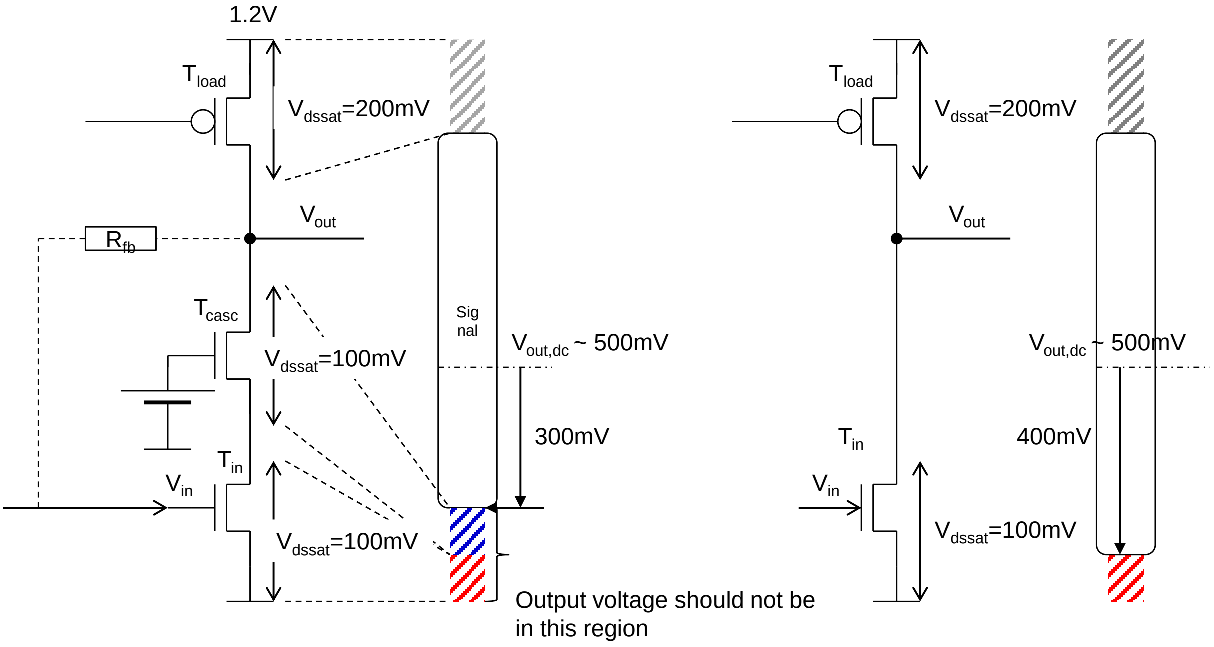


*Fig 17: Dynamic range of the amplifier with cascode (left) compared with the dynamic range of the amplifier without cascode (right)*

Let us calculate the maximum signal region at the output of the amplifier with cascode.

The potential $v_{OUT}$ must be high enough so that both transistors $T_{casc}$ and $T_{in}$ are in saturation. This means:

$$v_{OUT} > V_{dssat,in} + V_{dssat,casc} = 0.1V + 0.1V = 0.2V \qquad (1F)$$

This minimum voltage holds only when we chose the gate potential of $T_{casc}$ in the way that the source potential of $T_{casc}$ equals $V_{dssat,in}$.

The potential $v_{OUT}$ must be low enough so that $T_{load}$ is in saturation. This means:

$$v_{OUT} < VDD - V_{dssat,load} = 1.2V - 0.2V = 1.0V \quad (2F)$$

If we use the feedback as in lecture 5 (illustrated with resistance $R_{fb}$ in Fig 17), it holds $V_{in} = V_{out}$.

Therefore:

$$V_{out} = V_{in} = V_{gs,in} = V_{dssat,in} + V_{th} = 0.1V + 0.4V = 0.5V \qquad (3F)$$

The DC value $V_{out}$ is 0.5 V. The $V_{out}$ can decrease to 0.2 V (1F) and increase to 1.0 V (2F). If the signal is symmetrical around mean value, the maximum peak to peak amplitude is 0.6 V. This is shown in Fig 18.

Similar analysis can be carried out for the amplifier with double cascode, as shown in Fig 18.

The dynamic range is an important property of an analog circuit. The quality of an analog circuit is largely determined by its signal-to-noise ratio (SNR). In many cases, the signal amplitude is limited by the available dynamic range. Therefore, a larger dynamic range generally results in a higher SNR.

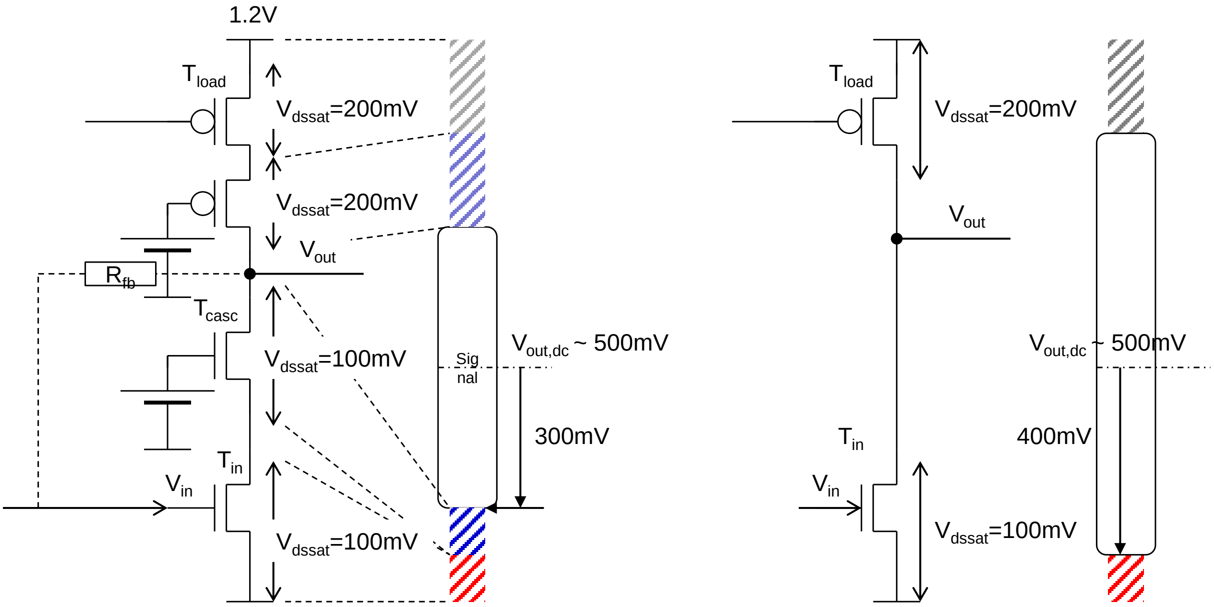


*Fig 18: Dynamic range of the amplifier with double cascode (left) compared with the dynamic range of the amplifier without cascode (right)*

### Folded cascode amplifier

A cascode transistor can also be used as a circuit for summing several currents, as shown in Fig 19. A PMOS transistor can also be used as the cascode device.

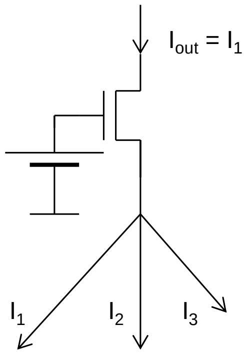


*Fig 19: Adding of currents using a cascode transtor*

Node **C** (Fig 20, right) is the source of the cascode transistor $T_{casc}$. The AC current is inverted and flows as indicated in Fig 20.

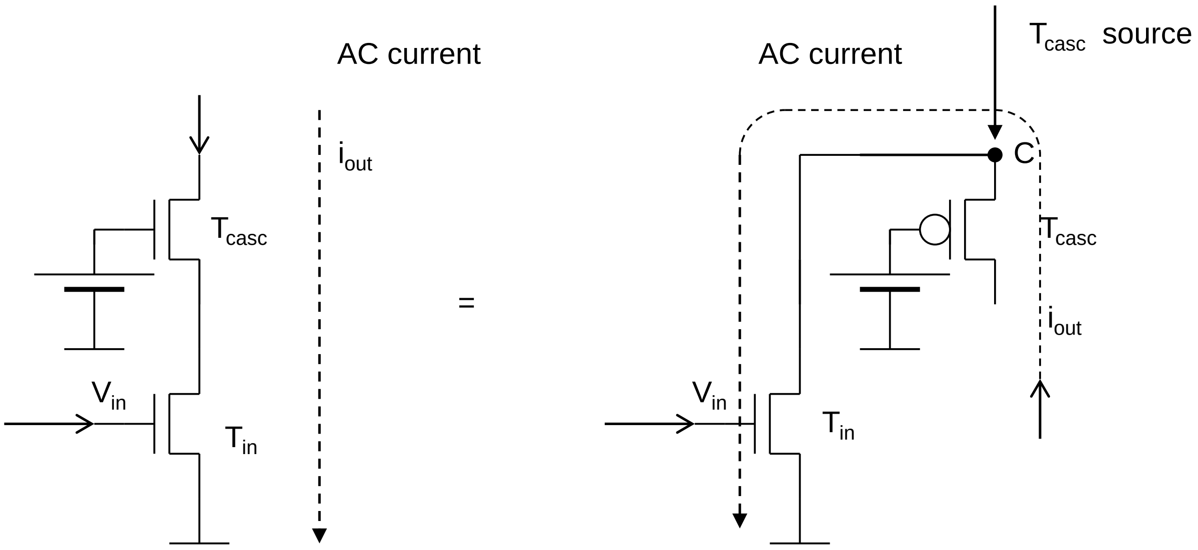


*Fig 20: Folded cascode*

To build a complete voltage amplifier, two additional components are required, as shown in Fig 21:

- A PMOS bias current source $I_{bias}$, which ensures the correct operating point of the cascode transistor $T_{casc}$.
- A resistance $R_{out}$, which converts the output current into an output voltage.

In this topology, the signal path both begins and ends at ground. In other words, when the drain–source current $I_{DS}$ of the input transistor Tin increases,

the magnitude of the current $|I_{DS}|$ flowing through the cascode transistor $T_{casc}$ decreases (see Fig 21).

For this reason, the circuit is referred to as a **folded cascode** amplifier.

In contrast, the circuits shown in Fig 15 and Fig 16 are referred to as **direct cascode** amplifiers.

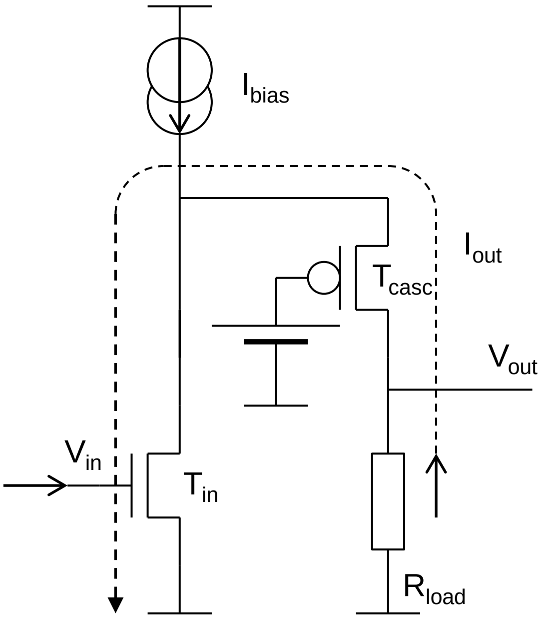


*Fig 21: Folded cascode amplifier*

We use an NMOS current source as the load element. The entire circuit is shown in Fig 22.

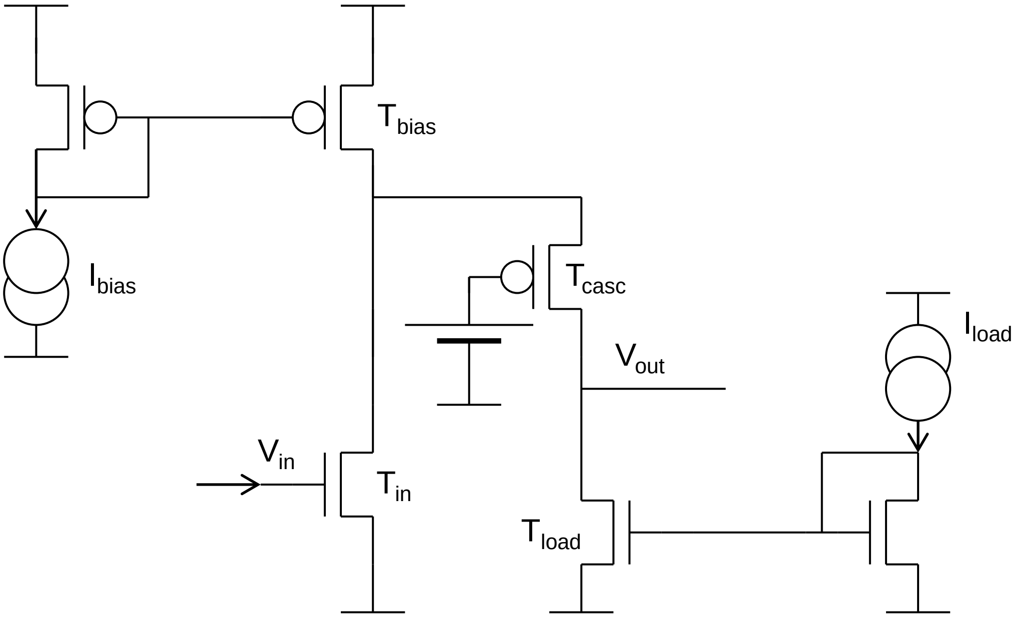


*Fig 22: Folded cascode amplifier: full schematics*

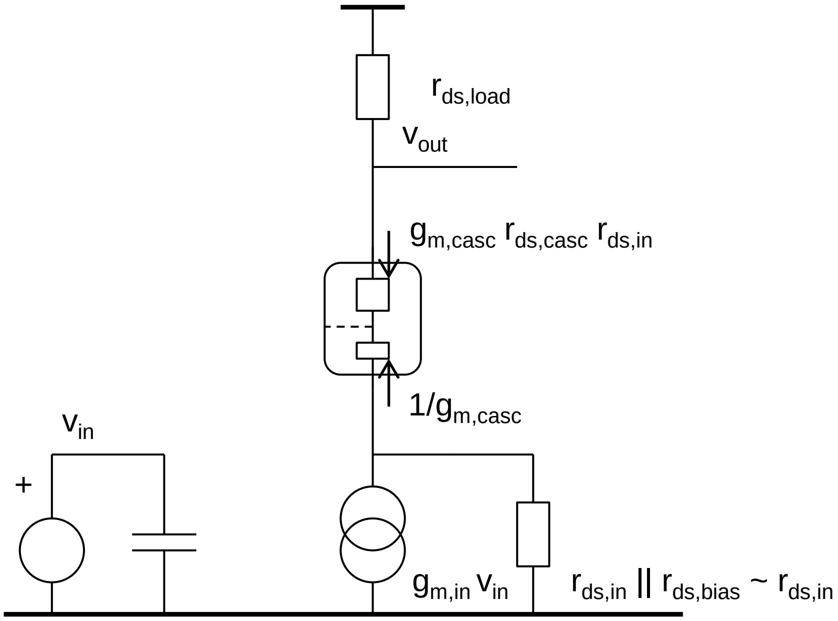


*Fig 23: Folded cascode amplifier: small signal circuit*

The small signal circuit is shown in Fig 23. We removed all constant current sources. The PMOS bias source now behaves primarily as a relatively large resistance $r_{ds,bias}$, which is in parallel with the input transistor's drain–source resistance $r_{ds,in}$. Since $r_{ds,bias} >> r_{ds,in}$, it can be neglected. The NMOS load provides a load resistance $r_{ds,load}$.

When we compare this circuit with the small-signal schematic of the direct cascode amplifier (Fig 15), we observe that the two circuits are equivalent. Therefore, parameters such as voltage gain and output resistance can be determined using the same formulas.

The voltage gain is given by:

$$A = -g_{m,in}\left(r_{ds,load}||r_{ds,casc}\, g_{m,casc}\, r_{ds,in}\right) \quad (4F)$$

Let us estimate the values of the key parameters by considering the DC currents.

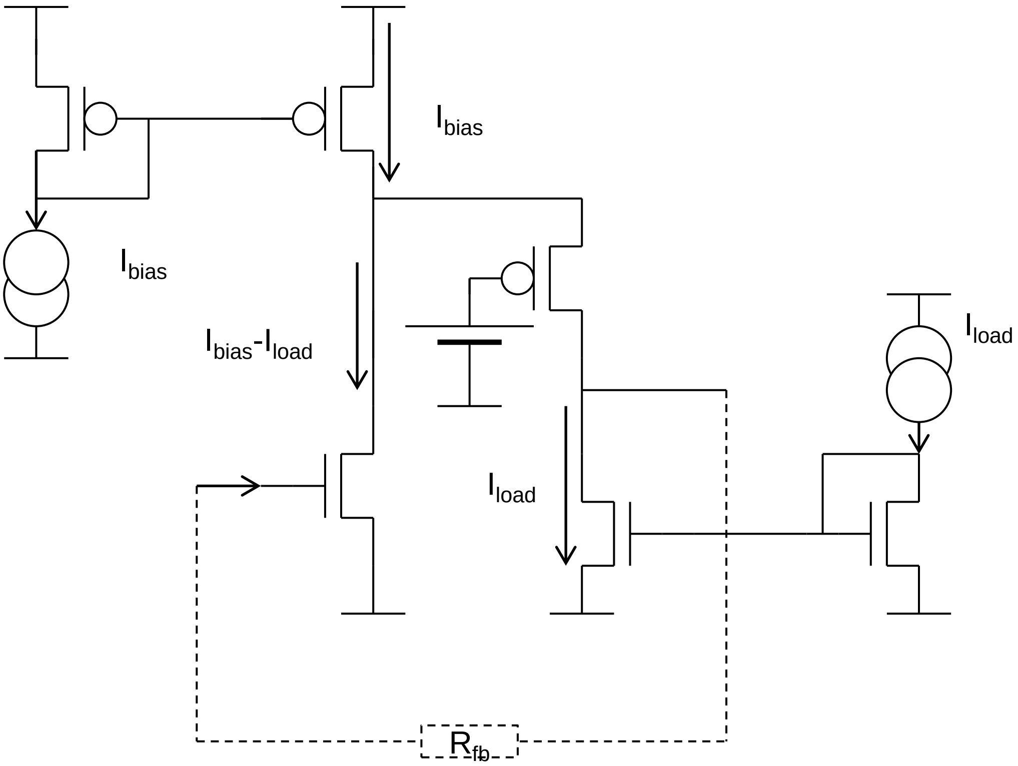


*Fig 24: Folded cascode amplifier: DC-currents*

The DC current $I_{load}$ flows through both $T_{load}$ and $T_{casc}$ (Fig 24), while the DC current $I_{bias}$ flows through the PMOS transistor $T_{bias}$. The difference, $I_{bias} - I_{load}$ flows through the input transistor $T_{in}$. Note that $I_{bias}$ must be larger than $I_{load}$, otherwise $T_{in}$ would be turned off.

To achieve a large voltage gain, we aim to maximize both the transconductance $g_{m,in}$ and the load resistance $r_{ds,load}$. For a large $g_{m,in}$, the DC current through the input transistor must be high. Conversely, to achieve a large $r_{ds,load}$ , the DC current through the load transistor should be low.

In the simple direct cascode amplifier (Fig 15), both transistors carry the same current, making it impossible to satisfy both conditions simultaneously. In the folded cascode, however, both conditions can be achieved by setting

$I_{load} << I_{bias}$.

A practical choice is

$I_{load} = 0.1\ (I_{bias} - I_{load})$

Since $I_{load}$ is ten times smaller than the bias current of $T_{in}$ the channel length of the load transistor can be chosen longer than that of the input transistor. For example, $L_{load}=2L_{in}$.

In this case, the drain–source resistance of the load transistor becomes

$r_{ds,load} = 20 \times r_{ds,in}$,

because of $r_{ds} = E_{sat}\, L / I$.

The factor $r_{ds,casc}\, g_{m,casc}$ is approximately 80 for $L_{casc}$ = 400nm and $V_{dssat,casc}$ = 100 mV:

$$\boxed{g_{m,casc} r_{ds,casc} = 2\frac{L_{casc} E_{sat}}{V_{dssat}} = 2\frac{400\text{ nm} \times 10.4\frac{\text{V}}{\mu\text{m}}}{0.1} \sim 83.2}$$

Therefore, the voltage gain of the folded cascode is

$$A = -g_{m,in}\left(r_{ds,load} \| r_{ds,casc}\, g_{m,casc}\, r_{ds,in}\right) \sim 20\, g_{m,in} r_{ds,in} \quad (23)$$

This gain is about 20 times larger than that of a common-source amplifier (gain ≈ 40), 10 times larger than the simple direct cascode amplifier and approximately equal to that of the amplifier with a double cascode.

The folded cascode is widely used because it provides both a high voltage gain and a large dynamic range that is symmetric around the DC operating point, as illustrated in Fig 25.

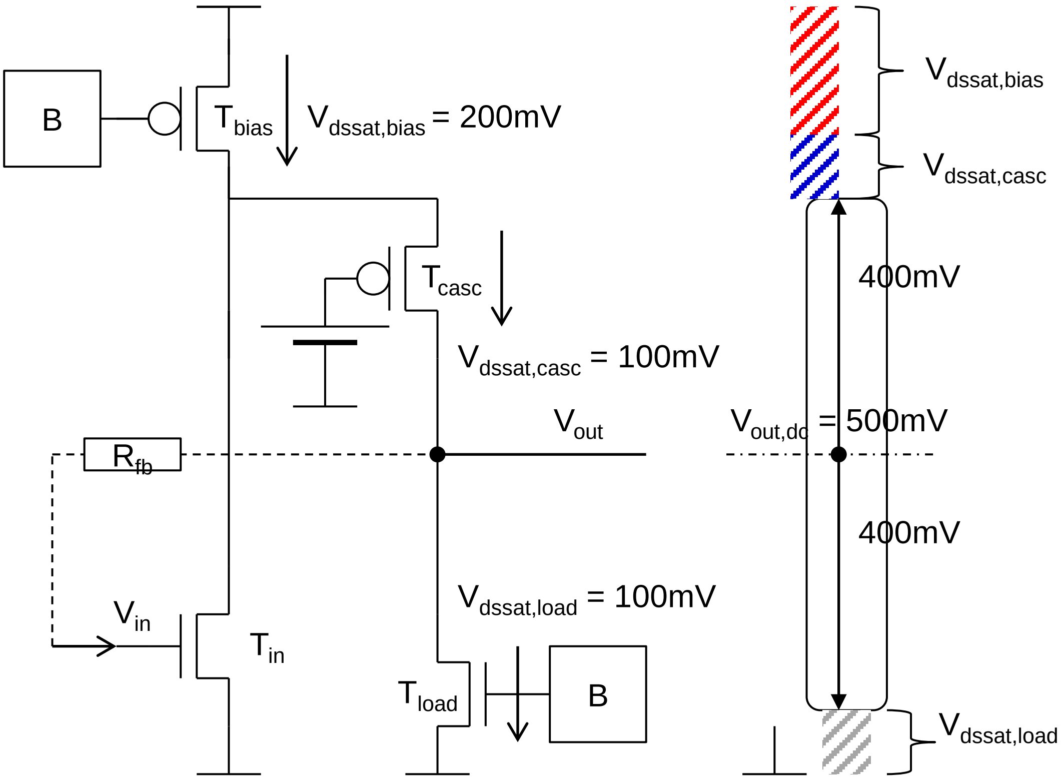
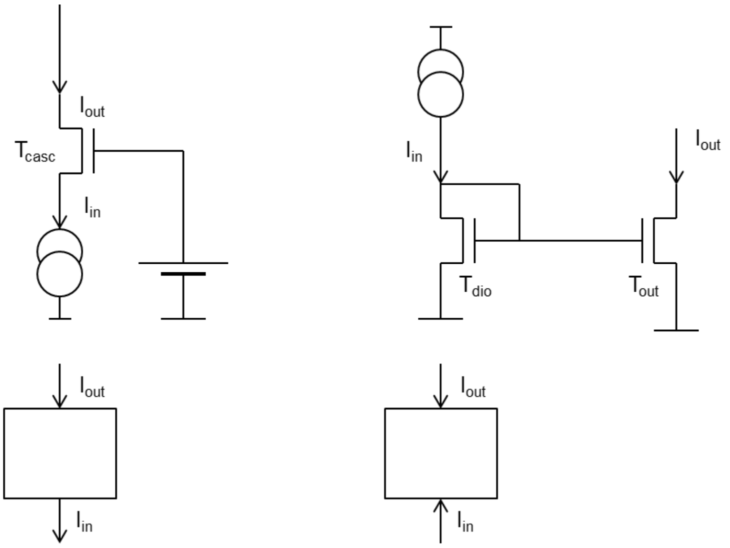


*Fig 25: Folded cascode amplifier: dynamic range*

## Comparison of Cascode Transistor and Current Mirror

The cascode transistor has a similar function like a current mirror connected to a signal source: there is a current input, a current output, $r_{in}$ is small, $r_{out}$ is large.

The main difference is that a cascode transistor change the current direction and a current mirror does not change, as shown in the figure.



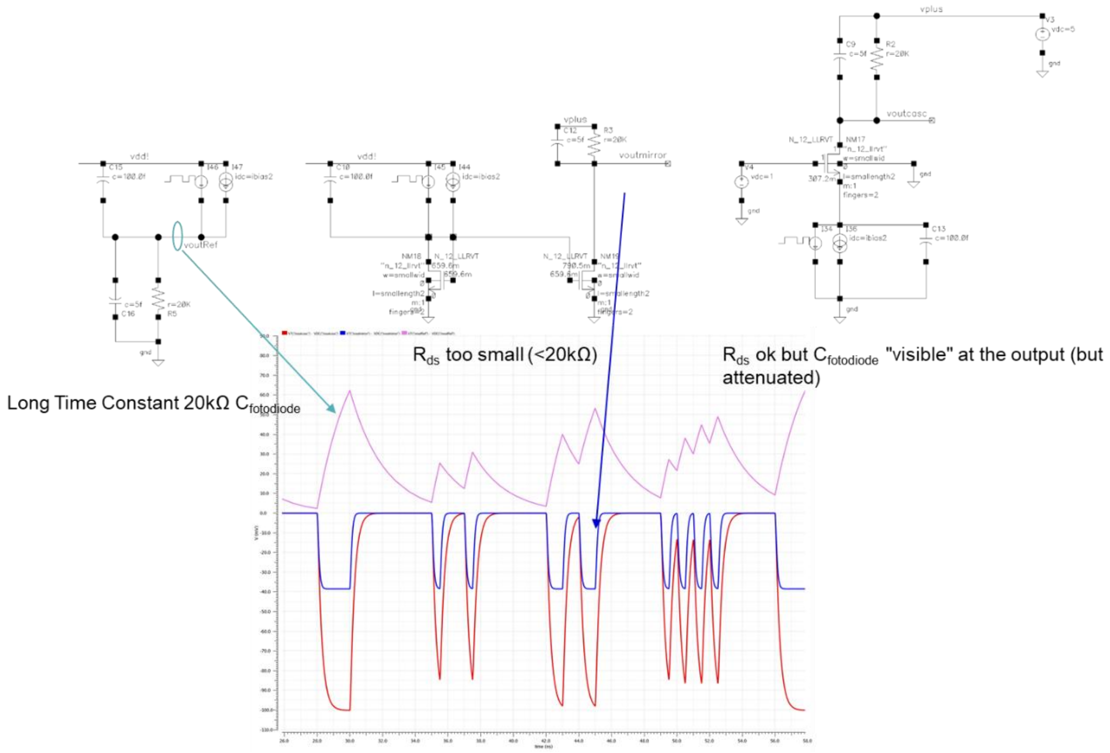
Another difference,$r_{out}$ of cascode is larger than $r_{out}$ from the current mirror

Current mirror: $r_{out} = r_{ds}$

Cascode: $r_{out} = r_{insc}\, g_{m,casc}\, r_{ds,casc}$

## Comparison of Three Photocurrent Receiver Circuits (Simulation Results)

Fig 26 shows a simulation-based comparison of **three different circuits** used to receive a photocurrent.



Long Time Constant 20kΩ $C_{fotodiode}$

$R_{ds}$ too small (<20kΩ)

$R_{ds}$ ok but $C_{fotodiode}$ "visible" at the output (but attenuated)

*Fig 26: Comparison of Three Photocurrent Receiver Circuits*

### Circuit 1:

Uses only a **20 kΩ resistor**.

*Disadvantage:* A large time constant, given by **20 kΩ · $C_{photodiode}$.**

### Circuit 2:

Introduced in **Lecture 7**, this circuit uses a **current mirror**.

*Disadvantage:* The output resistance is too small (approximately equal to **$r_{ds}$** of the output mirror transistor).

Since **$r_{ds}$< $R_{load}$= 20 kΩ**, the amplification is reduced and is **smaller than $I_{photo}$· 20 kΩ**.

**Circuit 3:**

Uses a **cascode transistor** with $\mathbf{R_{load}}$**= 20 kΩ** connected to its drain.

Since the **output resistance of the cascode** is much larger than $\mathbf{R_{load}}$ full amplification is achieved.
However, part of $\mathbf{C_{photodiode}}$ appears at the output, slightly increasing the time constant.

To conclude:

**Resistor-only circuit:** Simple, but limited by a large RC time constant.

**Current-mirror circuit:** Faster, but reduced gain due to low output resistance.

**Cascode circuit:** Achieves full gain with high output resistance, at the cost of a slightly increased time constant.