Lecture 7

Themes

- **Diode connected MOSFET**
- **Current source**
- **Current mirror**
- **Common source amplifier**

The themes of this lecture are several basic circuits, such as diode connected MOSFET, current mirror and common source amplifier.

Diode-Connected MOSFET

Figure 1 shows MOSFET diode and its U-I characteristic. The connection between the gate and the drain ensures that the transistor is in saturation (if it is in strong inversion). Therefore, the current is described by the equation for saturation current:

$$V_{ds} = V_{gs} > \frac{V_{gs} - V_{thsb}}{n} \equiv V_{dssat}$$

It follows

$$I_{ds} = I_{dssat}$$

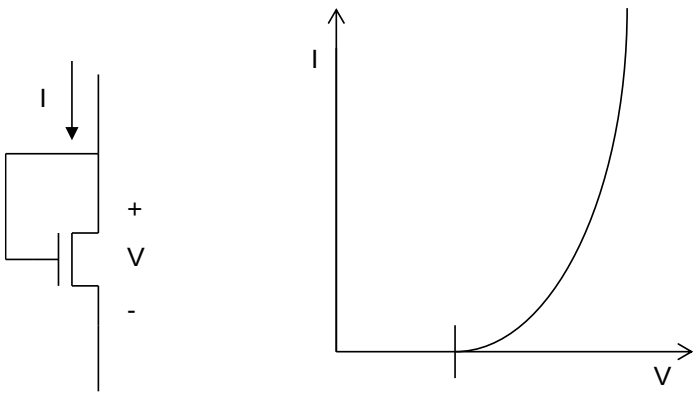

Figure 1: MOS diode and its characteristic curve

U-I Characteristics

The U-I characteristics of the MOSFET diode can be derived from the I_{ds}-equation of the transistor by substituting $V_{gs} = V_{ds} = V$:

$$I = I_{ds}(V_{gst}, V_{ds})(1 + \frac{V_{ds} - V_{dssat}}{V_A})$$

Strong Inversion

A MOSFET with its gate and drain connected is always in saturation when operating in strong inversion. The saturation condition, $V_{ds} > V_{gs} - V_{thsb}$, is inherently satisfied in this configuration. Therefore, the device exhibits the current–voltage characteristic of a diode.

$$I = I_{dsssat}(V)\left(1 + \frac{V - V_{dssat}}{V_A}\right) = k_s \frac{W}{L}(V - V_{thsb})^2\left(1 + \frac{V - V_{dssat}}{V_A}\right); k_s = \frac{\mu C'_{ox}}{2n}$$

Weak inversion

For weak inversion, $V_{gs} = V_{ds} = V$ is small and the saturation condition is not necessarily satisfied. The following equation applies:

$$I_{ds} = k_{wi} e^{(V - V_{thsb})/nU_T}\left(1 - e^{-V/U_T}\right); k_{wi} = \mu C'_{ox} U_T{}^2 (n - 1)$$

This characteristic is also diode-like.

Applications

The original application of a diode is as a rectifier. In CMOS technology, however, it is often impractical to use a PN diode. A forward-biased diode injects minority carriers, which can lead to problems such as latch-up. A MOSFET circuit that can replace the diode is shown in Fig 1 on the right. It is called diode connected transistor of MOSFET diode.

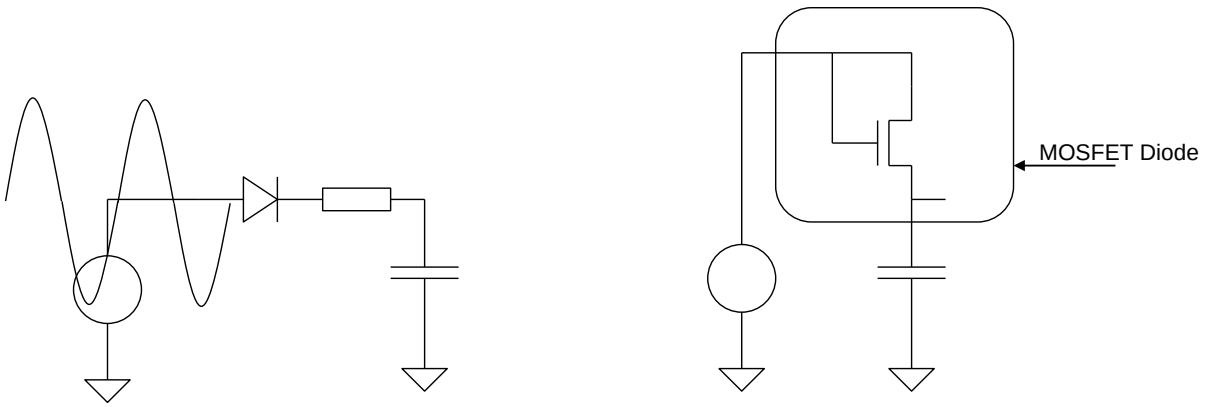

Fig 1: MOSFET diode used as a rectifier

Another application of a MOSFET diode is its use as a replacement for a resistor. In CMOS technology, resistors are implemented using polysilicon structures, and resistances greater than 1 MΩ require a very large layout area. A MOSFET diode can replace such large resistances when high linearity is not required. This is illustrated in Fig 2.

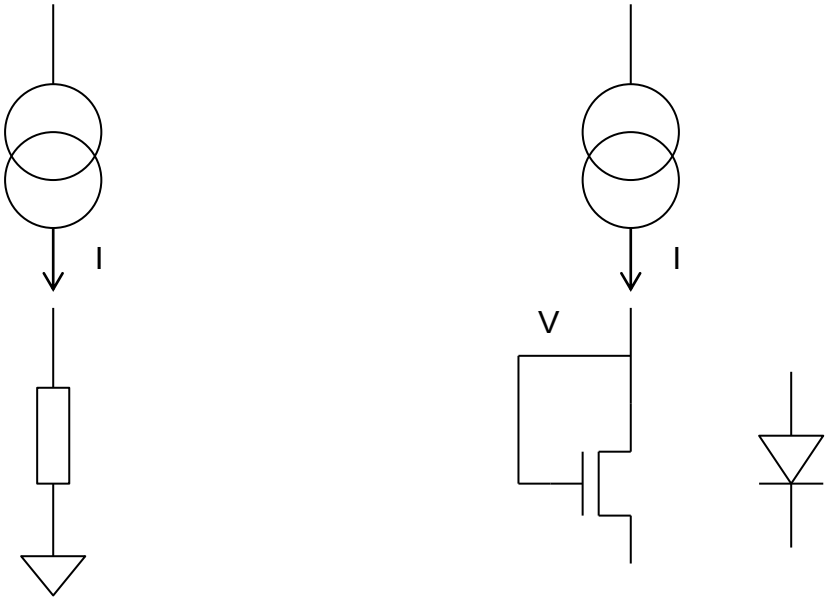

Fig 2: MOSFET diode as replacement for a resistor

MOSFET diode as resistance

Let us briefly consider the application of the MOSFET Diode as resistance. There are two variants of the circuit:

The signal current can be connected to either Drain/Gate or Source, as shown in Fig 3

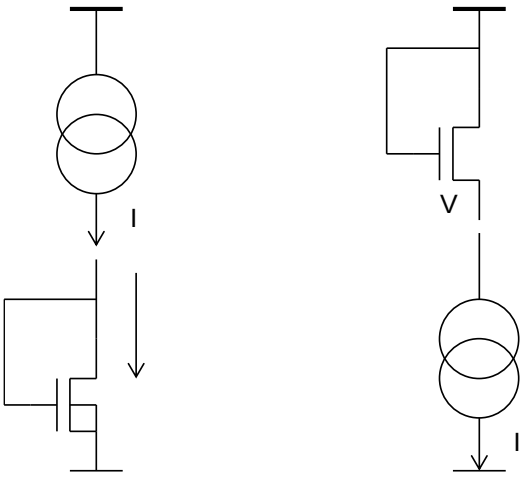

Fig 3: Two implementation of a MOSFET diode

The small-signal model of the MOSFET diode is shown in Fig 4.

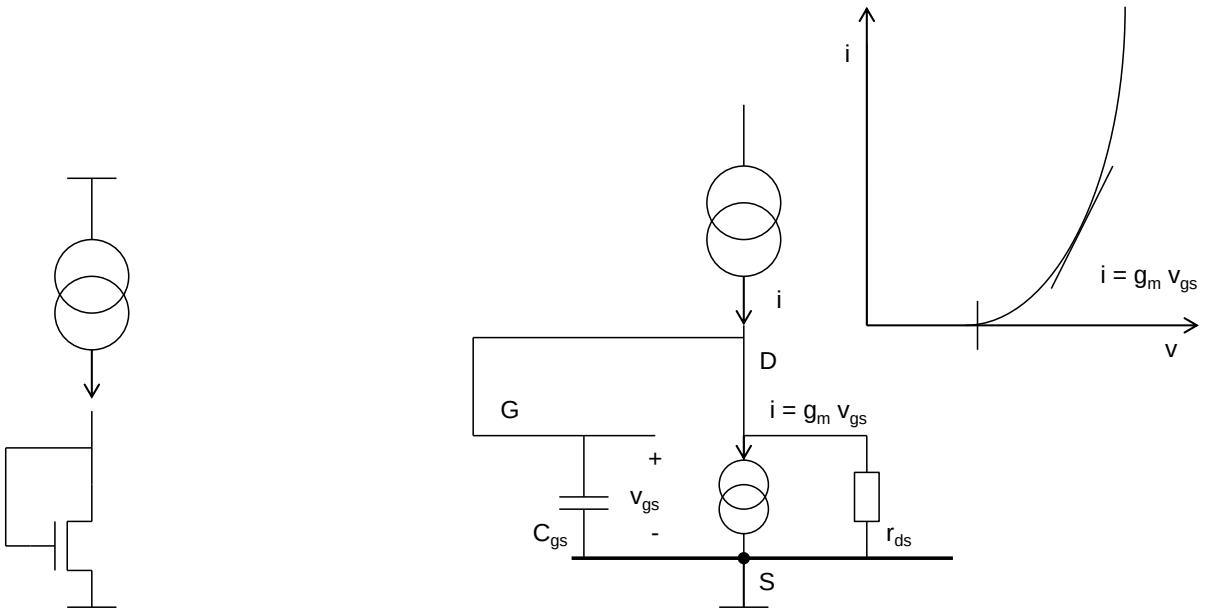

Fig 4: Small signal model of the MOSFET diode

How large is the small signal resistance of the diode connected transistor?

To calculate the small-signal resistance, imagine connecting an ohmmeter to the diode-connected MOSFET. The ohmmeter applies a voltage and measures the resulting current to determine the resistance. We consider only small changes in voltage and current (small signals). A small voltage change dv appears directly across the gate–source terminals, so the small-signal voltage is v_{gs} = dv. This produces a small-signal drain current

$i_{ds} = g_m \times dv$.

This corresponds to a resistance of $1/g_m$. There is also a current through the r_{ds} resistance that models the Early effect. The total resistance is then r_{ds} in parallel with $1/g_m$. Normally we can neglect r_{ds} since it is larger than $1/g_m$. Therefore, the small signal resistance of the diode connected transistor is:

$$r_{dio} = \frac{1}{g_m} || r_{ds} \approx \frac{1}{g_m}$$

The small signal capacitance of the diode is C_{gs} (gate-source dynamic capacitance) in parallel with C_{jd} (drain junction dynamic capacitance).

Diode connected MOSFET is a *passive* circuit. Passive means $i_{out} = 0$, if $v_{out} = 0$. i_{out} and v_{out} are the small signals. Passive circuits are described solely by their impedance.

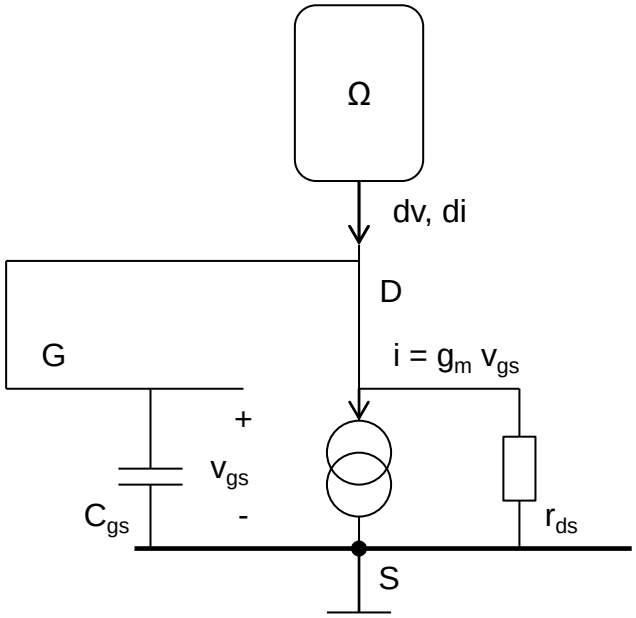

Fig 5: Small signal resistance of the MOFET diode

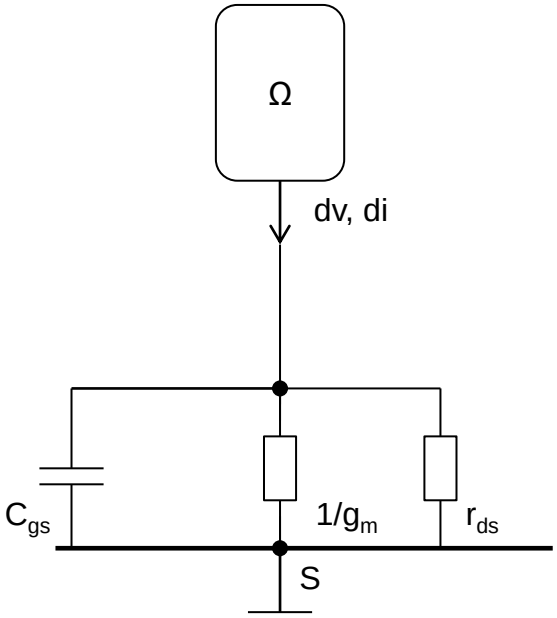

Fig 6: Equivalent circuit of the MOFET diode

Fig 7 shows several variants of the diode connected transistor.

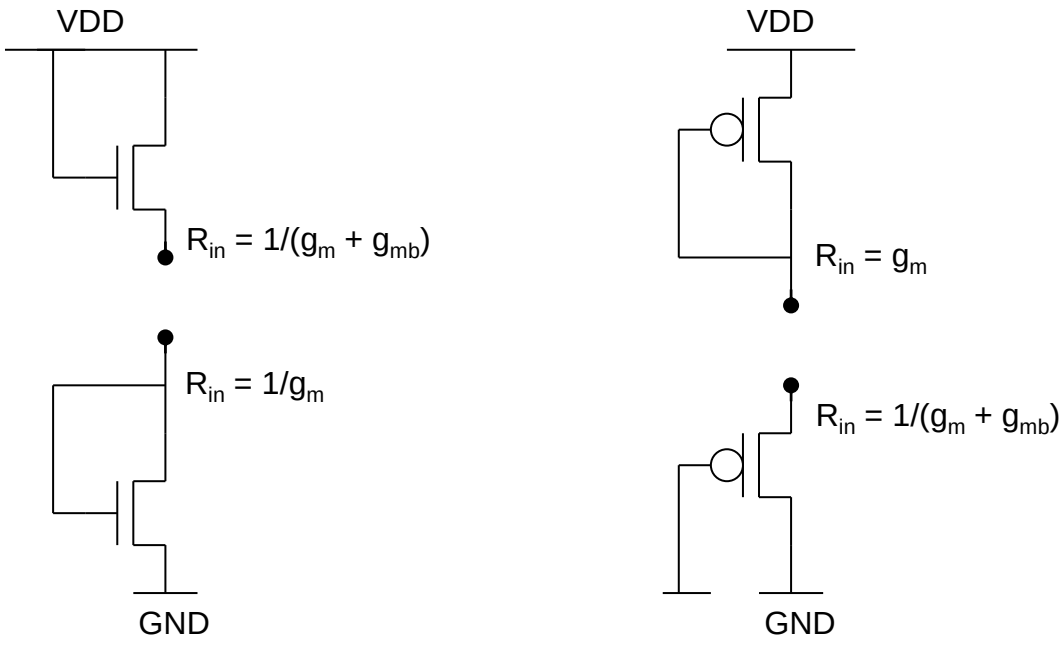

Fig 7: Input resistances of different implementations of the diode connected NMOSFET

The small-signal resistance differs slightly depending on whether the body effect is present. When the input (the node marked with a dot) is connected to the source, the small-signal input voltage dv causes changes in both v_{gs} and v_{sb}, each equal to dv. This results in a larger drain current i_{ds} compared to the case where only v_{gs} changes.

The dynamic resistance for the diodes with input at source is:

$$r_{dio} \approx \frac{1}{g_m + g_{mb}} = \frac{1}{n g_m}$$

Factor n is the slope factor of 1.25.

Current source

Another important circuit is the voltage-controlled current source (U–I converter or transconductor). There are two main applications for such a current source (Fig 8):

Application 1: Signal current source, for example as part of an amplifier. Application 2: Bias current source or constant-current generator.

The input voltage is applied to the gate of the transistor. The drain must be connected to an appropriate bias voltage to keep the transistor in saturation. The condition is: $V_{ds} > V_{dssat} = V_{gs} - V_{th}$.

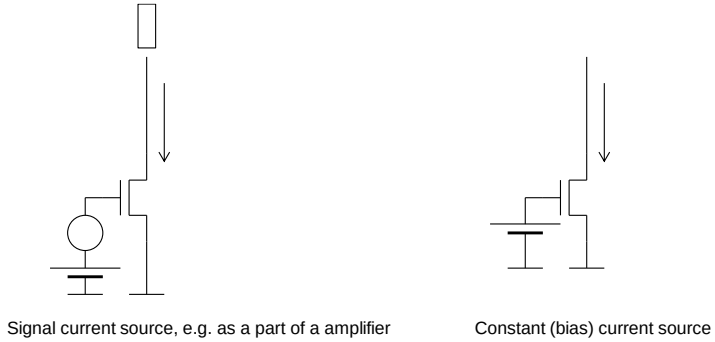

Fig 8: Two applications of the current source

We can implement current sources both using NMOS and PMOS transistors.

The source of an NMOS based current source is usually connected to ground (GND), as shown in Fig 9, right.

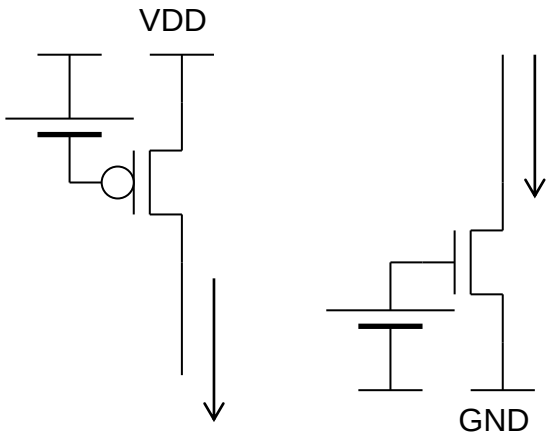

Fig 9: PMOS and NMOS variant of current source.

The source of a PMOS based current source is usually connected to positive supply voltage (VDD), as shown in Fig 9, right.

Fig 10 shows the small signal model of the current source.

The small-signal input voltage v_{in} is applied to the gate of the transistor. The drain must be connected to an appropriate bias voltage to keep the transistor in saturation (Condition $V_{ds} > V_{dssat} = V_{gs} - V_{th}$) The output resistance of the circuit is r_{ds}.

A voltage-controlled current source is an active circuit. *Active* means that, for small signals, the output current i_{out} can be non-zero even when the output voltage $v_{out} = 0$. Active circuits are characterized by their input and output impedances as well as their gain.

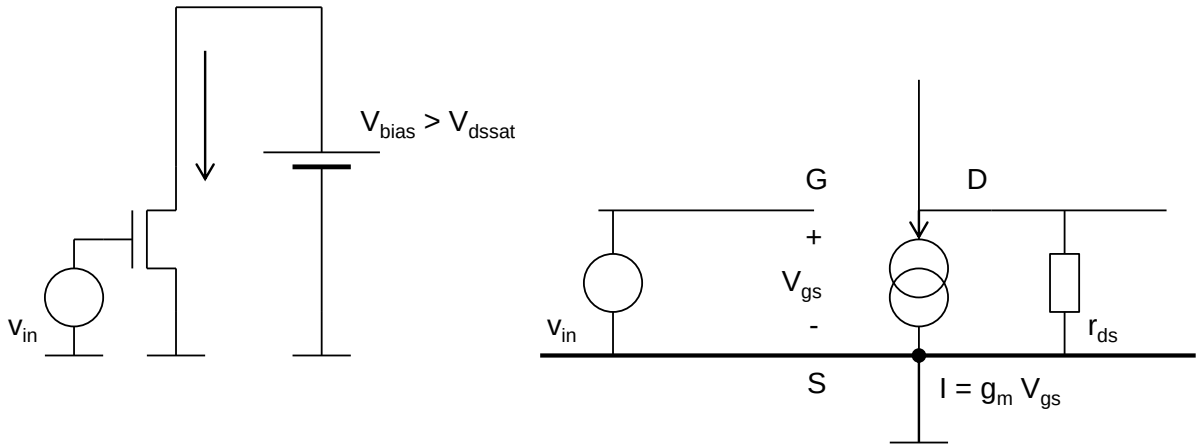

Fig 10: Current source. Small signal model is shown at the right side.

Current mirror

A current mirror is the combination of a MOSFET diode and a current source.

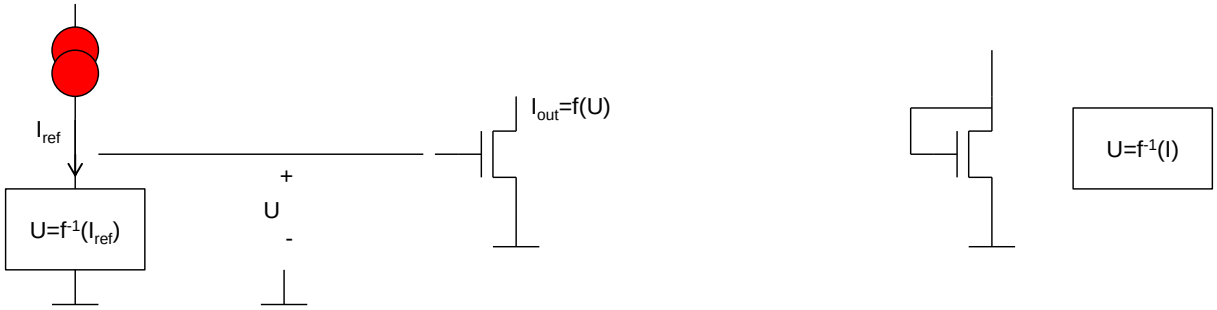

Fig 11: Current mirror uses a MOSET diode to convert input current to voltage

DC analysis in strong inversion

For diode (transistor T_{dio}) the following applies:

$$I_{in} = k_s \frac{W_{dio}}{L_{dio}} \left(V_{gsdio} - V_{th}\right)^2 \left(1 + \frac{V_{dsdio} - V_{dssat}(V_{gsdio})}{VA}\right)$$

Drain and Gate are short-circuited, therefore

$$V_{dsdio} = V_{gsdio} = V_{in}$$

The gates of T_{dio} and T_{out} are short-circuited:

$$V_{gsdio} = V_{gsout} = V_{in}$$

It also applies:

$$V_{dsout} = V_{out}$$

Let us make assumptions:

T_{out} is in saturation and Early effect does not play a role.

In this case, the equations get simplified:

For diode (transistor T_{dio}) the following applies:

$$I_{in} = k_s \frac{W_{dio}}{L_{dio}} \left(V_{gs} - V_{th}\right)^2$$

For the current source T_{out}:

$$I_{out} = k_s \frac{W_{out}}{L_{out}} \left(V_{gs} - V_{th}\right)^2$$

Therefore:

$$I_{out} = \frac{\left(\frac{W}{L}\right)_{out}}{\left(\frac{W}{L}\right)_{dio}} I_{ref} \qquad (1)$$

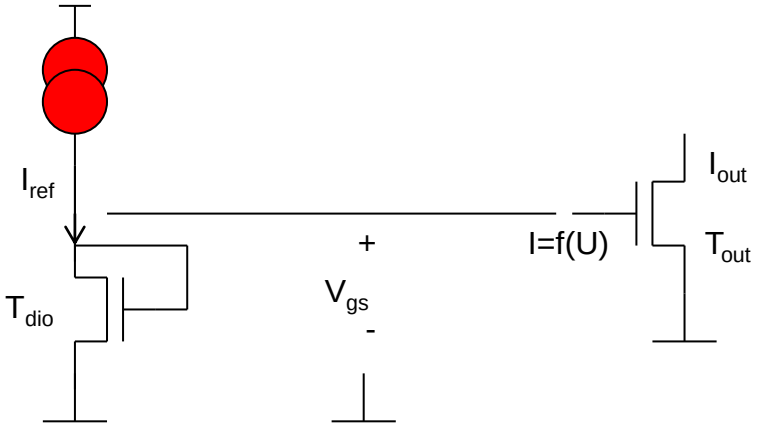

Fig 12: Current mirror

If the transistors have identical dimensions, the currents are the equal. (We are neglecting the drain source resistances)

We denote the ratio of (W/L) of the current source and the diode with "n".

Therefore

$$I_{out} = n\, I_{ref} \quad (2)$$

DC analysis in weak inversion (optional)

We will neglect Early Effect from the beginning

$$V_A \gg V_{ds} - V_{dssat}$$

For diode (transistor T_{dio}) the following applies:

$$I_{in} = k_{wi}\, e^{(V_{gsdio} - V_{th})/nU_T} \left(1 - e^{\frac{-V_{dsdio}}{U_T}}\right)$$

Drain and gate are short-circuited, therefore:

$$V_{dsdio} = V_{gsdio} = V_{in}$$

The following applies to the T_{out} current source:

$$I_{out} = k_{wi}\, e^{(V_{gsout} - V_{th})/nU_T} \left(1 - e^{\frac{-V_{dsout}}{U_T}}\right)$$

The gates of T_{dio} and T_{out} are short-circuited:

$$V_{gsdio} = V_{gsout} = V_{in}$$

It also applies:

$V_{dsout} = V_{out}$

Let us make two more assumptions:

T_{out} is in saturation ($V_{out,}\ V_{in} > 3U_T$) or $V_{in} \sim V_{out}$

In this case, the equations get simplified:

For diode (transistor T_{dio}) the following applies:

$$I_{out} = k_{wi} \frac{W_{out}}{L_{out}} e^{(V_{in} - V_{th})/nU_T}$$

For the current source T_{out}:

$$I_{in} = k_{wi} \frac{W_{dio}}{L_{dio}} e^{(V_{in} - V_{th})/nU_T}$$

Therefore:

$$I_{out} = \frac{\left(\frac{W}{L}\right)_{out}}{\left(\frac{W}{L}\right)_{dio}} I_{ref} \quad (1B)$$

Current mirror in weak inversion is usually less accurate than the current mirror in strong inversion because T_{dio} is not in saturation for small currents.

In order to get an exact integer factor n, we realize the current source (or diode) as a parallel connection of several transistors. Let us take as an example, that we want a current amplification of 2. There is here a small problem. When a transistor is designed with W = 1 µm, it has in reality the gate width by a constant dW smaller than the designed value. For example, for dW = 100 nm, the transistor with the designed value W = 1µm has the actual effective width W_{eff} = 0.9µm. This is shown in Fig 13.

Accordingly, a transistor with the designed value W = 2µm, has W_{eff} = 1.9µm. The ratio of effective widths is no longer 2, as shown in Fig 14.

Solution: We use as the current source two transistors with designed W = 1 µm and L = 1 µm in parallel and short circuit their drains, gates and sources, respectively. If the diode transistor has designed W = 1 µm and L = 1, it holds quite accurately $I_{out} = 2 \times I_{in}$. This is illustrated in Fig 15.

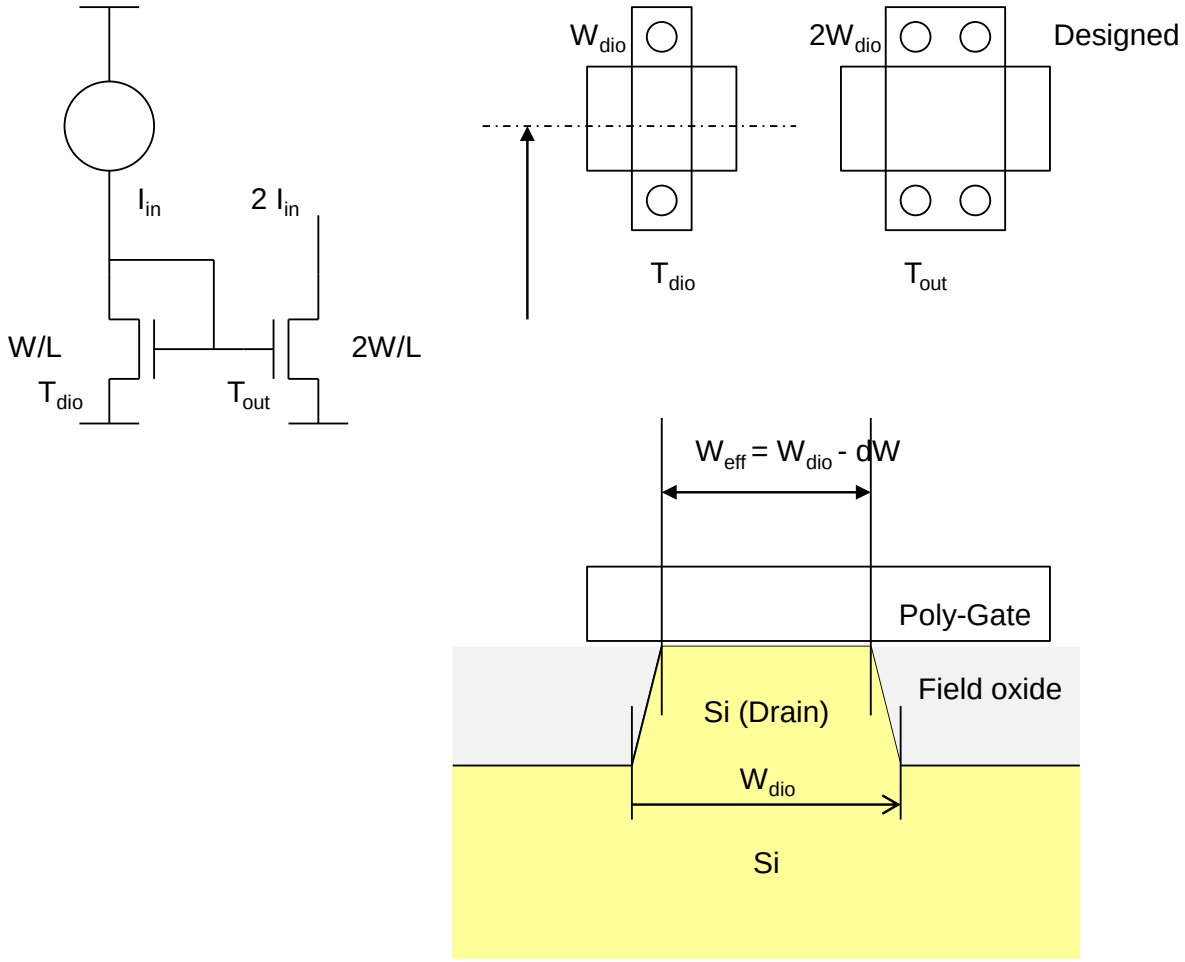

Fig 13: Accuracy of the current mirror with n = 2. Systematic error

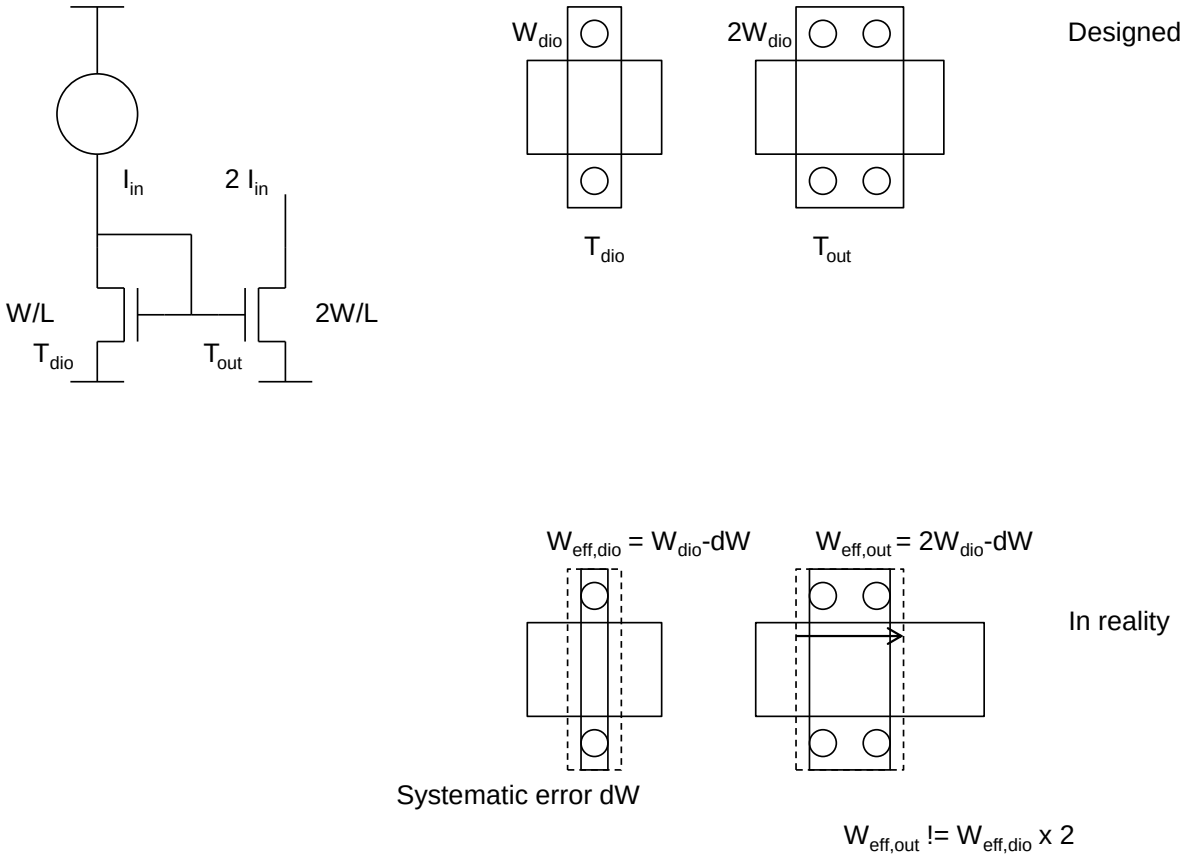

Fig 14: Accuracy of the current mirror with n = 2. T_{out} has double width

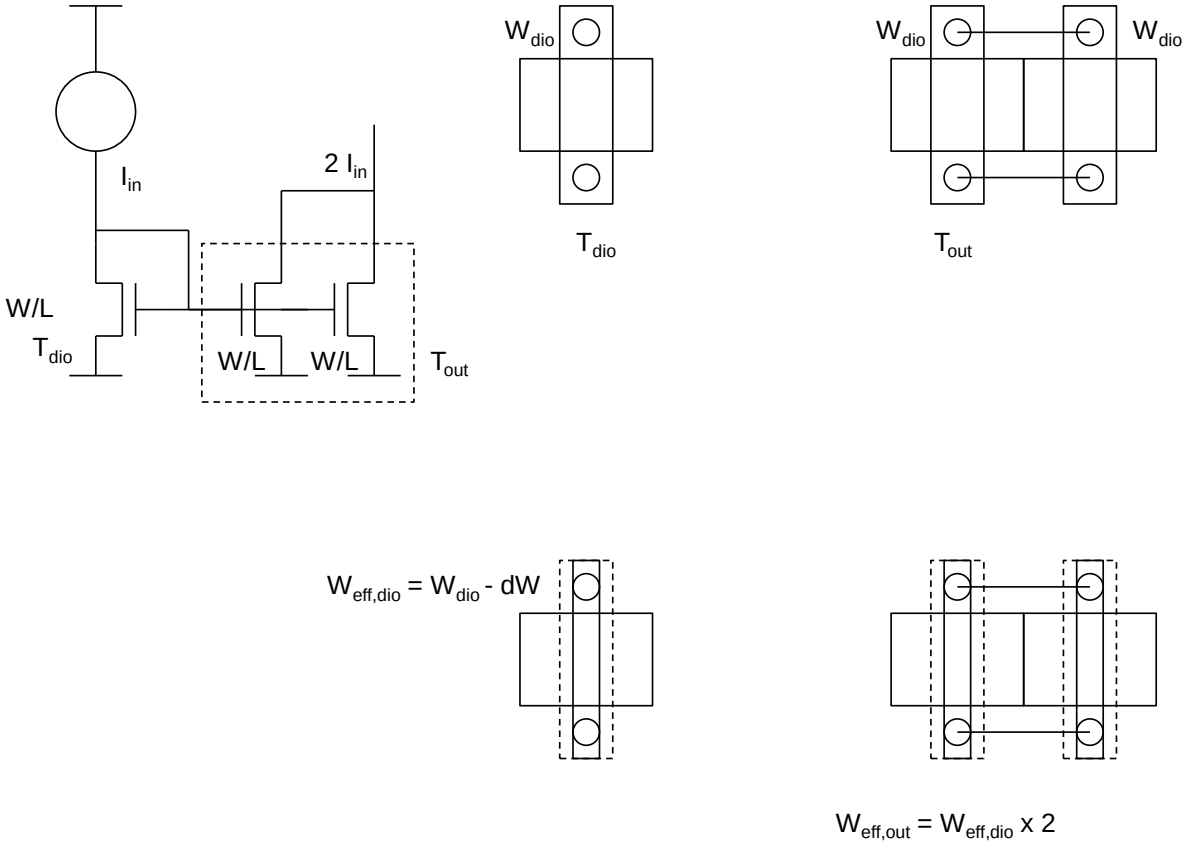

Fig 15: Accuracy of the current mirror with n = 2. T_{out} has two gates

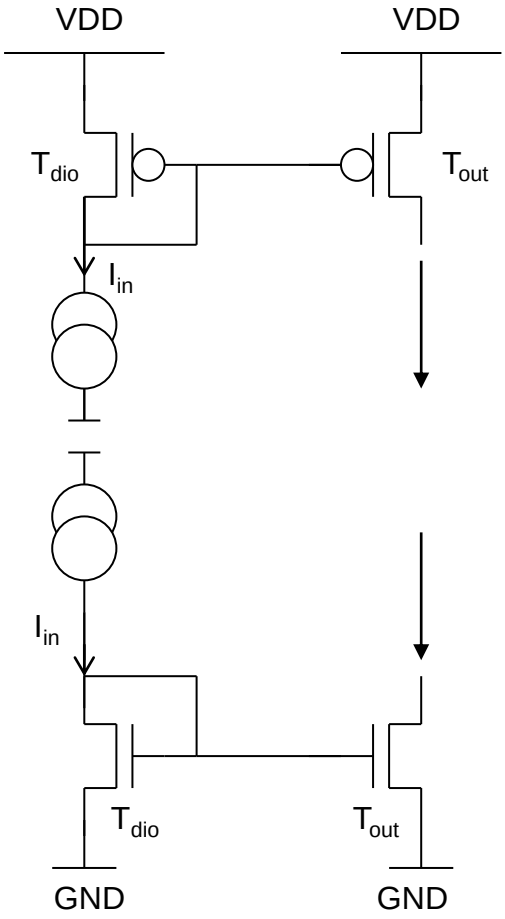

Fig 16: PMOS und NMOS implementation of a current mirror

Fig 16 shows PMOS and NMOS variants of a current mirror. There are following differences.

PMOS current mirror is normally connected to VDD (positive voltage supply). The current flows to GND. NMOS sources are normally connected to GND and the current flows from the external circuit into the device.

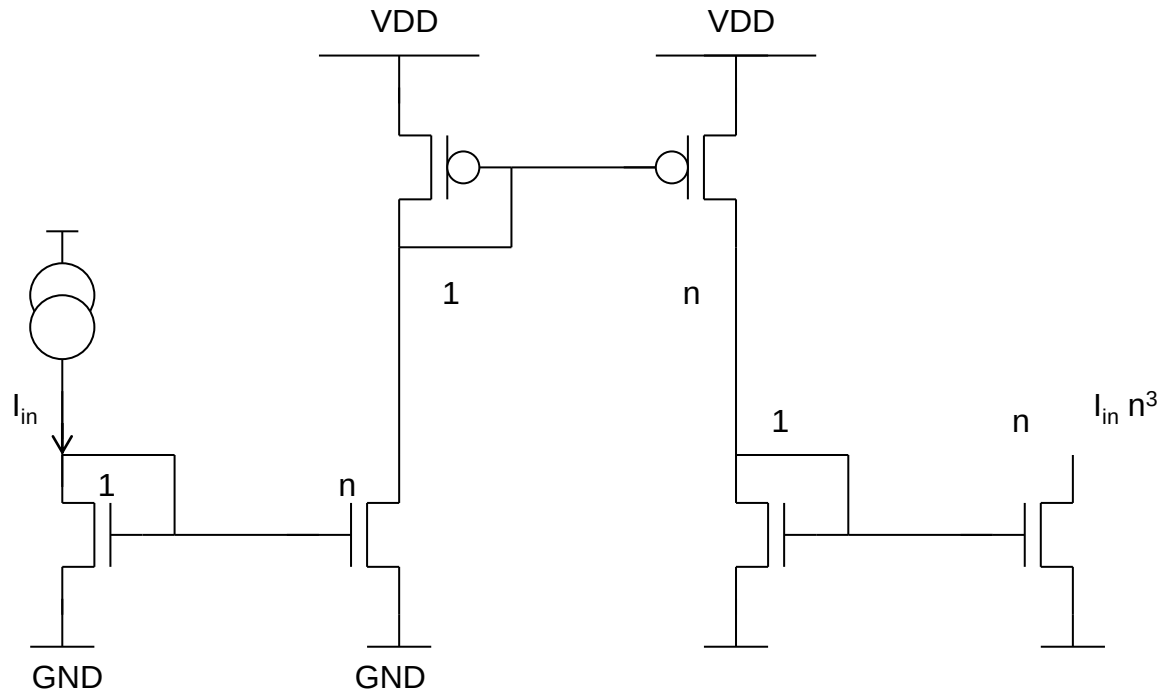

Fig 17: Cascade of current mirrors

Thanks to different current directions, PMOS and NMOS current mirrors can be combined (cascaded) to achieve greater amplification

Small Signal Model of the current mirror

The small signal circuit of the current mirror can be obtained when both transistors are replaced with small signal models. Fig 18 - Fig 21 illustrate the approach.

It holds for small signals:

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{n}{1+(n+1)\frac{C_{gs,dio}}{g_{m,dio}}} \qquad (3)$$

With: $n = g_{m,out}/g_{m,dio}$ and $n = C_{gs,out}/C_{gs,dio}$.

Notice the following:

The current multiplication is equal to n. The current mirror acts as a low pass filter. The time constant is $(n+1)\, C_{gs,dio}/g_{m,dio}$. The circuit is slower when the gain is higher.

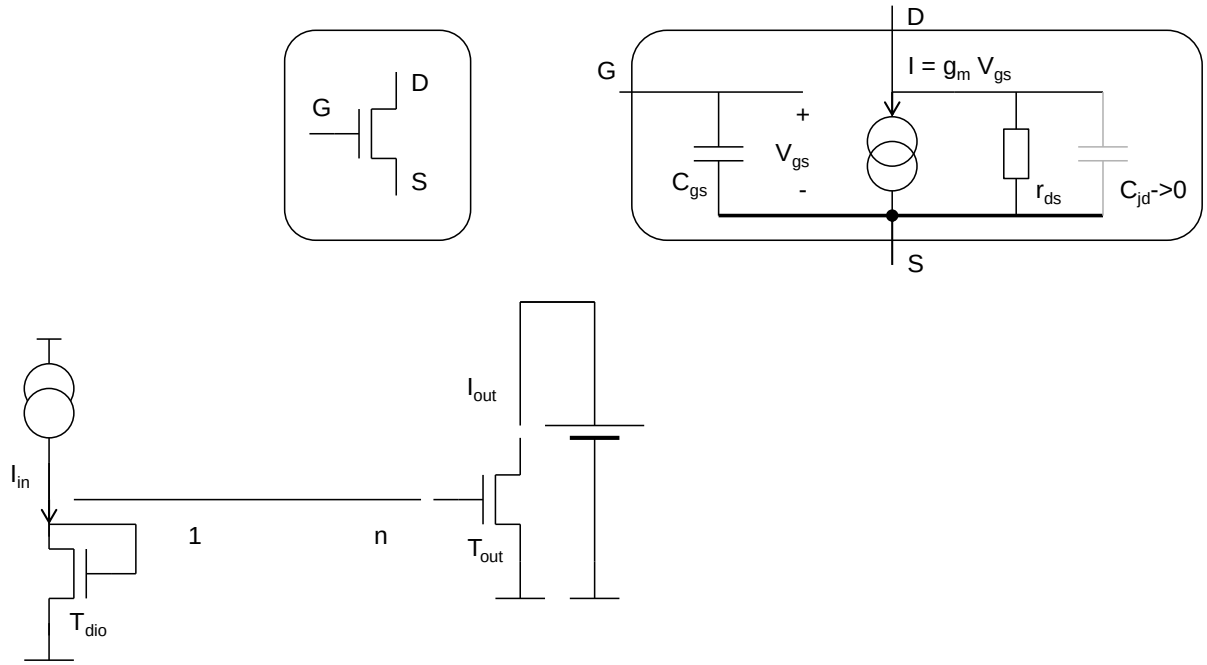

Fig 18: Small signal model of the current mirror (1)

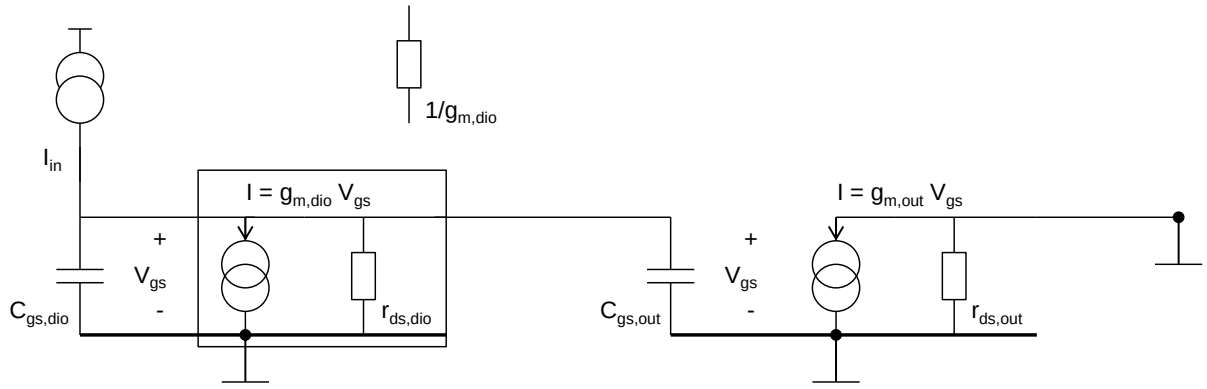

Fig 19: Small signal model of the current mirror (2)

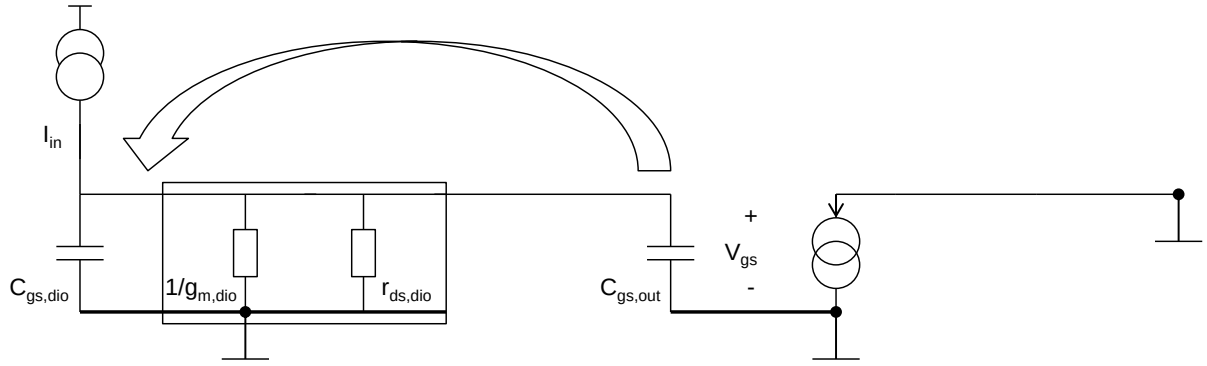

Fig 20: Small signal model of the current mirror (3)

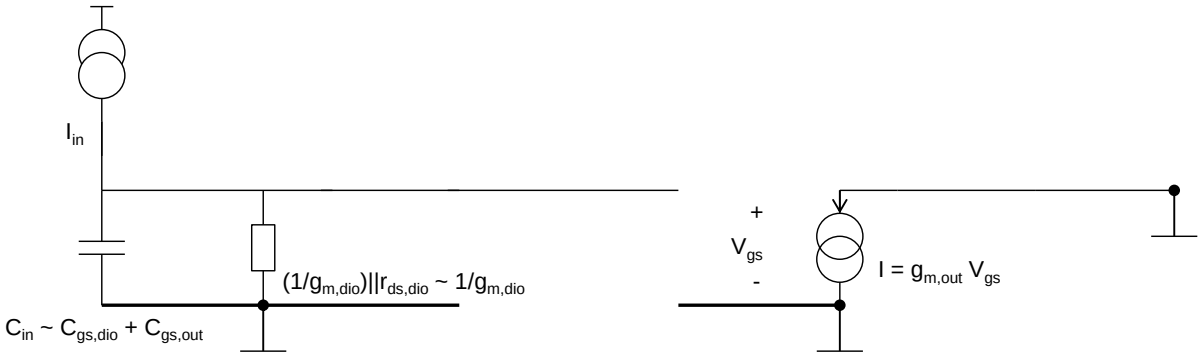

Fig 21: Small signal model of the current mirror (4)

We have shown (1) and (2) that: $n = \frac{\left(\frac{W}{L}\right)_{out}}{\left(\frac{W}{L}\right)_{dio}}$.

The small signal analysis leads to (3) $n = \frac{g_{m,out}}{g_{m,dio}}$.

Are the n-factors equal? Yes, because:

$I = ½ \mu C_{ox} W/L (V_{gs} - V_{th})^2$ and $g_m = dI/dV_{gs} = \mu C_{ox} W/L (V_{gs} - V_{th})$.

Since $V_{gs} – V_{th}$ are equal for T_{dio} and T_{out} , it holds $g_{m,out} / g_{m,dio} = (W/L)_{out} /(W/L)_{dio}$.

Influence of output resistance (optional)

Let us bierfly discuss the influence of R_{ds} on the transmission function.

The resistors $R_{ds,dio}/R_{ds,out}$ lead to an error in the current copying and the current multiplication if V_{dsout} is different as V_{dsin}. If the drain-source voltages of T_{dio} and T_{out} transistors are different, I_{in} and I_{out} are not in the same relationship with the W/L-s because parts of the currents flow through R_{ds}. This is shown in Fig 22.

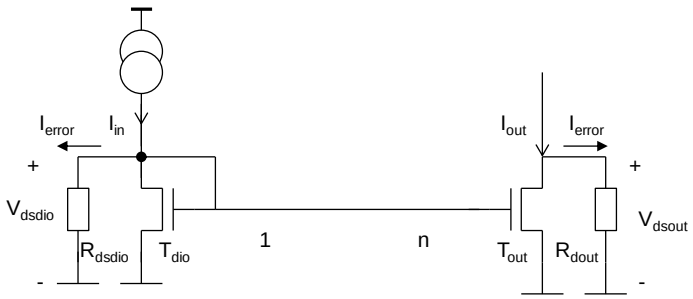

Fig 22: Influence of drain source resistances to the output current

How can we improve a current mirror? Remember that R_{ds} will be higher if the transistors are longer. Long transistors are usually suitable for current mirrors and for current sources.

There is a problem here: if we extend L, V_{gs} and V_{dssat} increase as well. The condition $V_{out} > V_{dssat}$ is more difficult to fulfil and we get a limited range for the output voltage, as shown in Fig 23.

There are trade offs between amplification, speed, linearity (absence of signal-dependent errors) and the possible dynamic range.

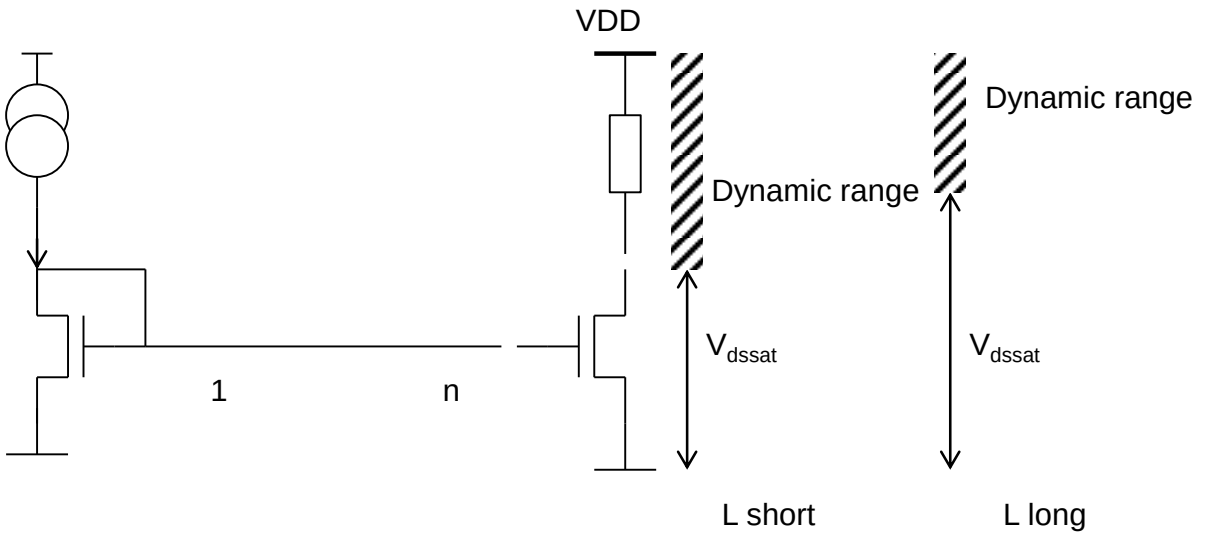

Fig 23: Voltage dynamic range at the output of the current mirror

Common source amplifier

We will discuss one of the most important basic circuit: the common source voltage amplifier.

The name indicates that the source of the input transistor is connected to a constant voltage or ground in the small signal model.

The easiest way to design a common source amplifier is to attach a load resistor R_{load} to an input transistor T_{in} working as a current source, as shown in Fig 24. The resistance fulfils two tasks: first to bias the input transistor T_{in} and to create a proper DC work point, second to convert the output current into a voltage.

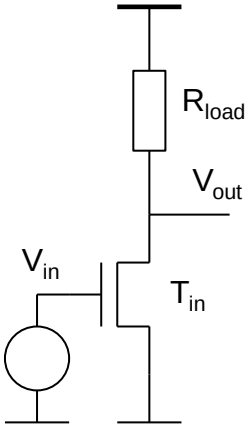

Fig 24: Common source amplifier

As we shown in lecture 5, we can perform the DC analysis graphically (using U-I characteristic).

On the same plot we draw the I_{ds} - V_{ds} characteristic of the transistor and the corresponding characteristic of the resistor, as shown in Fig 25. We determine the output voltage as the intersection point of the transistor and the resistor characteristic. If the input voltage increases, the transistor characteristic moves upwards and the output voltage moves from the positive supply VDD to the left.

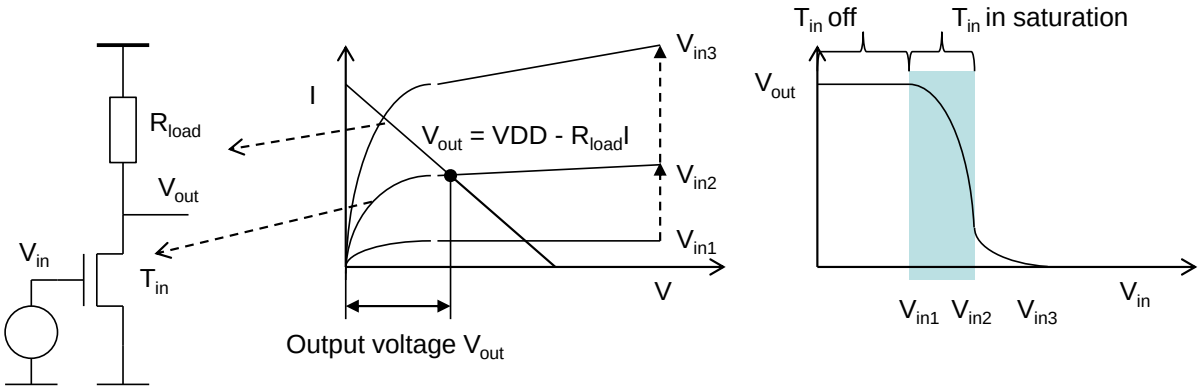

Fig 25: Graphical DC analysis

For the working region where T_{in} is in saturation (condition $V_{out} > V_{dssat} = V_{in} - V_{th}$), we can derive the small signal model. The voltage gain can be calculated from the small signal circuit shown in Fig 26:

$$A = \frac{v_{out}}{v_{in}} = -g_m(r_{ds}||R_{load}) \equiv -g_m r_{out} \quad (6)$$

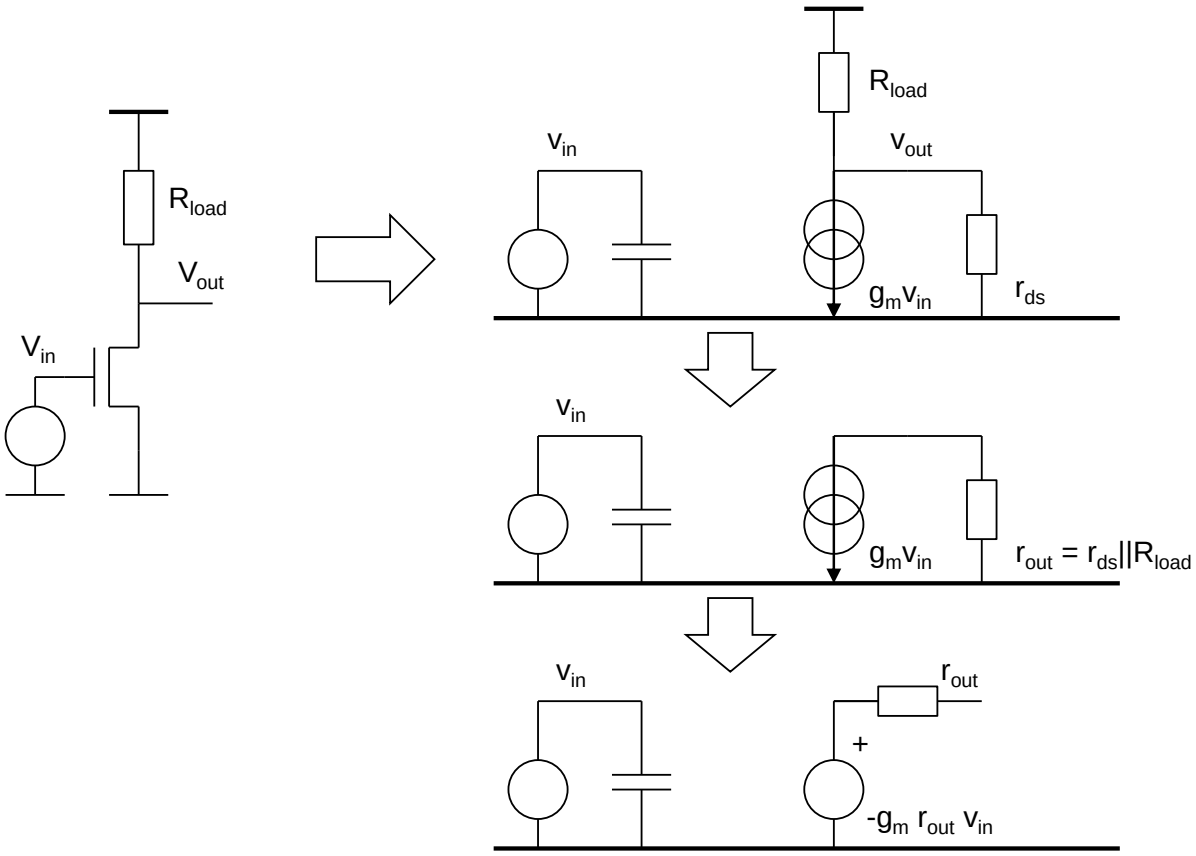

Fig 26: Common source amplifier – small signal circuit

Common source amplifier with active load

Motivation

In order to maximize the voltage gain we need large values for g_m and r_{out}.

Resistance $r_{out} > 50\ k\Omega$ is considered to be large. A transconductance $g_m > 1$ mS is also considered as large.

The disadvantage of the amplifier with a linear resistance is that it is not possible to maximize both g_m and R_{load}. If the resistance R_{load} is large, its characteristic is close to the x-axis. The transistor current is small. A small current leads to a small transconductance. This is illustrated in Fig 27.

If the resistance R_{load} is small, the transistor current is higher, as well as the transconductance. However, because of the small R_{load}, the amplification is small.

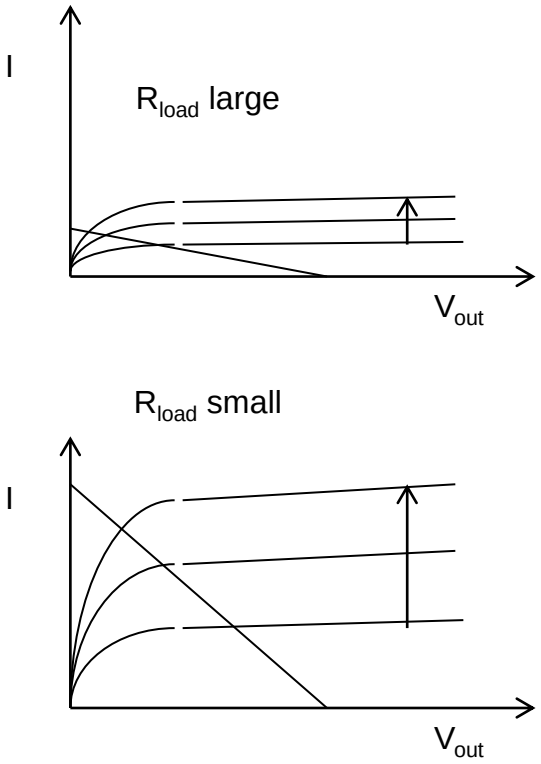

Fig 27: I-V characteristic for small and large R_{load}

A characteristic that rises relatively quickly and then moves horizontally across a large V_{out} region (as shown in Fig 28) would be better than the characteristic of a linear resistor.

A PMOS transistor (a PMOS current source) with source connected to VDD (positive voltage supply) and with a constant gate potential has almost ideal characteristic, as shown in Fig 29.

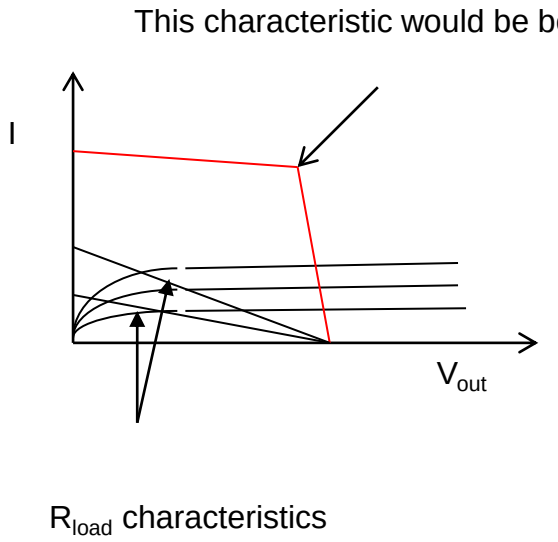

Fig 28: I-V characteristic of the ideal load element

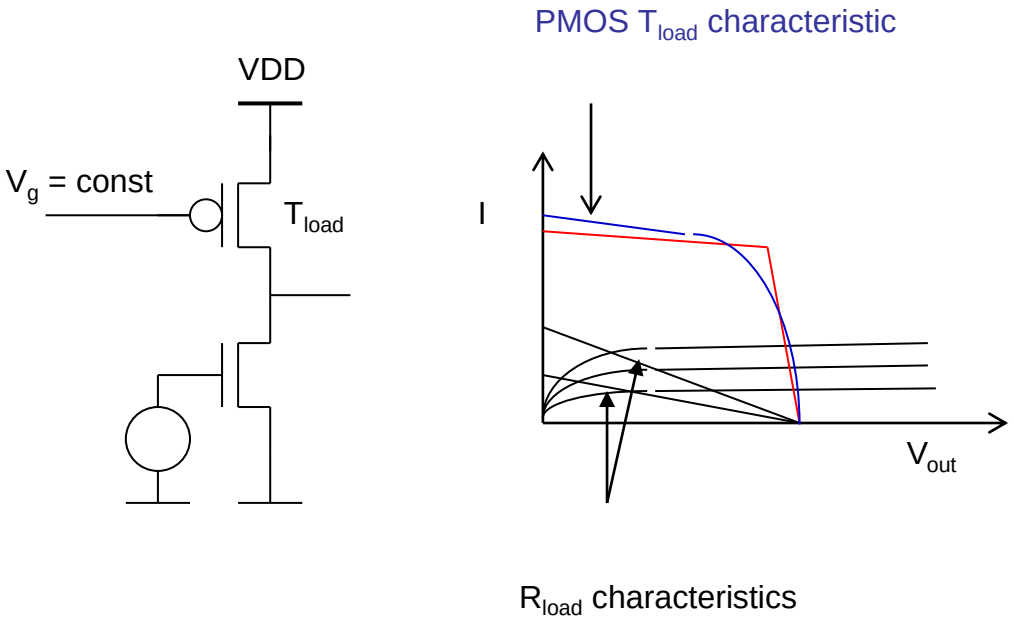

Fig 29: I-V characteristic of the ideal load element and PMOS current source characteristic

Therefore, we can improve the voltage amplifier by replacing the resistance R_{load} with a PMOS current source, as shown in Fig 30. The figure also shows the bias circuit for the current source in the form of a MOSFET diode T_{dio} and a reference current source I_{bias}. The reference current can be implemented in different ways, the simplest is using a resistor R_{bias}. We refer to the load element implemented with a transistor as the *active load*. We call the circuit from Fig 30 the common source amplifier with active load.

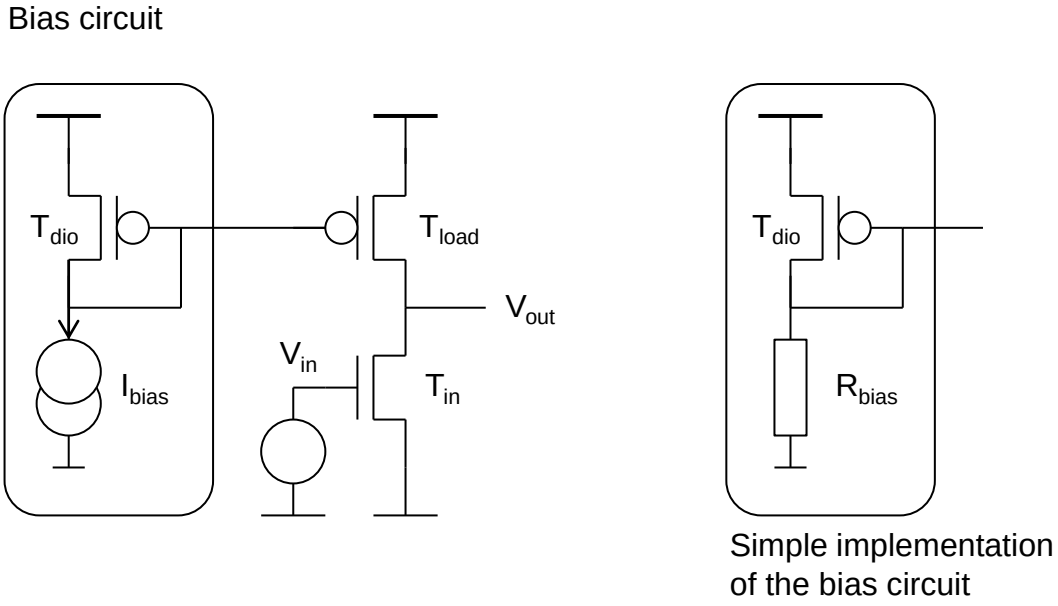

Fig 30: Common source amplifier with active load

From the characteristics of T_{in} and T_{load} we can graphically derive a $V_{out} = f(V_{in})$ characteristic (Fig 31). The amplification is high only in the region where both transistors T_{in} and T_{out} are in

saturation. We see that DC current is relatively high in this area, so we can expect a high transconductance.

The condition for saturation of T_{in} is $V_{out} > V_{in} - V_{th}$. The condition for saturation for T_{load} is $V_{out} < VDD - V_{dssat,load}$ where $|V_{dssat}| = |V_{gs}| - |V_{th}|$.

The region where both transistors are in saturation is marked with grey in Fig 31 (bottom figure).

We see from the upper graph in Fig 31 that the DC current is large in the region with large gain. We can therefore expect a large transconductance g_m.

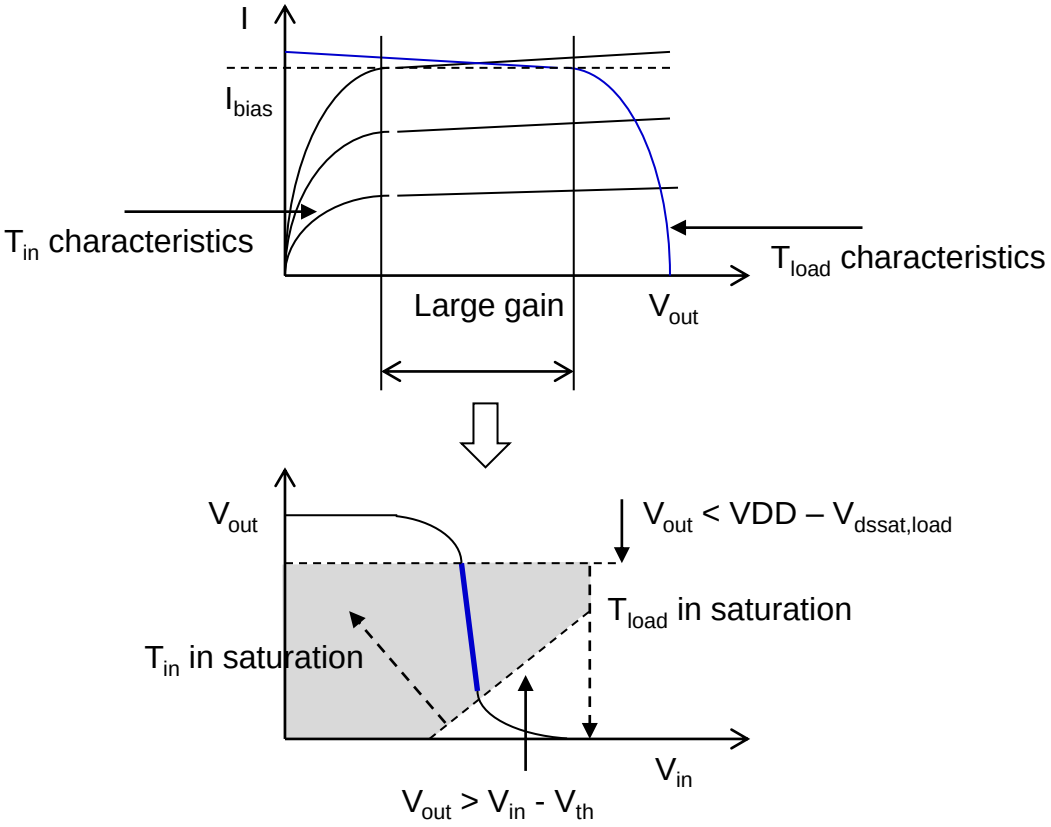

Fig 31: Input-output characteristic of the voltage amplifier with active load

The small signal model of the circuit, when both transistors are in saturation is shown in Fig 32.

The voltage amplification is:

$$A = -g_{m,in}(r_{ds,in}||r_{ds,load}) \equiv -g_{m,in}r_{out}$$

$G_{m,in}$ and $r_{ds,in}$ are the transconductance and the drain-source resistance of the input transistor Tin. $r_{ds,load}$ is the drain-source resistance of the load transistor T_{load}.

An amplifier is a two port circuit. This circuit can be described with its amplification and the input and the output impedances. The input impedance of the amplifier arises from the gate source capacitance of T_{in}. The output resistance is:

:

$$r_{out} = r_{ds,in} || r_{ds,load}$$

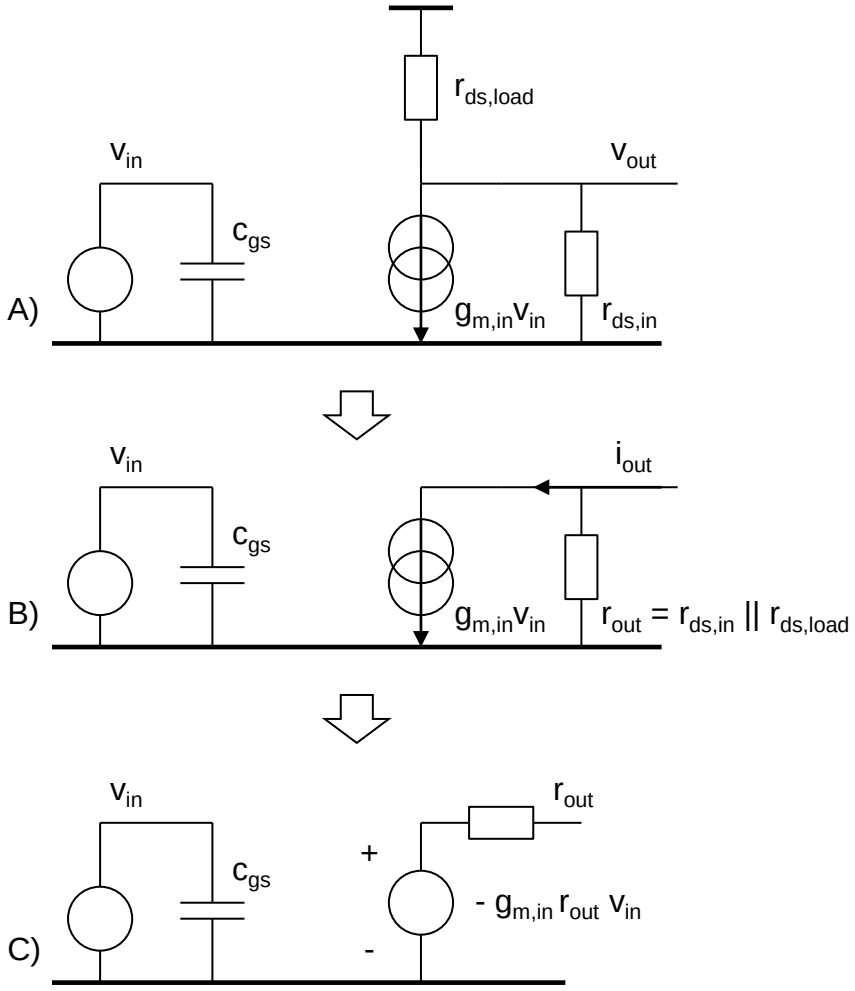

Fig 32: Small signal model of the common source amplifier with active load

The amplifier can therefore be represented as a voltage controlled current source with the current $i_{out} = g_{m,in}\, v_{in}$ and the output resistance $r_{out} = r_{ds,in} \parallel r_{ds,load}$. This is circuit B in Fig 32.

The amplifier can also be represented as a voltage controlled voltage source with the voltage $v_{out} = - g_{m,in}\, r_{out}\, v_{in}$ and the output resistance $r_{out} = r_{ds,in} \parallel r_{ds,load}$. This is circuit C in Fig 32. Both representations are equivalent.

One application example for the current mirror – receiver of the photo-current (optional)

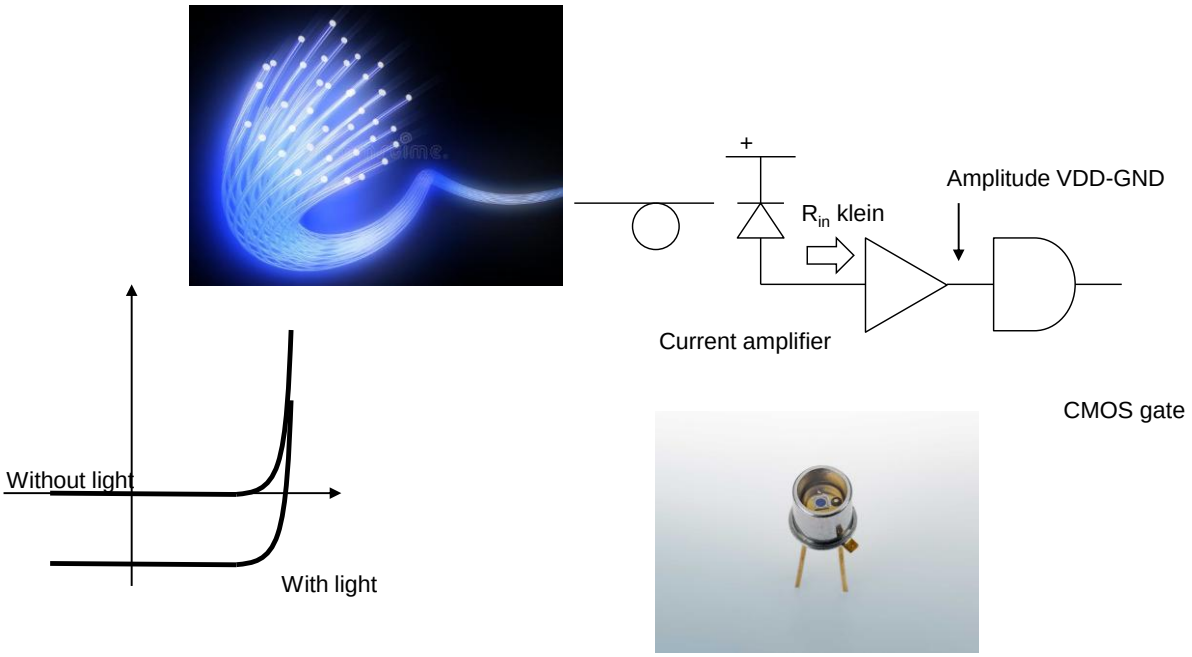

Fig 33: Fast current amplifier based on a current mirror

Current mirrors are fast current amplifiers. An application example for a current mirror as an amplifier shown in Fig 33. A photodiode measures the light and generates the photo current. The current sould be converted into a voltage whose amplitude is large enough so that the digital circuits "understand" the logical 1 or 0.

The important feature of a current amplifier is a small input resistance. Why? If the resistance is large, a large time constant is created at the input and makes the circuit slower.

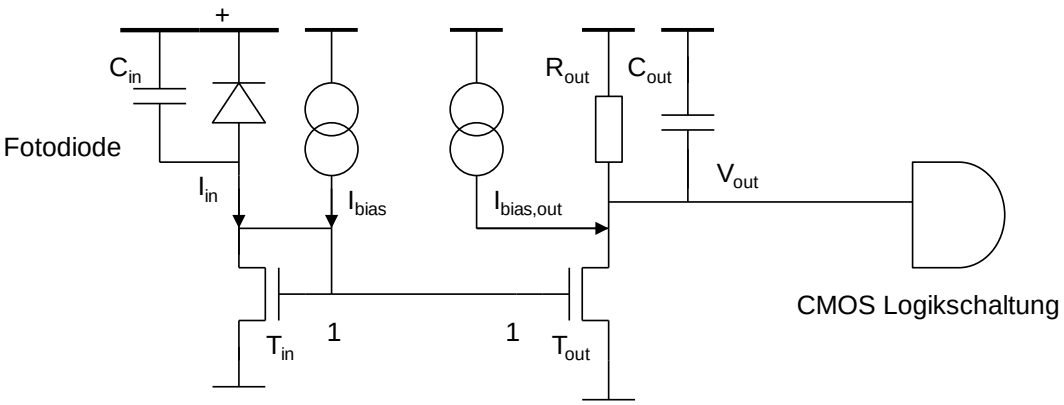

Fig 34: Fast current amplifier based on a current mirror - schematics

Fig 34 shows the schematic diagramm of the current amplifier. The photodiode is placed at the input of the current mirror, the output is connected to the resistance R.

Analysis of the circuit

The AC output voltage is

$v_{out} = R_{out}\, i_{out} = R_{out}\, i_{in}$

The gain $Z = v_{out} / i_{in}$, called transimpedance, is:

$$Z = \frac{v_{out}}{i_{in}} = R_{out}$$

The circuit is a low pass filter with two time constants. The first time constant T_{in} is created at the entrance:

$$T_{in} = C_{in}R_{in} = (C_{fotodiode} + 2C_{gs})/g_{m,in}$$

The second time constant is at the output:

$$T_{out} = C_{out}R_{out}$$

Specifications

Let us assume the following values: $C_{photodiode} = 100fF$, $i_{in} = 5\mu A$, $C_{out} = 5fF$. We want the time constants to be less than 100ps and the output amplitude to be at least 100mV.

Synthesis of the circuit

The specified gain can be achieved with the following output resistance:

$$Z = \frac{v_{out}}{i_{in}} = \frac{100mV}{5\mu A} = 20k\Omega = R_{out}$$

From the condition:

$$T_{in} = C_{in}R_{in} = \frac{C_{fotodiode}+2C_{gs}}{g_{m,in}} = 100ps$$

$g_{m,in}$ can be derived.

We assume that $C_{photodiode}$ is greater than $2C_{gs}$. Therefore:

$$\frac{C_{fotodiode}}{g_{m,in}} = 100ps \Rightarrow g_{m,in} = \frac{C_{fotodiode}}{100ps} = 1mS$$

To achieve a transconductance of 1mS, we need a bias current source I_{bias}. The photo current alone would not be enough to achieve the transcondance 1mS.

To calculate I_{bias}, we can assume that the formula for strong inversion is valid:

$$I_{bias} = I_{ds} = k_s \frac{W}{L}(V_{gs} - V_{th})^2$$

Transconductance is:

$$g_{m,in} = \frac{dI_{ds}}{d_{Vgs}} = k_s \frac{W}{L} 2(V_{gs} - V_{th}) = \frac{2I_{ds}}{(V_{gs} - V_{th})} = \frac{2I_{bias}}{(V_{gs} - V_{th})}$$

We can further assume that V_{gs} is e.g. 200mV higher than $V_{th.}$ The transistor can be dimensioned later accordingly. The following applies:

$$I_{bias} = \frac{1}{2} g_{m,in} (V_{gs} - V_{th}) = \frac{1}{2} 1\text{mS}\ 200\text{mV} = 100\mu\text{A}$$

The bias current can also be roughly estimated if one assumes that T_{dio} works between strong and weak inversion and that its transconductance can be calculated with the formula for weak inversion:

$$g_{m,in} = \frac{I_{bias}}{1.25U_T} = 1\text{mS} => I_{bias} = 32.5\mu\text{A}$$

Let us note that the bias current is much larger than the photo current. If we only had one bias power source, the bias current would also flow through T_{out} and $R_{out,}$ creating a DC voltage (offset). The offset would be:

$$I_{bias} R_{out} = 100\mu\text{A} \times 20\text{k}\Omega = 2\text{V}$$

This is too much, as the supply voltage is 1.2V.

To minimize offset, we use another bias current source $I_{bias,out}$ = 100µA, which subtracts the bias current at the output and minimizes the offset.

At the end, let us calculate the output time constant:

$$T_{out} = C_{out} R_{out} = 5\text{fF}\ 20\text{k}\Omega = 100\text{ps}$$

The time constant is small enough because C_{out} is small. If C_{out} were larger, we would have to reduce R_{out} and achieve the necessary transimpedance with a current amplification.