Lecture 6 (part 2)

Themes:

Small signal model of a MOSFET

MOSFET capacitances

Transit frequency

RF-MOSFET

Small signal model of MOSFET for slow signals (without capacitances)

In lectures 2 - 4 we described MOS transistors, their production and working principle.

We have derived the equations for drain-source current as a function of V_{gs} and V_{ds}.

An important parameter is the threshold voltage.

For V_{ds} voltages higher than V_{dssat}, the drain-source current saturates.

V_{dssat} is the saturation voltage.

$V_{dssat} = (V_{gs} – V_{thsb})/n$.

N is the subthreshold factor

$n = 1 + C_{dep,ac}/C_{ox} \sim 1.25$.

All the equations we have derived for NMOS also apply to PMOS transistors if we negate voltages (V_{gs} and V_{ds}) and currents (I_{ds}), or take their magnitude instead of the signed value.

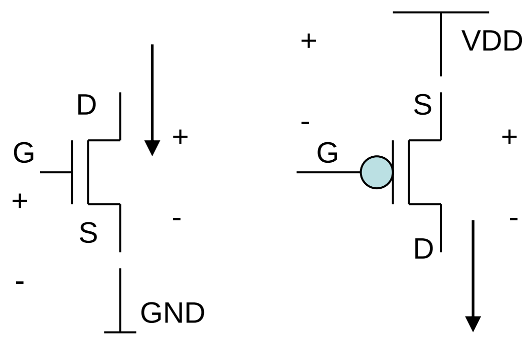

Figure 1: NMOS und PMOS

For $V_{ds} > V_{dssat}$, the current increases only slightly due to the channel length modulation, as shown in Figure 2.

We define the drain-source conductance:

$$g_{ds} = \frac{dI_{ds}}{dV_{ds}}$$

And the output resistance:

$$r_{ds} = \frac{1}{g_{ds}} \sim \frac{E_{sat} L}{I_{dssat}}$$

E_{sat} is the E-field strength at which mobility (drift speed of electrons) gets saturated. L is the transistor length.

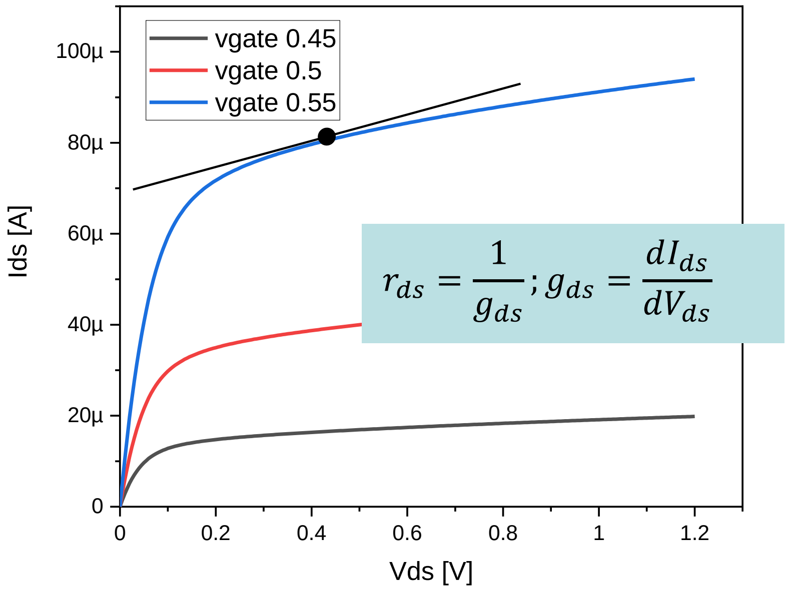

Figure 2: *Output characteristics of the MOS transistor*

For small signals, the transistor in saturation behaves like a controlled current source with the following transconductance (Figure 3).

$$g_m = \frac{dI_{dssat}}{dV_{gs}}$$

and the output resistance r_{ds}.

We can also derive the following formula:

$$g_m = \frac{dI_{dssat}}{dV_{gs}}$$

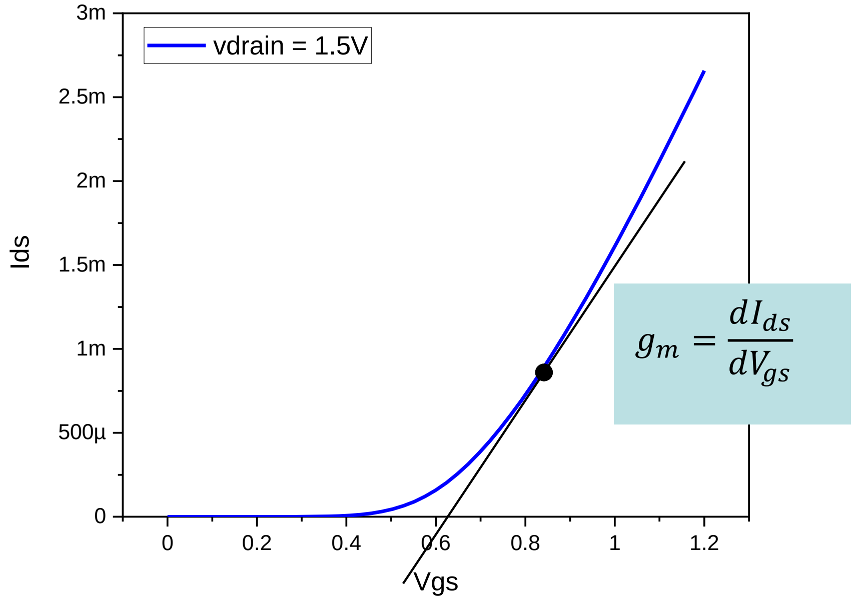

Figure 3: Input characteristics of MOS transistor

The small signal model of the transistor (for slow signals) is derived from the transistor equation:

$$I_{ds} = I_{dssat}(V_{gst})\left(1 + \frac{V_{ds} - V_{dssat}}{V_A}\right);\ v_{gst} = V_{gs} - V_{thsb}; V_{thsb} = V_{th} - (n-1)V_{bs}$$

We linearize the equation at the operating point:

$$i_{DS} = I_{ds,DC} + i_{ds,ac} = I_{ds,DC} + \frac{dI_{ds}}{dV_{gs}} v_{gs} + \frac{dI_{ds}}{dV_{ds}} v_{ds} + \frac{dI_{ds}}{dV_{sb}} v_{bs}$$

It follows:

$$i_{ds,ac} = \frac{dI_{ds}}{dV_{gs}} v_{gs} + \frac{dI_{ds}}{dV_{ds}} v_{ds} + \frac{dI_{ds}}{dV_{sb}} v_{sb} = g_m v_{gs} + g_{ds} v_{ds} + g_{mb} v_{bs}$$

The last term describes the substrate effect. A higher voltage v_{bs} lowers the threshold and leads to the current increase. Note that v_{bs} increases current in a similar way to v_{gs}. The following applies:

$$g_{m,b} = (n-1)\, g_m$$

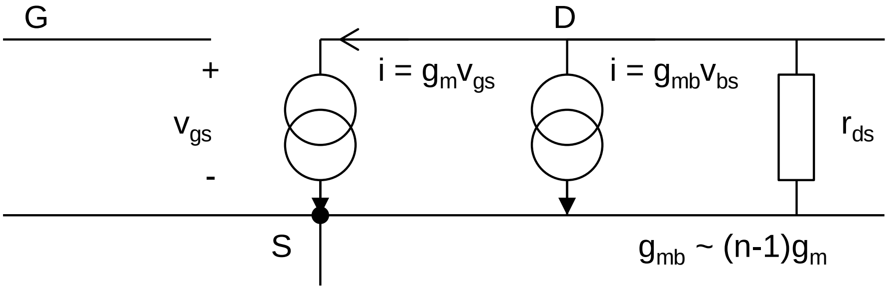

Figure 4: *Small signal model of the MOS transistor for slow signals*

Capacitances in MOS structure

The depletion regions and electrodes in the MOS structure contain charge, as shown in Figure 5. The amount of charge depends on the voltages applied between the electrodes. This is the reason why capacitances are formed. The relationship between the charge in the depletion regions and the voltages is non-linear. So-called dynamic capacitances are defined as dQ(V)/dV at the operating point. These dynamic capacitances are used in the small-signal model of the transistor.

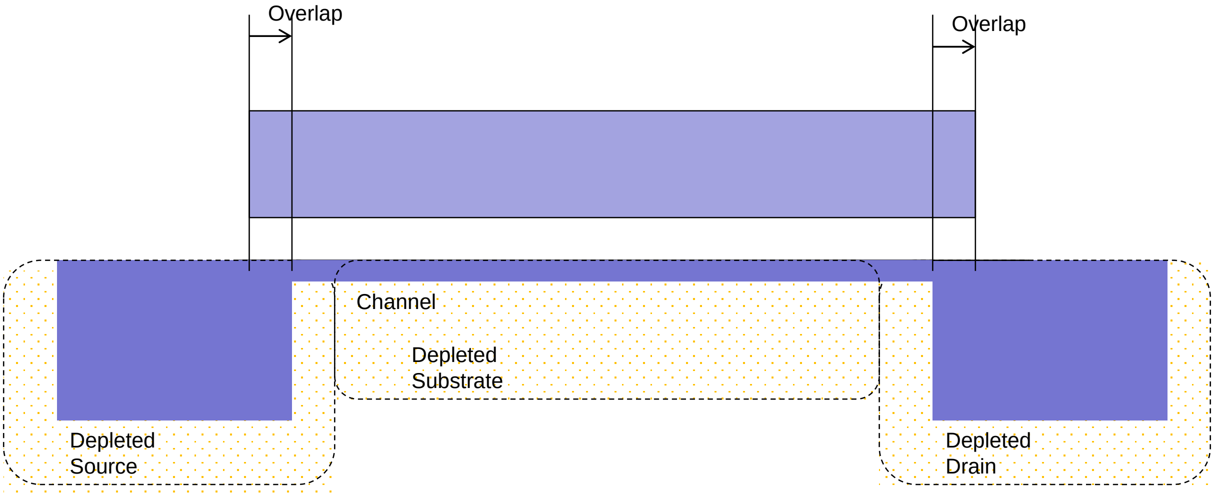

Figure 5: Regions with space charge within a MOSFET

Gate capacitance

The most important capacitance in transistor is its gate capacitance. We have already seen that there are two capacitances below the gate. The oxide capacitance $C_{ox} = C'_{ox} \times W \times L$ and the capacitance of the depletion zone $C_{dep} = C'_{dep} \times W \times L$.

C'_{ox} and C'_{dep} are the capacitances per unit area. Depending on operation region, weak- or strong inversion, the gate capacitance differs.

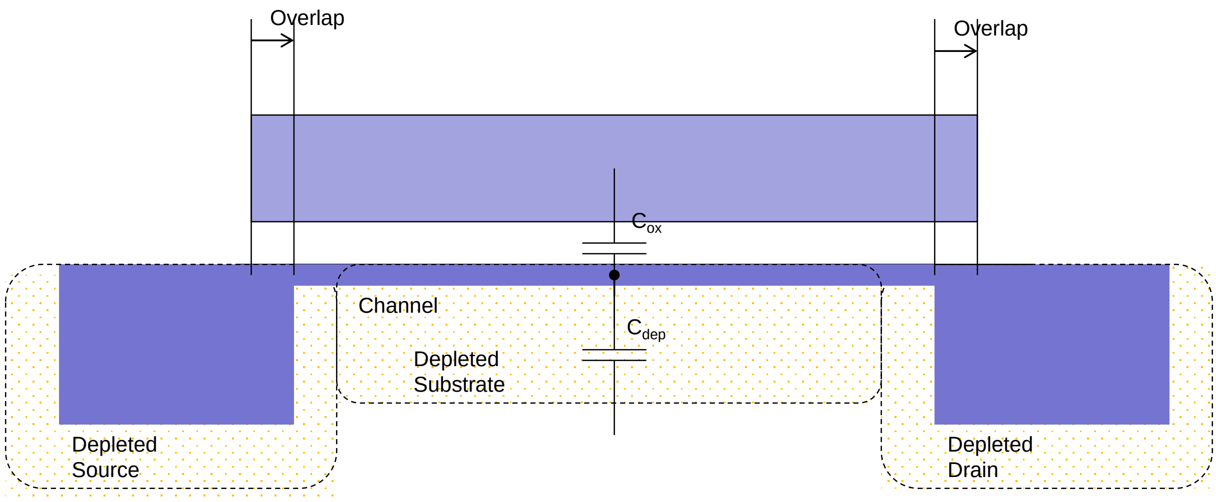

Figure 6: Gate capacitance

C_{gate} in weak inversion

The gate capacitance in weak inversion Figure 7 is the series circuit of C_{ox} and C_{dep}

$$C_{gate} = C_{gb} = WL\frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}}$$

The gate capacitance connects gate and substrate.

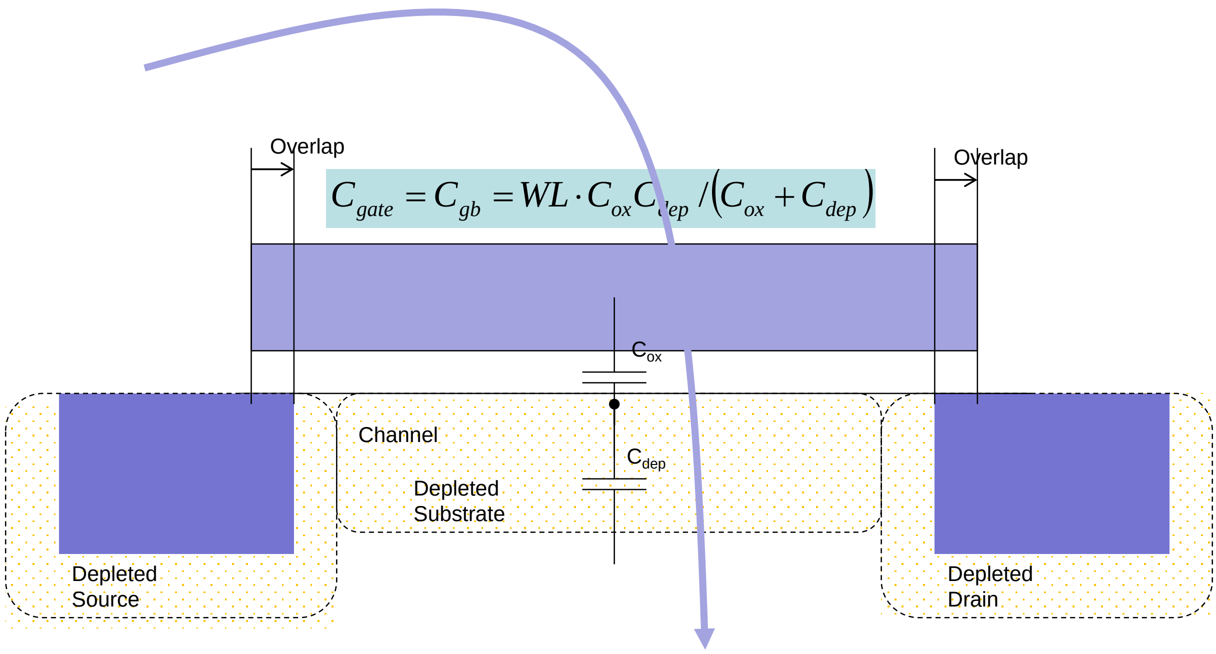

Figure 7: Gate capacitance in weak inversion

C_{gate} in strong inversion and V_{ds} = 0

The voltage across the depletion capacitance C_{dep} is, in strong inversion, essentially fixed because the source and drain are "shorted" by the conductive channel. This is why C_{dep} is not observed when the gate voltage is varied — the amount of charge in the depletion region does not change. Of the original two capacitances, only C_{ox} remains. Therefore, the gate capacitance is given by:

$$C_{gate} = C_{gsd} = WLC'_{ox}$$

The gate capacitance is therefore larger than in weak inversion.

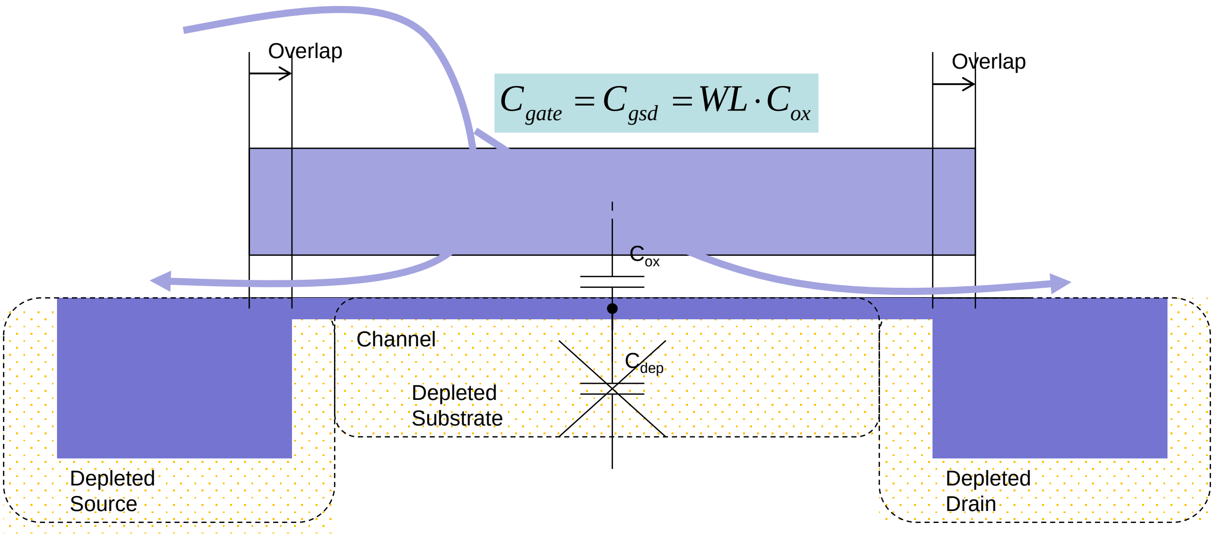

Figure 8: Gate capacitance in strong inversion for V_{ds} = 0.

C_{gate} in strong inversion and saturation ($V_{ds} > V_{dssat}$)

t can be shown that the charge in the channel is approximately 2/3 of that for V_{ds} = 0. Therefore, the gate capacitance is approximately:

$$C_{gate} = \frac{2}{3} WLC'_{ox}$$

If we have $V_{ds} > V_{dssat}$ (saturation), the channel is pinched off near the drain. As a consequence, the gate capacitance only exists between the gate and the source:

$$C_{gate} = C_{gs} = \frac{2}{3} WLC'_{ox}$$

There is no capacitance between drain and gate, as Figure 9 shows.

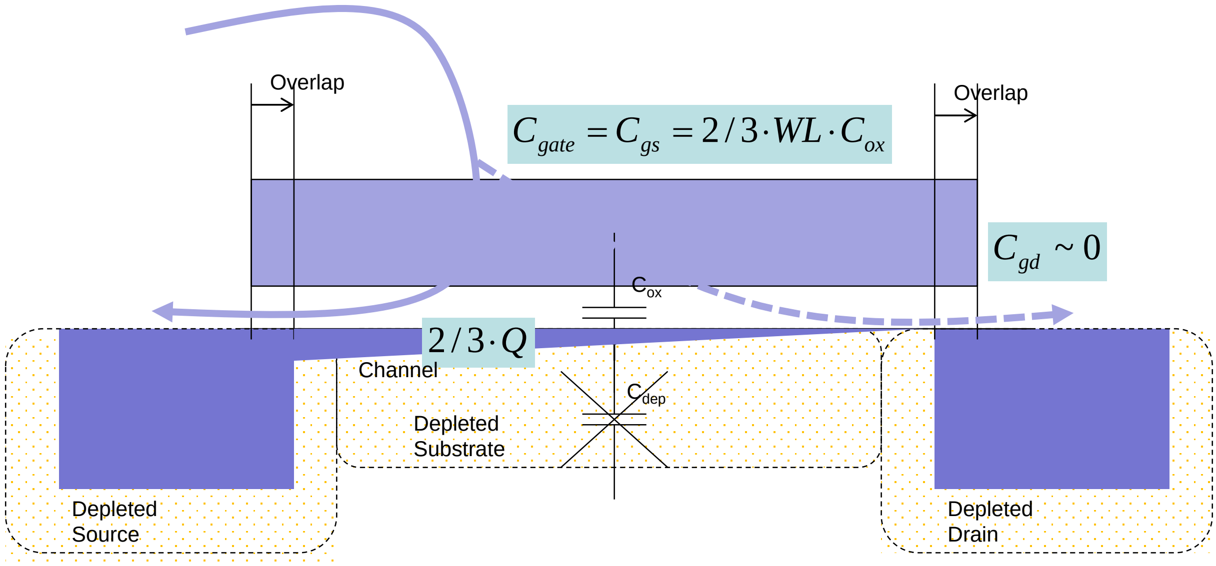

Figure 9: Gate capacitance in strong inversion for $V_{ds} > V_{dssat}$.

In addition to gate capacitances, we have the following smaller capacitances:

PN junction capacitances (junction capacitances) C_{jd}, C_{js}.

Overlapping capacitances $C_{gs,ovl}$ and $C_{gd,ovl}$. These capacitances are created because the source and drain areas extend partially under the gate oxide gate.

The drain gate capacitor $C_{gd,ovl}$ is especially important because it introduces feedback between transistor drain and gate. Drain is usually the output and gate the input of an amplifier.

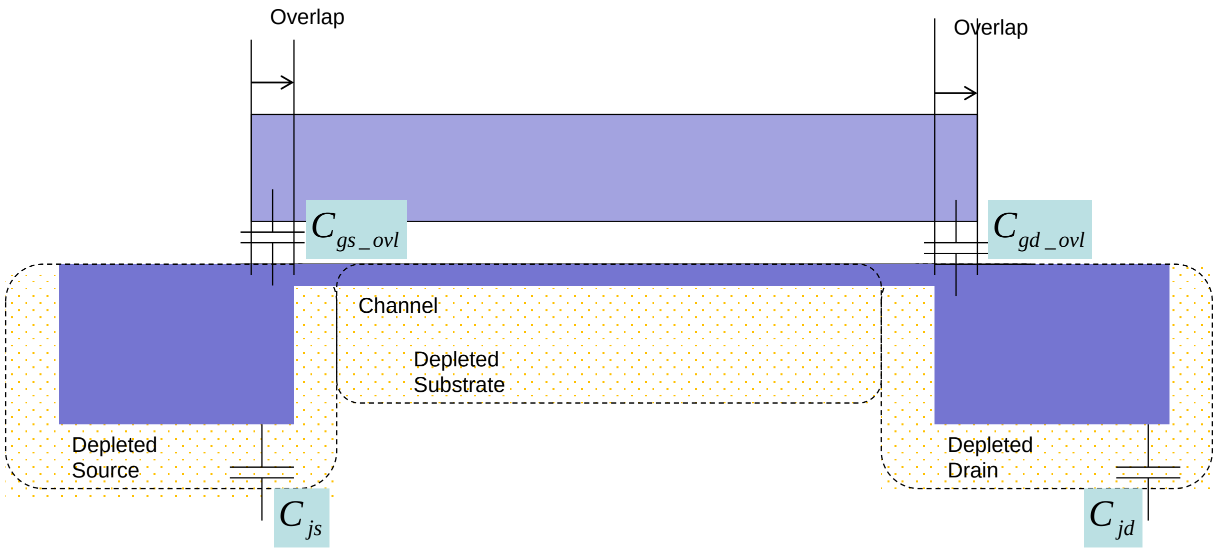

Figure 10: Additional capacitances

Small-signal model of the transistor with capacitances

The complete small signal model of the transistor is shown in Figure 11.

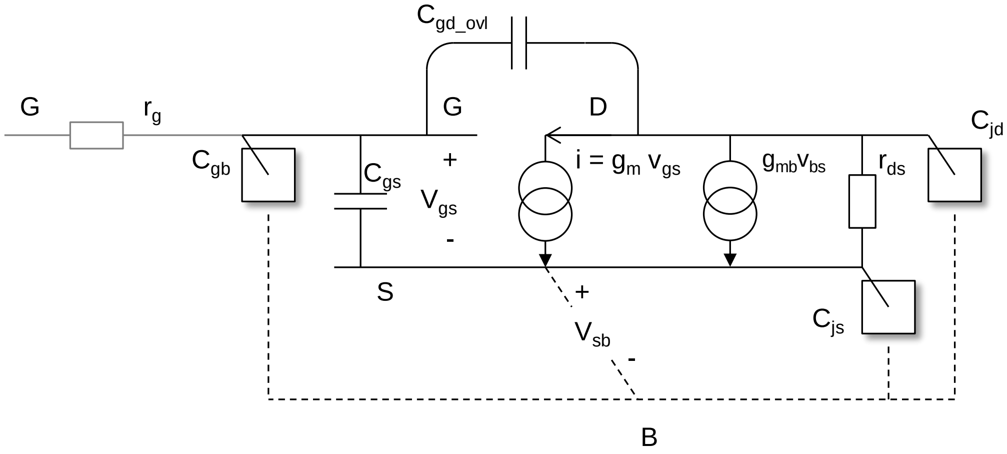

Figure 11: Small-signal model of the MOS transistor1

If the substrate and source are shorted, the model simplifies as shown in Figure 12.

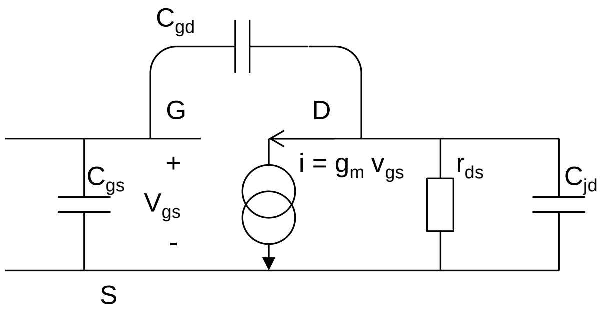

Figure 12: Small-signal model of the MOS transistor for $V2_{sb} = 0$

Transit Frequency (optional)

The transit frequency is the frequency at which a transistor has the small signal amplification equal to 1:

$$A(j\omega) = \left|\frac{i_{out}(j\omega)}{i_{in}(j\omega)}\right| = 1$$

Figure 13 shows the test circuit for the calculation of the transit frequency.

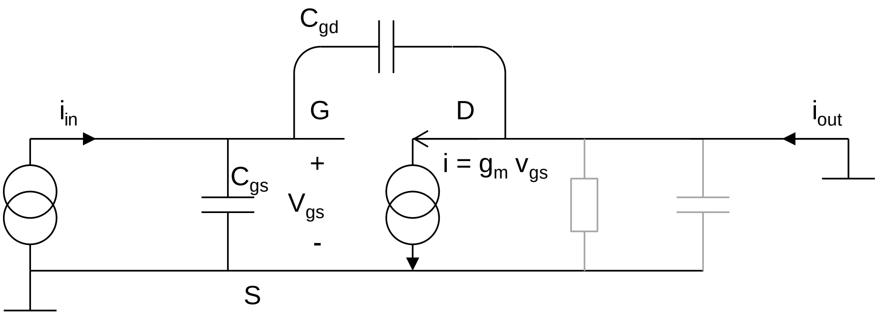

Figure 13: *Test circuit for the calculation of transit frequency*

It holds:

$$i_{in} = i\omega\left(C_{gs} + C_{gd}\right)v_{in}$$

$$i_{out} = \left(g_m - i\omega C_{gd}\right)v_{in}$$

The current amplification is:

$$A(\omega) = \left|\frac{i_{out}}{i_{in}}\right| = \left|\frac{(g_m - j\omega C_{gd})}{j\omega(C_{gs}+C_{gd})}\right| = \frac{\sqrt{g_m^2+\omega^2 C_{gd}^2}}{\omega(C_{gs}+C_{gd})}$$

From the condition:

$$A(\omega_T) = 1$$

follows the formula for the transit frequency ω (in rad/s):

$$\omega_T = \frac{g_m}{C_{gs}\sqrt{1+\frac{2C_{gd}}{C_{gs}}}} \sim \frac{g_m}{C_{gs}}$$

The transit frequency in Hertz is:

$$f_T = \frac{\omega_T}{2\pi}$$

We have shown in lecture 4 that the maximum conductance for a bias current is described with the following formula:

$$g_{m,max} = \frac{I_{bias}}{nU_T}$$

The transistor is then in weak inversion.

Example:

For an NMOS transistor in 65nm technology with W = 8µm and L = 60nm and for V_{gs} = 1V we simulate the transit frequency of f_T = 160GHz.

The transit frequency shows us the theoretical maximum bandwidth of an amplifier with gain 1 and without load impedances.

Such large bandwidths are difficult to achieve. One reason are the time constants that arise e.g. because of the resistance of the gate line. This time constant is:

$$T_{gate} = R_{gate}C_{gs}$$

Let us take, as example, a transistor in a 65nm technology with W = 8µm and L = 60nm. The transistor layout looks like Figure 14.

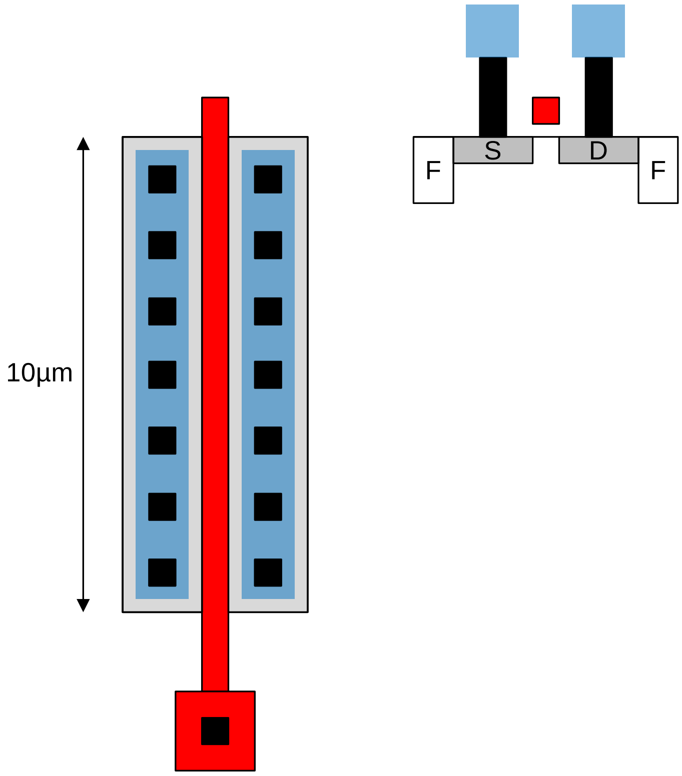

Figure 14: *Layout of the transistor*

In the technology, the capacitance is C'_{gs} = 13fF/µm^2 and the gate sheet resistance R'_{gate} = 12Ω/sq.

The gate-source capacitance is:

$$C_{gs} \sim C'_{gs}WL = 7.6fF$$

The gate resistance is:

$$R_{gate} = R'_{gate}\frac{W}{L} = 2k\Omega$$

The time constant is

$$T_{gate} = R_{gate}C_{gs} = 15.6ps$$

Which corresponds to a frequency of f = 1/(2πRC) = 10.2GHz. When we design transistors for high frequencies, we should try to minimize this time constant. This can be achieved through a better layout as in Figure 15. The transistor is realized as a parallel connection of several transistors to reduce the gate resistance.

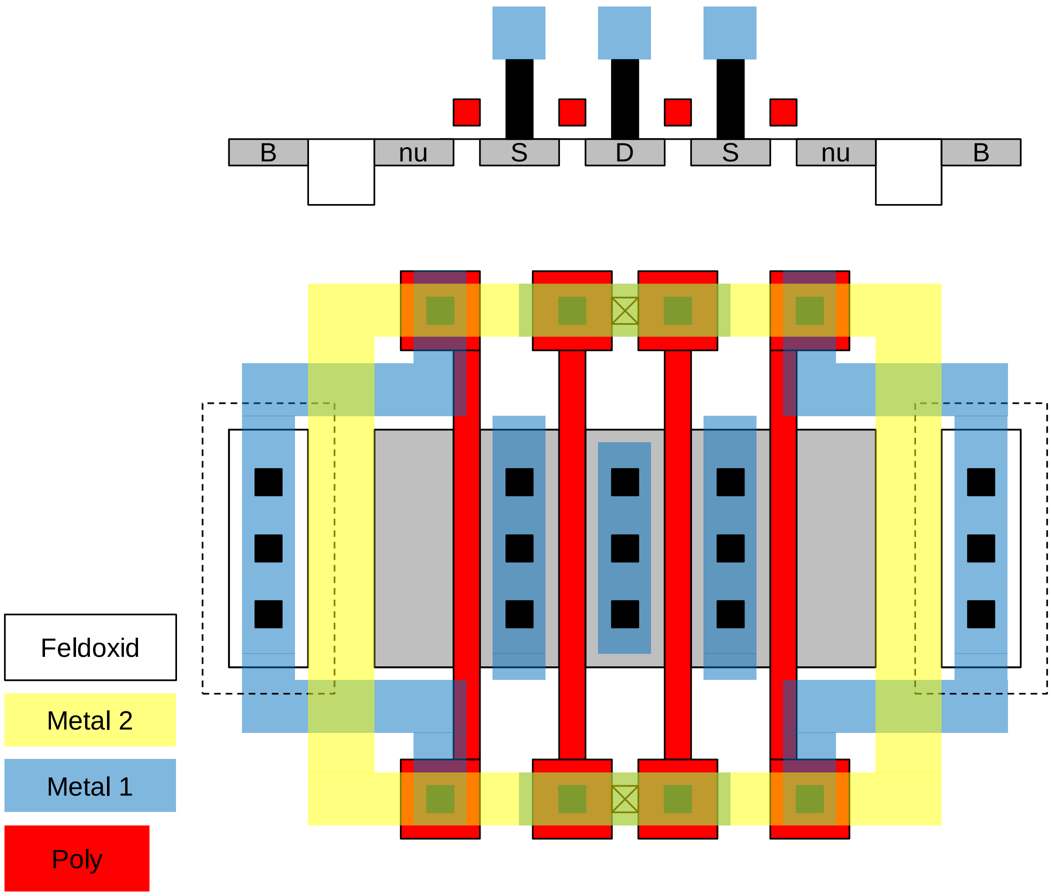

Figure 15: *Transistor layout optimized for high frequencies*