

## Lecture 1

### Themes of this lecture are

CMOS Technology: Origins and Significance

IC Manufacturing

Evolution of Analog IC Design Tools

Foundry & Manufacturing Processes

Cadence Virtuoso

Europractice

Schematics Design

Simulation

Layout Design

GDSII: The Layout File Format of IC Design

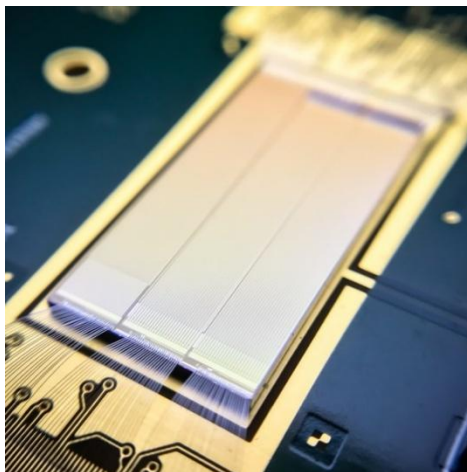
Analog Design Flow

Pixel Sensor Example

CMOS vs. Specialized Analog Circuits

### Introduction

Our group, the ASIC and Detector Laboratory (KIT-ADL) <https://adl.ipe.kit.edu/english/>, develops microchips for scientific and medical applications — for example, for detectors at particle accelerators, as well as for 3D ultrasound tomography or ion therapy.



*Figure 1: CMOS pixel sensor developed at KIT-ADL*

## **The course Analog Circuit Design**

The topic of this course is the design of integrated analog circuits in CMOS technology. The course includes lectures and exercises. In the lectures, theoretical knowledge is provided:

CMOS semiconductor technology and transistors

Analysis of circuits with feedback

CMOS amplifiers, starting from simple circuits such as the common-source amplifier up to multi-stage, differential, and switched amplifiers

Analog-to-digital converters

If time permits: noise sources in integrated circuits

In the exercises, we will use chip design software to design circuits.

No special prior knowledge is required for this course.

As supplementary literature, I recommend the following book:

Design of Analog CMOS Integrated Circuits by Behzad Razavi

<https://primo.bibliothek.kit.edu>

## **CMOS Technology: Origins and Significance**

The circuits in this course are based on CMOS technology.

CMOS: Complementary Metal-Oxide Semiconductor.

CMOS integrated circuits are one of the most important inventions of the 20th century. This type of circuit has enabled powerful microprocessors and computers.

The foundation of modern CMOS (Complementary Metal-Oxide-Semiconductor) technology begins not with CMOS itself, but with the invention of the transistor in 1947 by John Bardeen, Walter Brattain, and William Shockley at Bell Labs.

Their point-contact transistor—made of germanium—replaced bulky, power-hungry vacuum tubes and earned them the 1956 Nobel Prize in Physics.

In 1958, Jack Kilby at Texas Instruments demonstrated the first integrated circuit (IC) using germanium and discrete components. Months later, in 1959, Robert Noyce at Fairchild Semiconductor invented the planar IC using silicon and photolithography—laying the groundwork for scalable semiconductor manufacturing.

[Mohamed Atalla](#) and [Dawon Kahng](#) (dah-wuhn) proposed a silicon MOS transistor in 1959<sup>[17]</sup> and successfully demonstrated a working MOS device with their Bell Labs team in 1960.

The CMOS process was presented by Fairchild Semiconductor's Frank Wanlass and Chih-Tang Sah (sa dztan) at the International Solid-State Circuits Conference in 1963. Wanlass later filed US patent 3,356,858 for CMOS circuitry and it was granted in 1967. <https://patents.google.com/patent/US3356858A/en>

They proposed pairing n-channel and p-channel MOSFETs in a complementary symmetry.

Dec. 5, 1967

F. M. WANLASS

3,356,858

LOW STAND-BY POWER COMPLEMENTARY FIELD EFFECT CIRCUITRY

Filed June 18, 1963

5 Sheets-Sheet 5

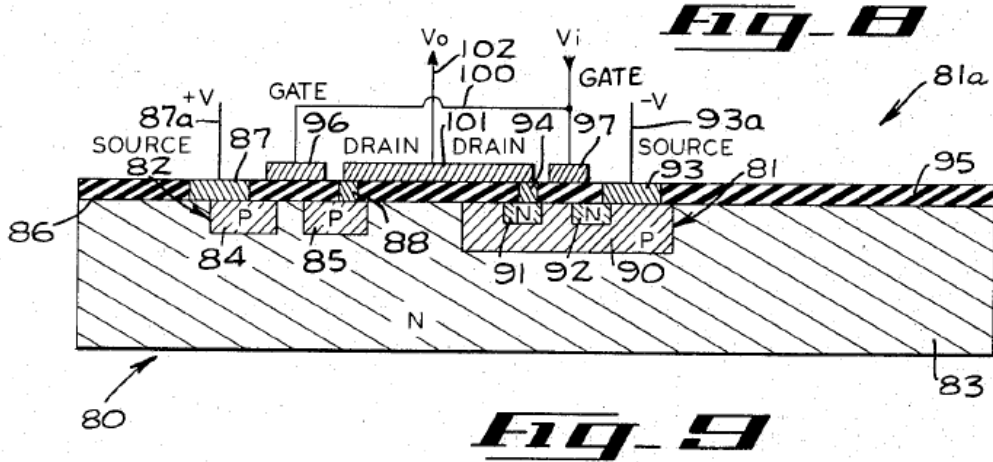


Figure 2: Drawing from the CMOS patent by F. N. Wanlass

Why CMOS was revolutionary:

Static power was near zero because one transistor is always off in steady state. This made CMOS ideal for battery-powered and dense circuits—though early CMOS was slow and expensive.

CMOS technology is particularly suitable for digital circuits:

CMOS components, based on field-effect transistors (FETs), are power-efficient and compact.

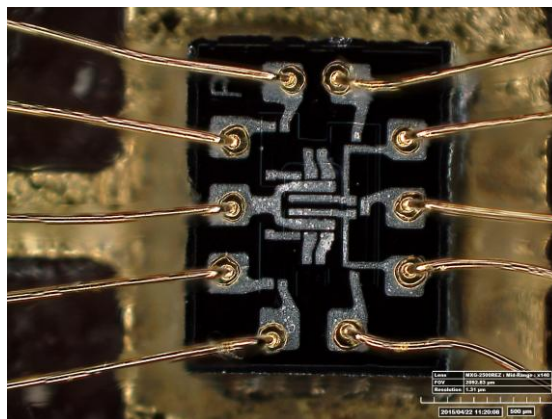


Figure 3: One of the first integrated circuits.

<https://airandspace.si.edu/stories/editorial/apollo-guidance-computer-and-first-silicon-chips>

## History of CMOS technology development

CMOS was commercialised by [RCA](#) in the late 1960s. RCA adopted CMOS for the design of [integrated circuits](#) (ICs), developing CMOS circuits for an Airforce computer in 1965 and then a 288-bit CMOS [SRAM](#) memory chip in 1968.<sup>[24]</sup> RCA also used CMOS for its [4000-series integrated circuits](#) in 1968, starting with a [20 µm semiconductor manufacturing process](#) before gradually scaling to a [10 µm process](#) over the next several years.<sup>[27]</sup>

CMOS technology was initially overlooked by the American [semiconductor industry](#) in favour of NMOS, which was more powerful at the time. However, CMOS was quickly adopted and further advanced by Japanese semiconductor manufacturers due to its low power consumption, leading to the rise of the Japanese semiconductor industry

The first mass-produced CMOS consumer electronic product was the [Hamilton Pulsar](#) "Wrist Computer" digital watch, released in 1970.<sup>[31]</sup> Due to low power consumption, CMOS logic has been widely used for [calculators](#) and [watches](#) since the 1970s.<sup>[32]</sup>

The [earliest microprocessors](#) in the early 1970s were PMOS processors, which initially dominated the early [microprocessor](#) industry. By the late 1970s, NMOS microprocessors had overtaken PMOS processors.<sup>[33]</sup> CMOS microprocessors were introduced in 1975, with the [Intersil 6100](#),<sup>[33]</sup> and RCA [CDP 1801](#).<sup>[34]</sup>

CMOS overtook [NMOS logic](#) as the dominant MOSFET fabrication process for [very large-scale integration](#) (VLSI) chips in the 1980s. CMOS has since remained the standard fabrication process for MOSFET [semiconductor devices](#).

**1982: Intel 80286** – First mainstream CPU with CMOS support chips

**1985: Intel 80386** – Full 1.5 µm CMOS process

**1989: Intel 80486** – 1 µm CMOS, on-chip cache, FPU



## 1990s – Deep Submicron Era

- Marked by rapid scaling of CMOS technology and exponential growth in performance.
- Key milestones:
  - **1990:** Intel 486DX – 0.8  $\mu\text{m}$ , 1.2 million transistors
  - **1993:** Pentium – 0.5  $\mu\text{m}$ , 3.1 million transistors
  - **1995:** Pentium Pro – 0.35  $\mu\text{m}$ , 5.5 million transistors
  - **1997:** Pentium II – 0.25  $\mu\text{m}$ , 7.5 million transistors
  - **1999:** Pentium III – 0.18  $\mu\text{m}$ , 28 million transistors

**Key trend:** Continuous transistor scaling led to higher clock speeds and integration density, but also increased power consumption.

## 2000s – The Power Crisis

- Planar CMOS technology began to reach its physical and thermal limits.
- Power density became a major design constraint.
- Emphasis shifted from frequency scaling (“faster clocks”) to power efficiency and multi-core architectures.

**Challenge:** Managing heat and leakage currents became critical in high-performance chips.

## 2010s – The 3D Revolution

- Introduction of FinFET (Fin Field-Effect Transistor) technology.
- Transition from planar to 3D transistor structures improved gate control and reduced leakage.
- Enabled further scaling beyond 22 nm nodes.

**Impact:** FinFETs revitalized Moore’s Law by improving performance and energy efficiency.

## 2020s – Beyond Planar

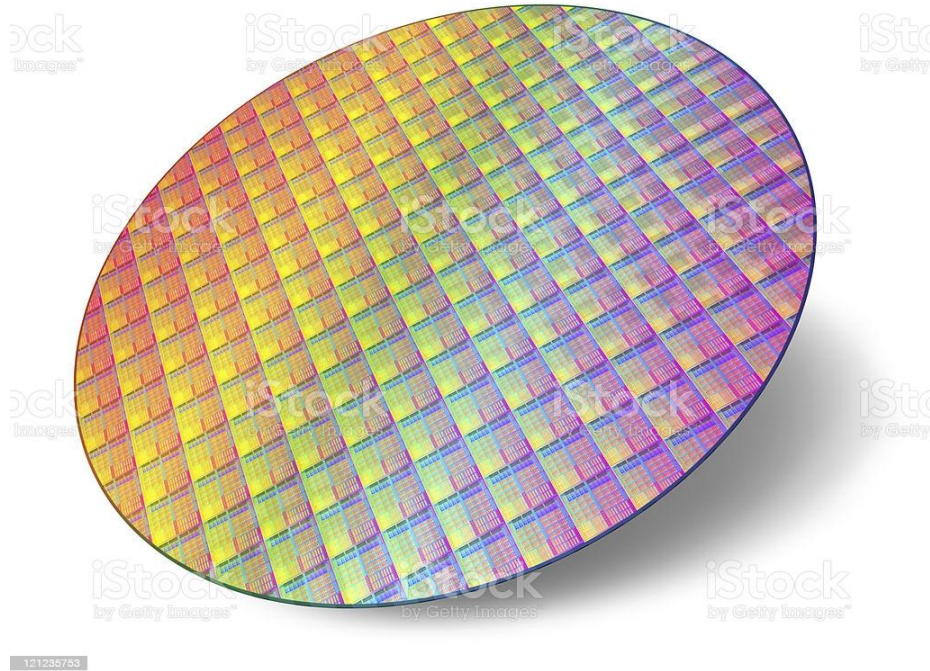
- Emergence of Gate-All-Around (GAA) and nanosheet/nanowire transistor architectures.
- These next-generation devices continue the trend toward better electrostatic control and scalability.
- Research explores 2D materials (e.g., MoS<sub>2</sub>, graphene) and quantum-based device concepts for future integration.

The industry moves “beyond CMOS,” exploring new materials, device structures, and 3D integration technologies.

## IC Manufacturing

Since this course deals with integrated circuits, I will briefly cover their manufacturing process. Microchips are produced on silicon wafers in a process similar to image printing (e.g., lithography).

Wafers typically have a diameter of 200 mm or 300 mm.



*Figure 4: Wafer with Recticles*

**The layers of a chip:**

**Silicon regions** (mono- and polycrystalline)

**Insulators** ( $\text{SiO}_2$  and other materials)

**Vias** (tungsten, aluminum)

**Metal connections** (aluminum and copper)

These layers are created using processes such as epitaxy, chemical deposition, and oxidation and are patterned by etching (wet chemical, plasma, or ion etching). Photoresist is used to protect areas that should not be etched.

Photoresist is patterned using UV light (exposed and developed). The template for this patterning is called a mask.

Silicon regions are doped by diffusion or ion implantation. Masks ( $\text{SiO}_2$ ) are also used here, structured with photoresist.

The fabrication of a wafer requires about 400 individual steps and at least 30 masks.

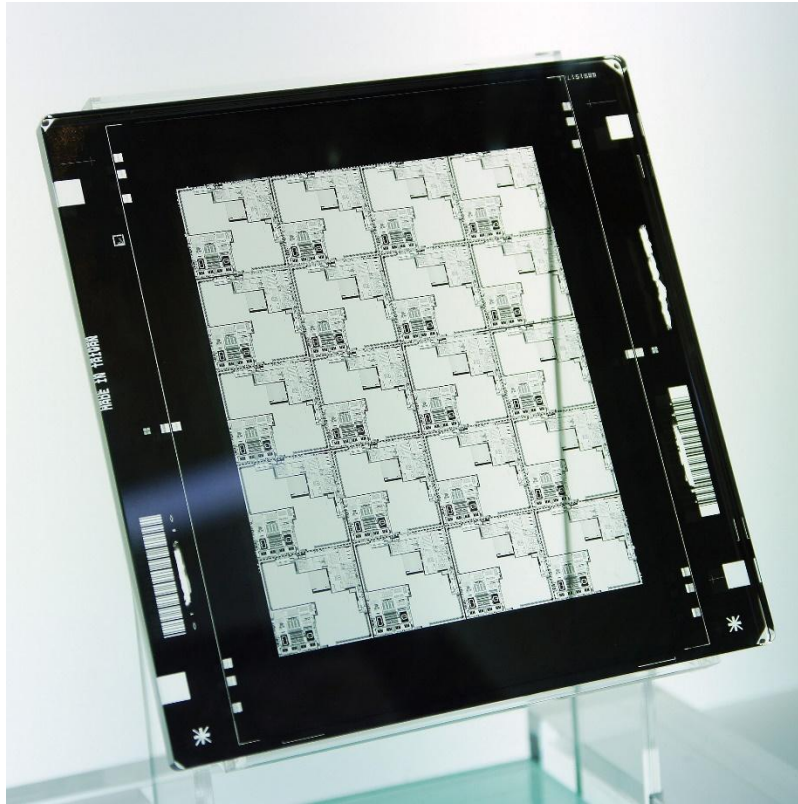


Figure 5: Mask for Photolithography <https://en.wikipedia.org/wiki/Photomask>



Figure 6: Stepper (Projector) <https://www.asml.com/en/products/duv-lithography-systems/twinscan-nxt2000i>

The masks are projected onto silicon using projectors (steppers) with, for example, 4× reduction.

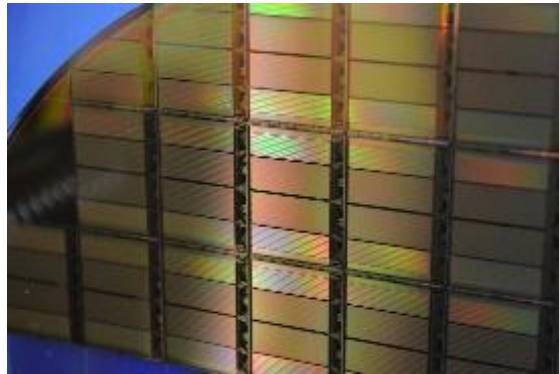
The size of the image is limited to about 2.5 cm × 2.5 cm.

This is also the maximum chip size.

The image on the mask is called a reticle.

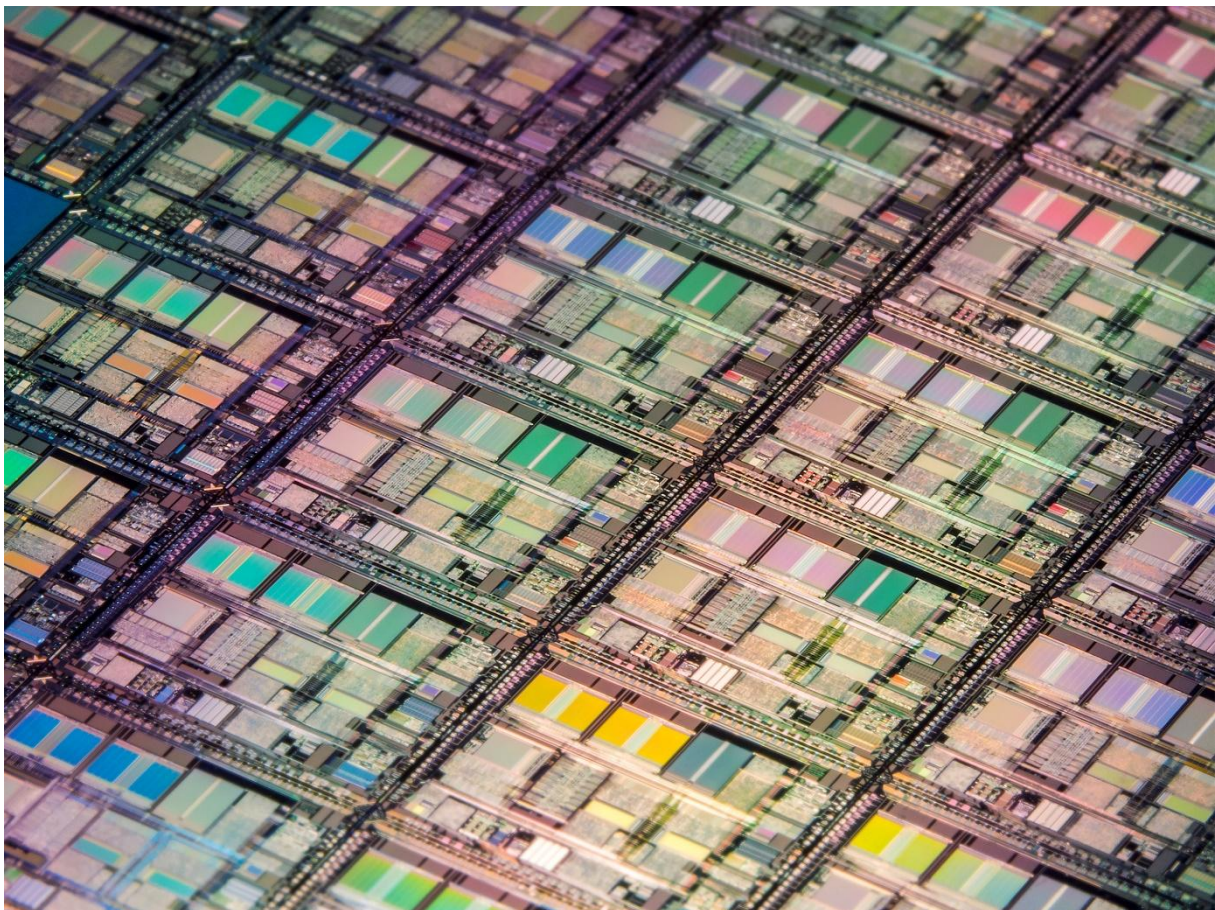
On a wafer, the mask is projected multiple times with a fixed offset, so there are multiple identical reticles.

A well-known manufacturer of lithography equipment is ASML (Netherlands).

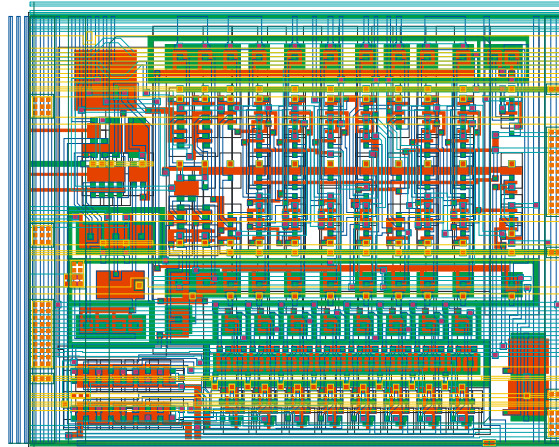


*Figure 7: CMOS Wafer (KIT-ADL)*

In a reticle, multiple chip designs are often grouped together to optimize wafer usage during fabrication.



*Figure 8: Reticles with Chips.* <https://www.renishaw.com/en/advanced-position-encoders-in-photolithography--42654>



*Figure 9:* Technical drawing of mask layers – Layout

## **Chip design**

Chip design is a process that starts with the specification of an electronic device and ends with the creation of the layout.

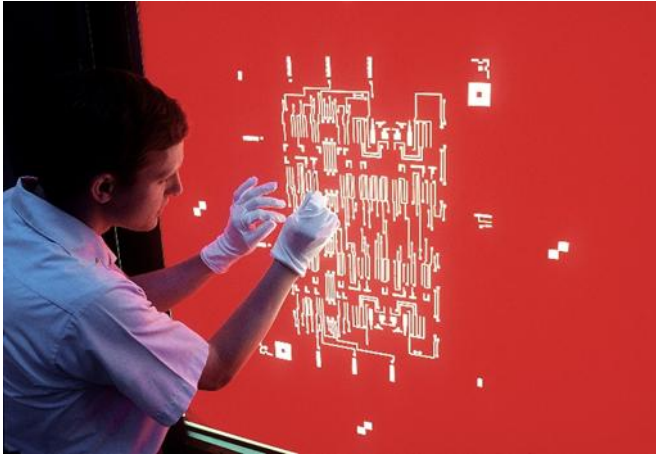
The chips are then manufactured by a chip foundry, subsequently integrated into a system (chip packaging), characterized, and, if necessary, a new version is designed.

### **Evolution of Analog IC Design Tools (1970s–1980s)**

In the beginning, there were no software tools—chip design was entirely manual. Engineers hand-drew and calculated schematic diagrams on paper. Layouts were created by cutting rubylith (a red translucent film) to form photomasks, a labor-intensive process prone to errors.

A breakthrough came in 1971 with Calma's Graphic Design System (GDS), evolving to GDSII in 1978—a digital file format for storing and exchanging mask layouts. GDSII became the de facto standard for full custom designs, including analog, and is still used today in tools like Virtuoso for outputting layouts to foundries.

GDSII was designed to drive vector photoplotters that exposed film to create photomasks — a direct evolution from rubylith.



*Figure 1: A technician makes small-detail corrections of a circuit image on a large Rubylith. The image will be copied, miniaturized, and utilized in making computer chips. Wikipedia*

Simulation also emerged: SPICE (Simulation Program with Integrated Circuit Emphasis), developed at UC Berkeley in 1973, allowed engineers to model analog circuit behavior at the transistor level before fabrication.

The 1980s transformed electronic design automation EDA into a commercial industry, driven by the need for more complex chips.

Companies such as Mentor Graphics were founded, offering tools for schematic capture, simulation, and layout. These supported analog flows through graphical interfaces for custom layouts.

Company ECAD introduced DRaCula for Layout vs. Schematic (LVS) verification, ensuring layouts matched schematics—a must for error-free analog designs.

The rise of ASICs (Application-Specific Integrated Circuits) and fabless models (TSMC founded in 1987) amplified demand for tools, blending analog and digital.

Hardware description languages like VHDL (1981) and Verilog (1984) allowed mixed mode simulation.

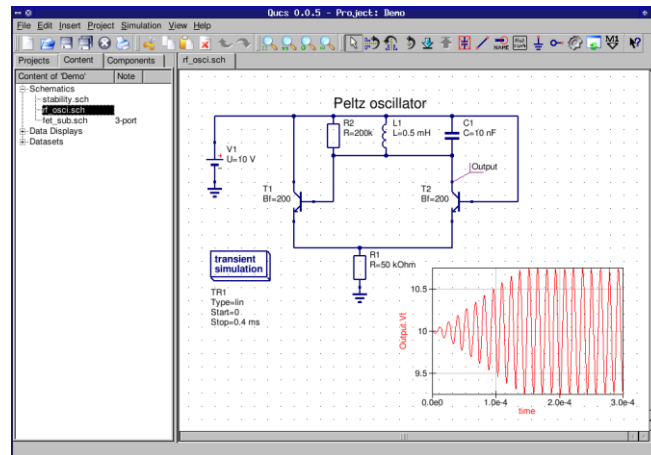


Figure 2: SPICE

In 1988, ECAD and SDA merged to form Cadence Design Systems, joining LVS and analog tools under one roof. This merger marked the EDA "Big Three": Cadence, Synopsys (founded 1986 for synthesis), and Mentor Graphics (now belongs to Siemens).

In 1990s, EDA tools integrate front-end (schematic/simulation) and back-end (layout/verification) flows, essential for analog full custom design where iteration between schematic and layout is frequent.

Cadence's Virtuoso emerged in 1991 as a layout editor for mask designers. It addressed the need for precise, hierarchical layout in analog ICs, supporting GDSII output and integrating with SPICE simulators. Over the decade, Virtuoso evolved into a full suite: adding schematic capture, parasitic extraction, and mixed-signal simulation. This allowed designers to handle RF, analog, and custom digital in one environment, reducing errors in full custom flows

Other tools complemented this: Mentor's IC Station for layout, and Synopsys' tools for verification. But Virtuoso became synonymous with analog design due to its user-friendly interface and PDK (Process Design Kit) support from foundries.

Modern analog tools like Virtuoso integrate AI for optimization—e.g., auto-routing sensitive analog paths or predicting parasitics.

In this course, we use the Cadence software suite (<https://www.cadence.com>). Cadence includes many tools:

**Schematic and Layout Editor:** Virtuoso

**Simulator:** INCISIV and MMSIM

**Layout Verification:** Assura

Layout versus Schematic (LVS)

Design Rule Check (DRC)

(Alternative: Mentor – Calibre DRC/LVS)

We also need data from the chip manufacturer, such as transistor models, pre-designed blocks, or LVS/DRC rule sets. This data is provided as a Process Design Kit (PDK).

Note: Cadence requires a paid license.

### **Foundry & Manufacturing Processes**

It is important to choose the right (technology) process or chip manufacturer for a chip design project.

The most well-known manufacturers are: TSMC, UMC, GlobalFoundries. In Germany: X-Fab. Our group also works with AMS, LFoundry, and IHP.

A semiconductor process in semiconductor technology refers to a sequence of processes used to fabricate semiconductor devices and microelectronic circuits.

Each manufacturer often offers multiple processes (sometimes multiple manufacturers offer the same process).

This could be, for example:

A CMOS process with extra components for analog design or optical sensors

A high-voltage CMOS (HV-CMOS) process

An SOI or BiCMOS process

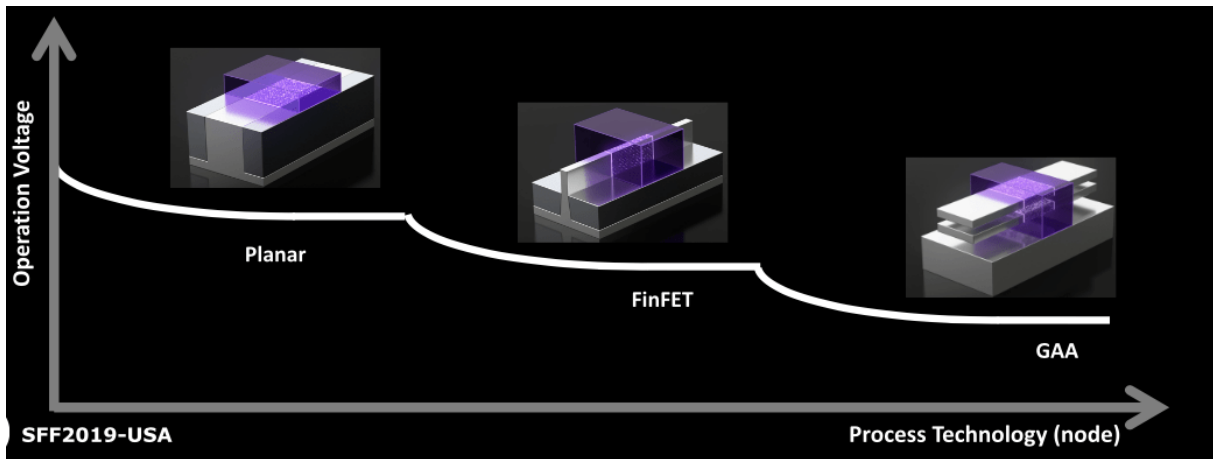
The newest processes include FinFET, Fully Depleted SOI, or Nanowire Gate-All-Around processes.

All processes are also classified by feature size / process node, e.g.: 0.35  $\mu\text{m}$ , 0.18  $\mu\text{m}$ , 0.13  $\mu\text{m}$ , 0.11  $\mu\text{m}$ , 90 nm, 65 nm, 55 nm, 40 nm, 28 nm, 22 nm, 16 nm, 12 nm, 7 nm, 6 nm, 5 nm

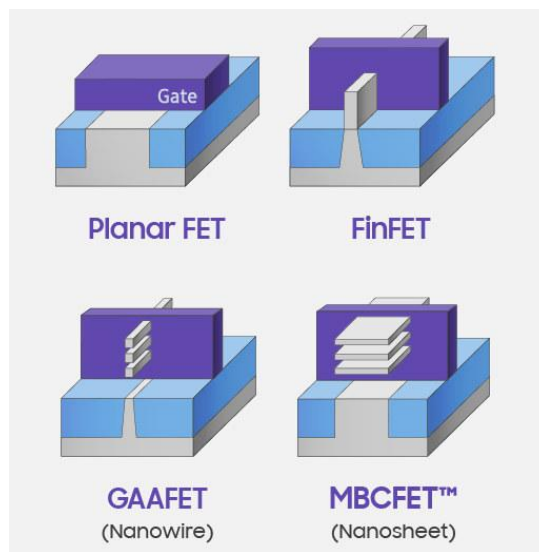
<https://de.wikipedia.org/wiki/Technologieknoten>

Smaller nodes are more modern, more expensive, and analog design is more challenging.

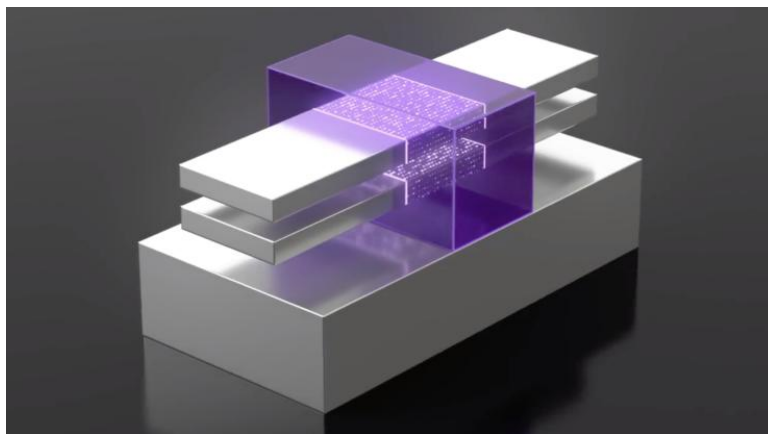
The chip manufacturers are also called foundries or vendors.



<https://semiengineering.com/5nm-vs-3nm/>



<https://www.cnx-software.com/2019/05/17/mbcfet-process-technology-3nm-processors/>



<https://wccftech.com/samsung-announces-3nm-mbcfet-process-5nm-production-in-2020/>

Figure 10: Different Transistor-types

## **Europractice**

Some foundries can be contacted directly. Others work only with larger customers. There are organizations that mediate between smaller customers and foundries – one of them is Europractice.

<https://europractice-ic.com/>

Europractice represents chip manufacturers and provides support. KIT is a member of Europractice.

For small quantities and small chips, it is not practical to manufacture a full set of masks and finance a wafer production.

In a 180 nm process, an engineering run costs about €150k.

In a 65 nm process, the cost is about €1 million.

Europractice offers Multi-Project Wafer (MPW) runs:

In MPW runs, many customers share the reticle area. A customer receives about 40–100 chips at a price starting from about €1k/mm<sup>2</sup> of area (example: 180 nm technology). We often order our chips via MPW runs.

## **Design Kit**

After selecting a process, we need to obtain the simulation models and layout rules and import them into the chip design software. Transistors differ from one process to another, and transistor models are complex. An example of a MOSFET model is BSIM.

We also need special libraries that are integrated into the chip design software, such as Cadence.

Such a library containing technology files is called a Process Design Kit (PDK).

## **Design Flow**

The sequence of design steps — the design flow — is precisely defined in chip design.

We distinguish between the analog and digital design flows.

The design steps are shown in the figure, and we will describe them here in more detail.

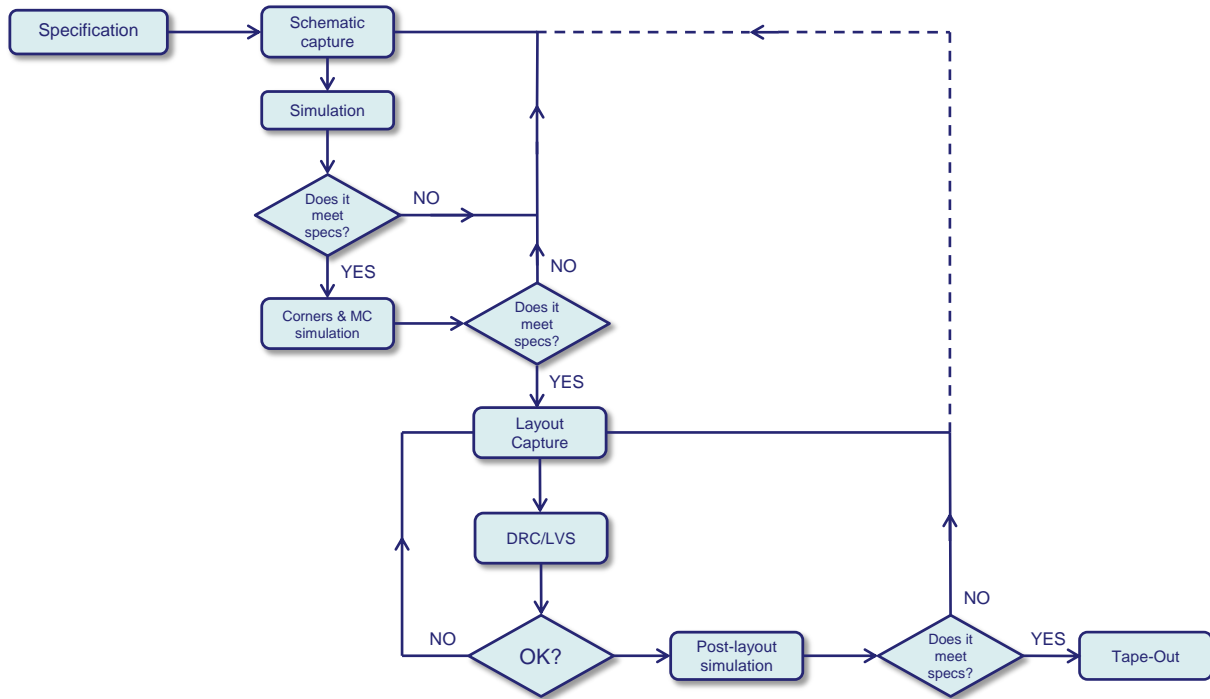


Figure 11: Analog Design-Flow

### Schematic capture

In the analog design flow, the first step is the creation of the schematic. The schematic is drawn using the schematic editor. The basic building block is the transistor.

We also use capacitors, resistors, and diodes, which can also be implemented on a chip.

Since integrated circuit schematics are complex, it is helpful to build a modular structure. Cadence supports this. From each schematic, a symbol can be generated. This allows the schematic to be used in other schematics.

To generate a symbol, inputs and outputs must be defined. A symbol has the same inputs and outputs as its schematic.

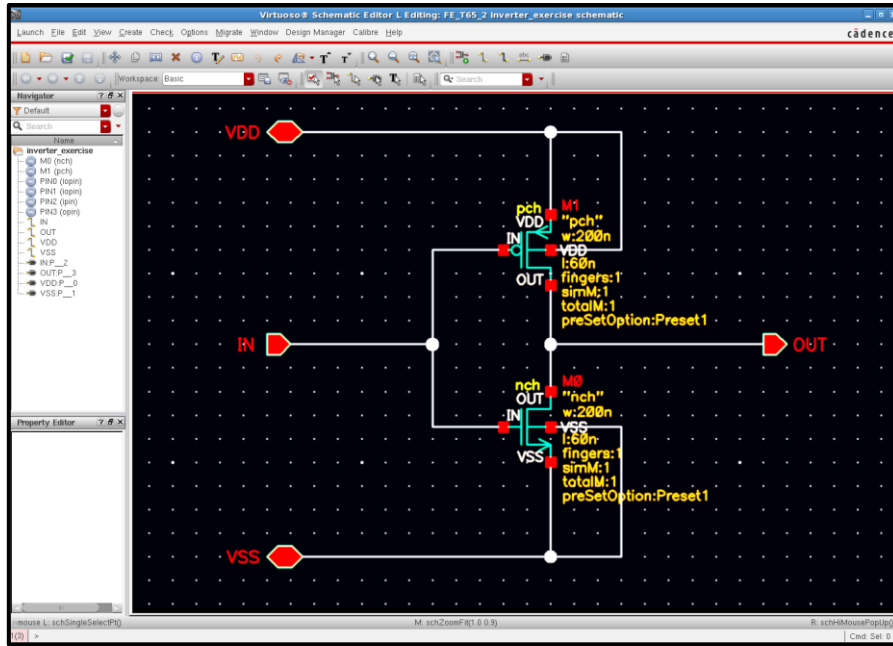


Figure 12: Schematic editor

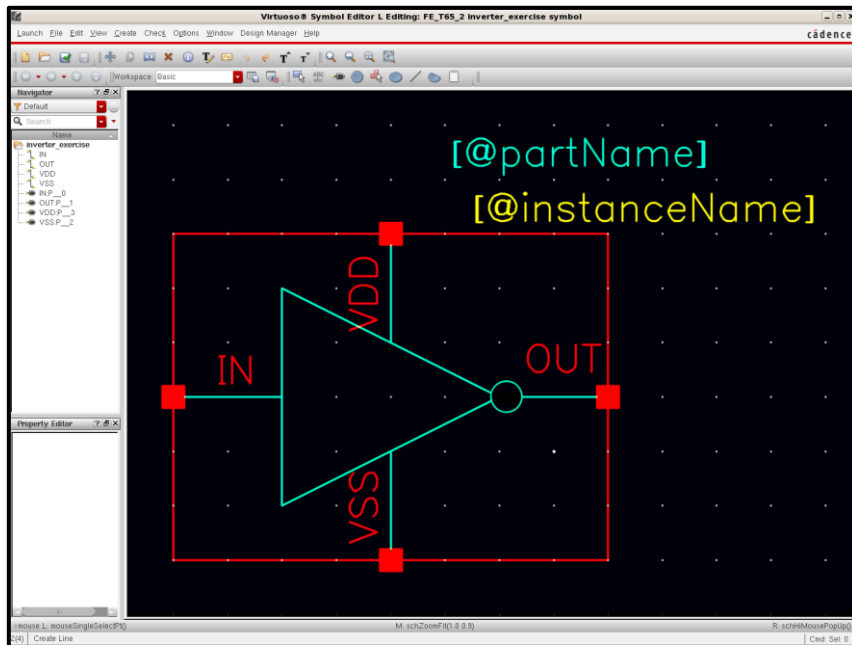


Figure 13: Symbol

## Simulation

The circuit can be simulated. We will learn more about this in the exercises.

There are various simulation tools for analog, mixed-mode, or digital simulation. Analog simulators can perform:

DC analysis

AC analysis

Large-signal analysis in the time domain (transient simulation)

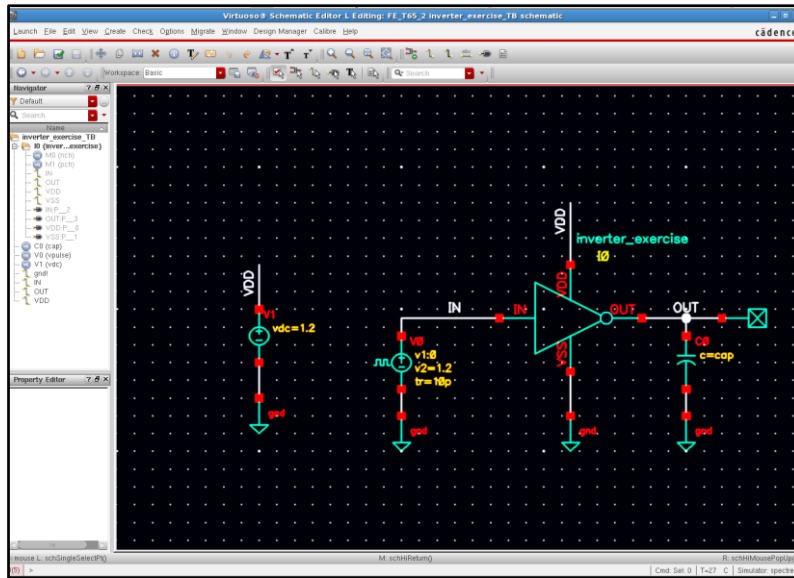


Figure 14: Test-bench (analog Simulation)

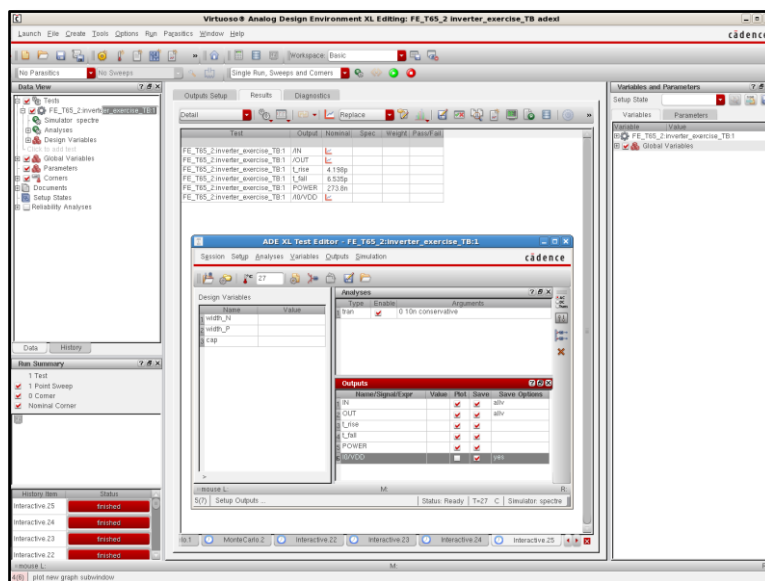


Figure 15: Analog simulator GUI

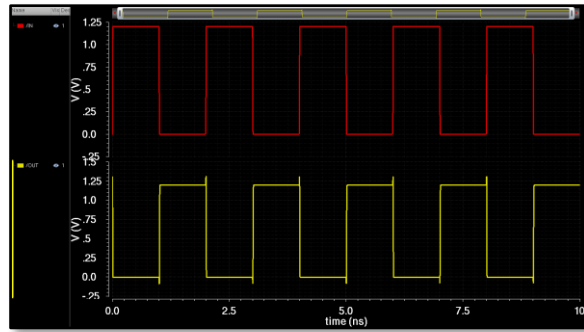


Figure 16: Result of a transient Simulation

It is possible to simulate noise in both the frequency and time domains. It is also possible to simulate parameter variations.

Noise: We consider a single component and examine how currents and voltages vary over time in the absence of signals. This is caused by the thermal motion of electrons or electron trapping.

Mismatch: We consider multiple identical components and examine the statistical variation of currents/voltages from one component to another.

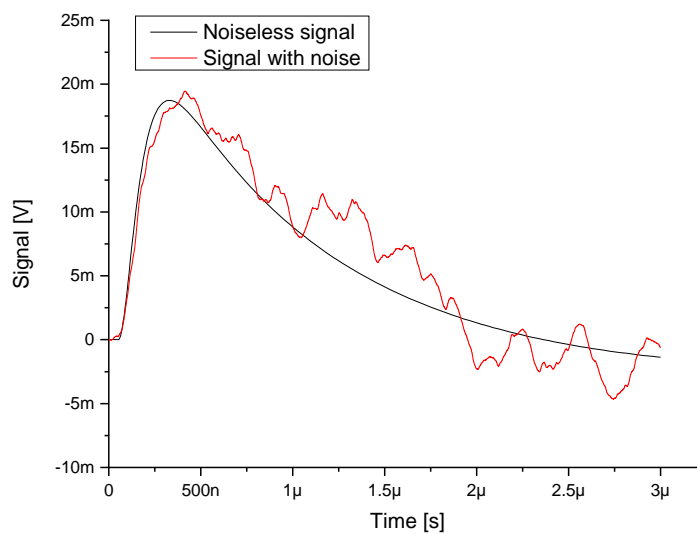


Figure 17: Noise simulation

## Layout

Once we are satisfied with the simulation results, we start layout design. The layout consists of multiple drawings, representing the mask layers used for fabricating transistors and metal connections.

In analog design, layouts are often drawn “by hand” (manually clicked together). This is done using the layout editor, whose graphical interface resembles a CAD program. You can draw polygons, paths, and other structures.

There are additional features:

Structures can be grouped and used as blocks

A hierarchy can be built

A group in layout software is similar to a class instance in programming: many instances (objects) of the same type can exist in a design

In Cadence, these “classes” are called cells

A cell has multiple views, e.g., schematic view or layout view

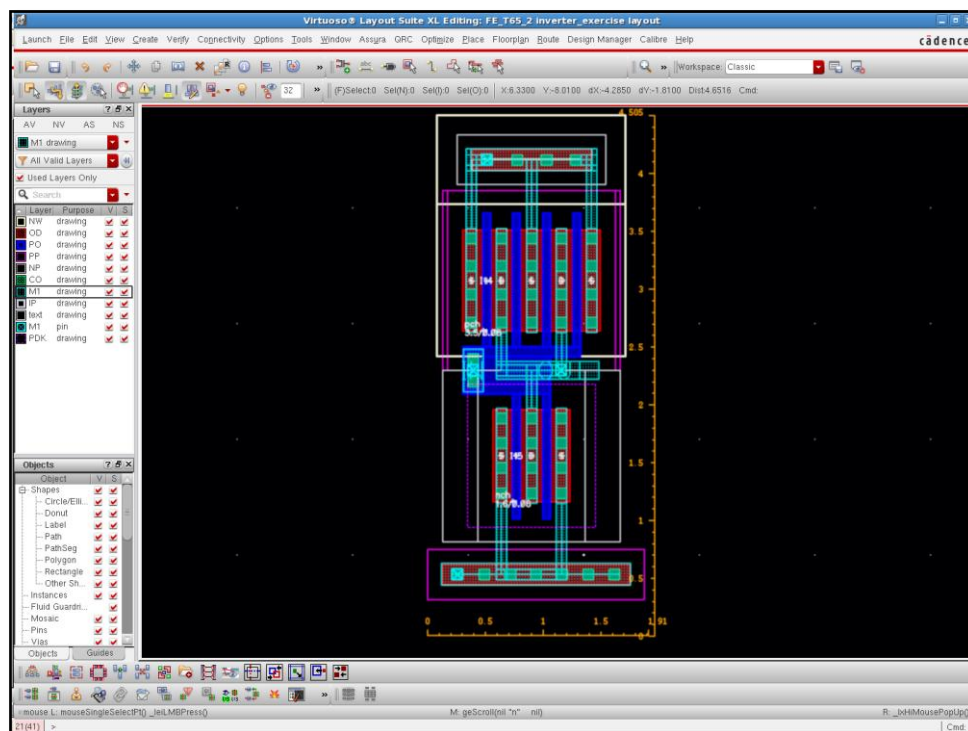


Figure 18: Layout Editor

A semi-automatic generation of the layout from the schematic is also possible.

When drawing, you must follow the layout rules – for example, transistors cannot be smaller than what the technology allows.

It is possible to check if layout rules are violated in the design. This verification uses the layout rules and is called a DRC (Design Rule Check).

It is also possible to extract a netlist from a layout. This allows the tool to check whether the layout matches its schematic. This is called LVS (Layout versus Schematic) check.

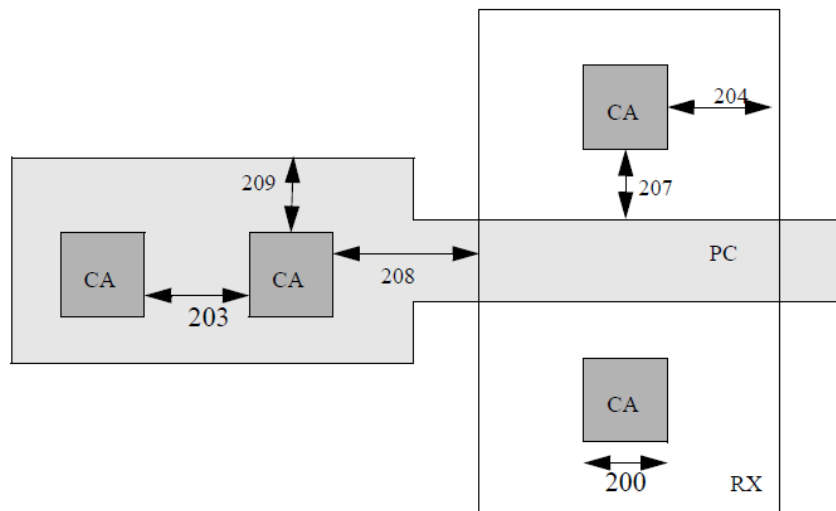


Figure 19: Design rules

*Your Virtuoso layout becomes silicon when it becomes GDSII.*

GDSII (Graphic Design System II) is a binary file format for representing 2D geometric layout data of integrated circuits.

**Binary format:** It is a binary file, which makes it difficult for humans to read directly, but makes it compact and efficient.

**Hierarchical structure:** It represents layout data in a hierarchical manner, with structures nested inside other structures.

**Layout information:** A GDSII file contains the geometric patterns, text labels, and other layout data, including information about layers, shapes, and paths.

**Final output:** It is the final output of the IC design cycle, also known as the "tape-out" database.

## Structuring in analog design

Proper structuring is helpful in circuit design.

Almost every analog circuit is based on a few fundamental components. Examples include:

Common-source amplifier (source configuration)

Source follower (drain configuration)

Cascode (gate configuration)

Current mirror

Differential amplifier

These fundamental components are built from transistors.

More complex circuits, such as operational amplifiers or analog-to-digital converters (ADCs), are composed of these fundamental components. Systems are composed of circuits.

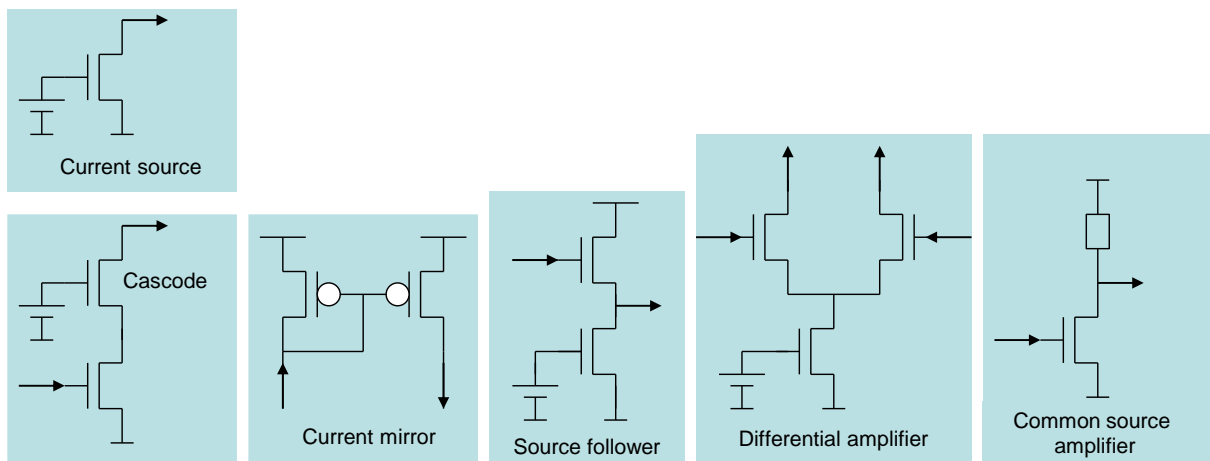


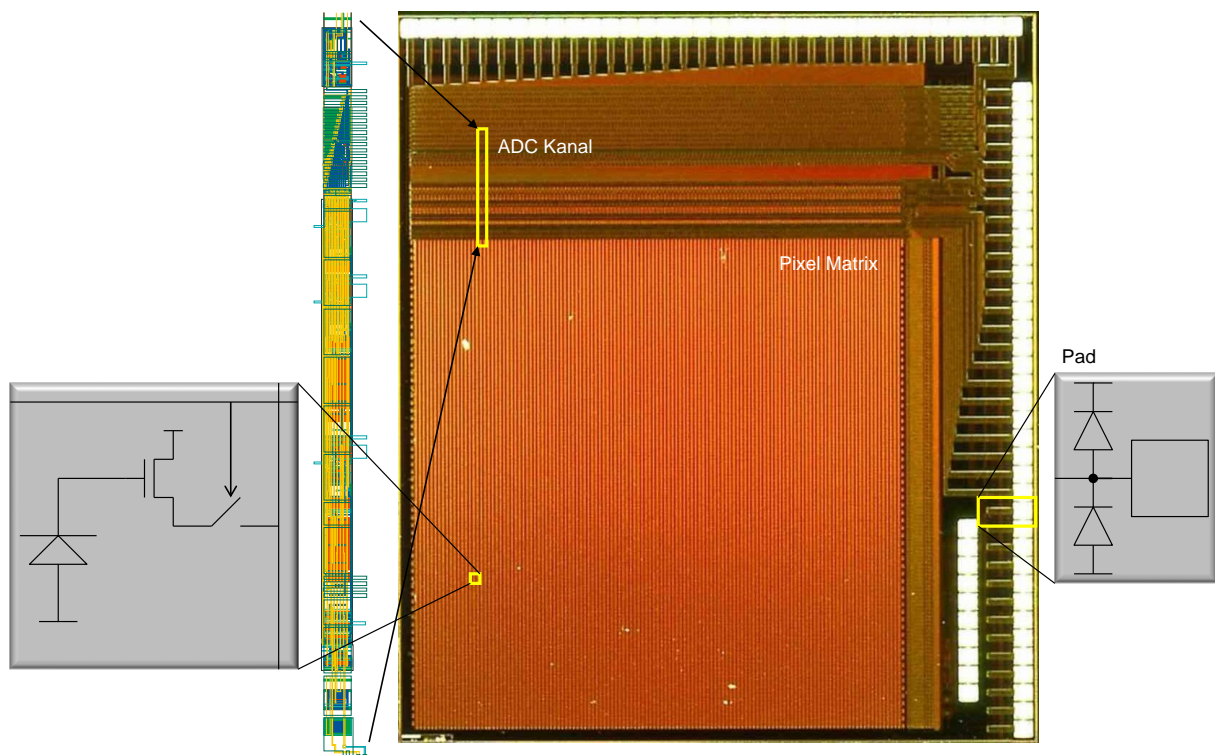
Figure 20: Basic components

## Structure of one microchip

A chip consists of many interconnected systems.

Using cells and instances in Cadence allows us to reuse the same circuits multiple times. Schematics and layouts have the same hierarchical structure.

For example, consider a pixel sensor. The light sensors – pixels – are based on diodes. These diodes are reverse-biased.



*Figure 21: Photo of a pixel sensor chip with important components*

The amplifiers in pixels are based on simple components – for example, a source follower. The pixels are organized in columns, and the columns form the matrix. This intuitive hierarchy is used in both the schematic and the layout.

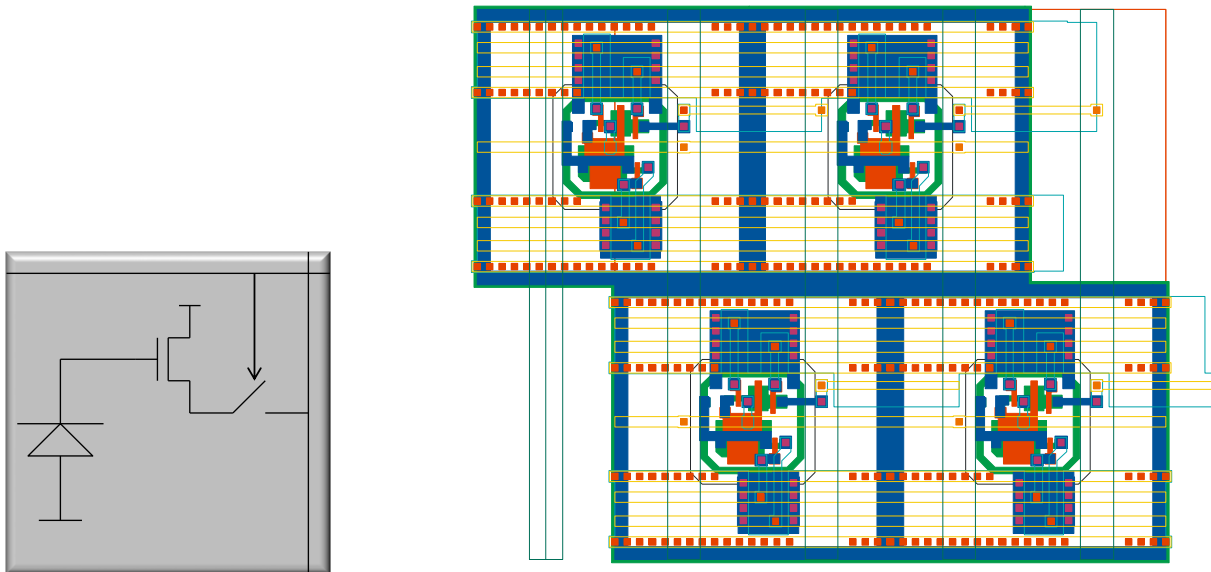


Figure 22: Pixel – Schematics and layout

We can therefore first design a single pixel as a circuit, then simulate it, draw the layout, and perform DRC/LVS checks.

After that, we can build a column and finally the entire matrix.

**It is advantageous to reduce the number of different layouts and schematics (i.e., the number of ‘classes’ or cells) in a design.**

Why? Because if we later make a change in the pixel layout, that change will be automatically applied to every pixel cell — we won’t have to repeat the modification multiple times.

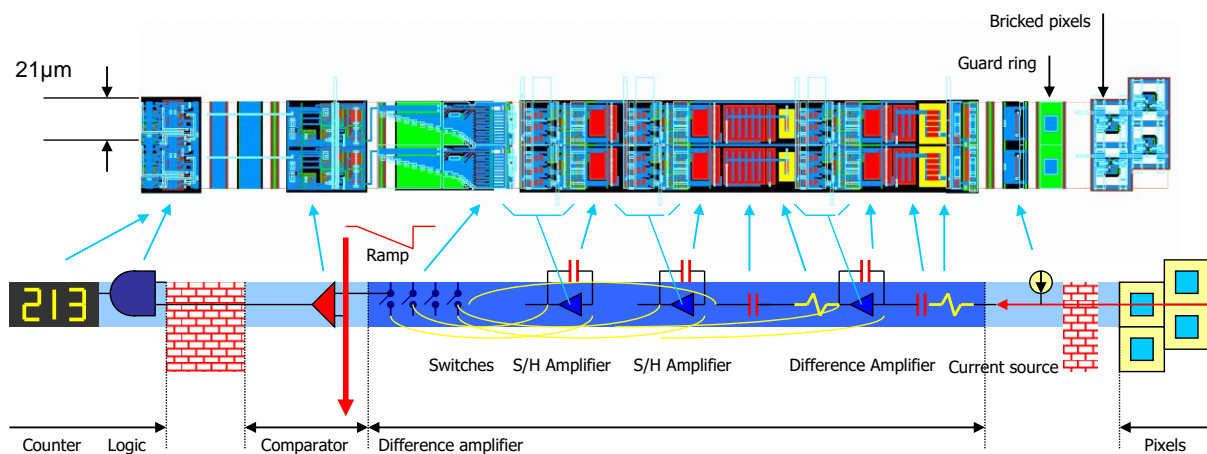


Figure 23: ADC

## ADC

The sensor chip contains ADCs that digitize the pixel signals (one ADC per column). These ADCs are located on the chip periphery.

An ADC is a system composed of multiple components, e.g.:

Amplifier

Comparator

DAC

Digital control circuitry

On a pixel sensor, we typically have about 1000 such ADCs.

## Digital part

Often, there is also a digital circuit that compresses the ADC signals and sends them out of the chip in a suitable format.

The digital components consist of logic standard cells (flip-flops, AND, OR, etc.), which are often provided by design companies.

A digital circuit can be assembled manually from these components or designed using a synthesis tool from HDL code.

Chips that contain both analog and digital components are called *mixed-mode chips* (or *mixed-signal chips*).

It is also possible to perform *mixed-signal simulation*, where the analog circuits are simulated in the analog domain (by numerically solving current and voltage equations), while the digital circuits are simulated based on logical functions.

The simulators include interfaces between the digital and analog blocks, which convert binary signals (0 and 1) into physical signals (voltages).

## Pads

A chip also has I/O contacts (pads, pins). These pads are connected to a PCB or the chip package using devices called wire bonders. A simple solder connection is not possible, as the pads are too small.

The chip pads include electrostatic discharge (ESD) protection circuits. They protect against overvoltages that could occur from static electricity and potentially damage the gate oxide.

## Discrete- vs. Integrated Circuits

Design of analog integrated circuits is based on the same principles and techniques as designing circuits with discrete components. There are, however, some differences:

When designing discrete circuits on a PCB, one must choose the right components from thousands of commercial options. In analog CMOS chip design, circuits are based on only two components: the NMOS and PMOS field-effect transistors.

The MOSFET is a versatile component: it can function as an amplifier, current source, resistor, capacitor, switch, or diode. Therefore, it is important to understand the transistor models.

Another peculiarity of CMOS design is that resistors and diodes are rarely used. The quality of real resistors on a chip is often quite poor, with values varying by  $\pm 10\%$ . Diodes in forward bias can cause latch-up effects.

Since capacitors in CMOS have good quality and precise capacitance, resistors are often replaced by capacitors, and diodes are replaced by transistors.