Lecture 13

The topics of Lecture 13 are amplifiers with two amplifying stages.

1. Implementation of a voltage amplifier using a single-stage amplifier
2. Implementation of a voltage amplifier / linear regulator using a two-stage amplifier (generic circuit)
3. Voltage amplifier with two amplifier stages, with and without frequency compensation
4. Nyquist stability criterion
5. Miller effect
6. Integrator
7. Linear low-dropout regulator (LDO regulator) implemented with a two-stage amplifier and frequency compensation
8. Additionally, we present the source follower and a voltage amplifier with source follower as its output stage

Two-stage amplifiers

In the previous lectures, we presented, among others, the common-source amplifier and the differential amplifier with a current mirror. Both amplifiers include a voltage-controlled current source in their small-signal model (Figure 1, top). This current source can be converted into a voltage source, as shown in Figure 1 (bottom).

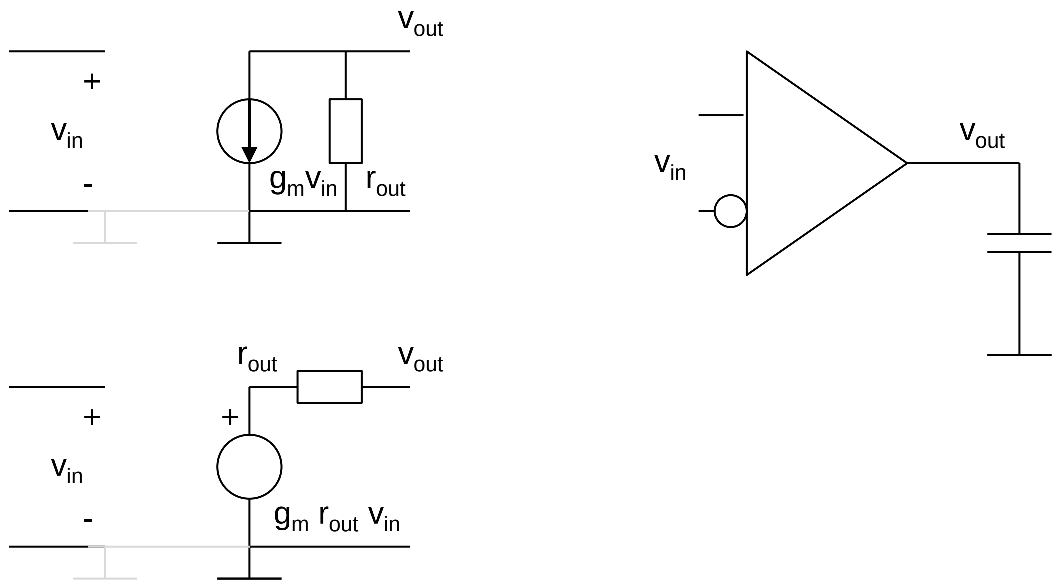
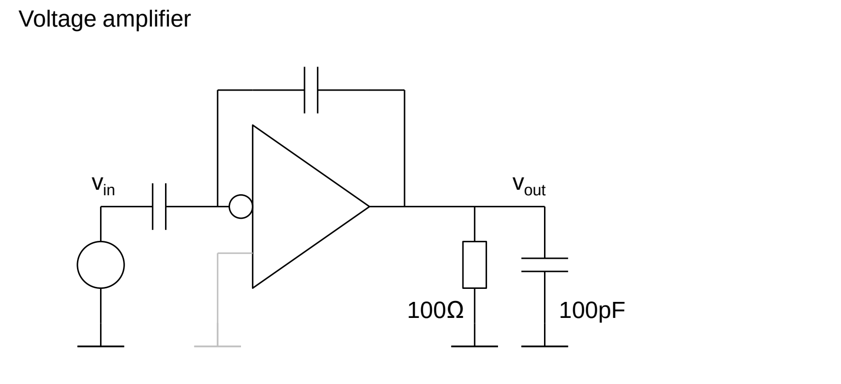


Figure 1: Single-stage amplifier, small signal model with current source (top), small signal model with voltage source (bottom) and symbol (right)

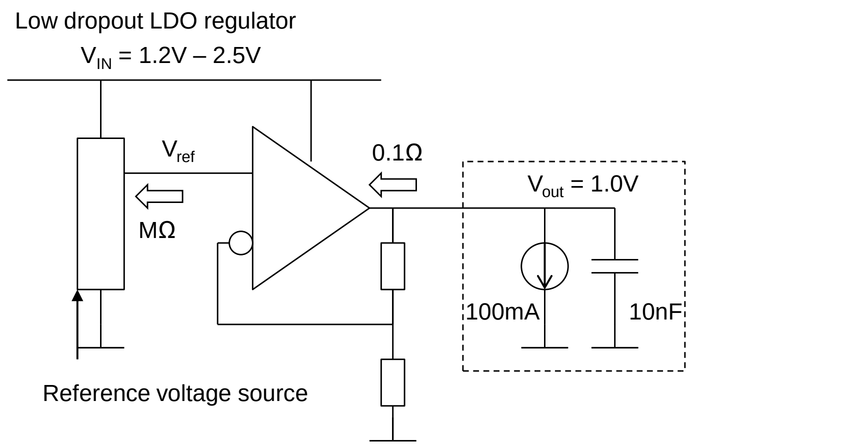
Since the small-signal model contains a single voltage-controlled source, we refer to these amplifiers as **single-stage amplifiers**.

A single-stage amplifier is a good choice when the amplifier has to drive a purely capacitive load that is not very large (≪ pF). This is usually the case when the amplifiers perform on-chip signal processing.

In this lecture, we will introduce amplifiers with two stages.



Voltage amplifier	
Parameter	Wert
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20



LDO regulator	
Parameter	Wert
C_{load}	10nF
I_{load}	0-100mA
r_{out}	0.1Ω

Figure 2: Voltage amplifier and linear regulator and their specifications

Let us introduce two application examples (Figure 2).

1) A voltage amplifier with feedback is to be designed. The amplifier output is connected to a chip pad and must drive a line with a termination resistance of 100Ω. The capacitive load at the pad is 100 pF. The amplifier should have a closed-loop (feedback) gain of 50. The required open-loop gain A_{OL} is 1000.

2) A power supply voltage VDD = 1 V for a chip is to be generated from an imprecise input voltage V_{IN}, where V_{IN} = 1.2 – 2.5V. (The input voltage can be generated by a battery.) A reference voltage generator providing V_{ref} = 1 V (or less) is available. This generator produces a constant voltage V_{ref} that is independent of V_{IN}, and its output resistance is high ($r_{out,ref} \approx$ 1 MΩ). The current consumption of the chip ranges from 0 to 100 mA. The chip can be modeled as a 10 nF capacitor in parallel with a current source. For this application, we use a so-called linear regulator (low-dropout, LDO, linear regulator). The linear regulator is based on a differential amplifier with feedback (non-inverting configuration) and a reference voltage source. The regulator should have an output resistance of 0.1Ω (Figure 2).

In both cases, a single-stage amplifier could be used. However, this would not be the best solution for the reasons discussed below.

To achieve an open-loop gain of 1000, a single-stage amplifier would require a folded-cascode architecture.

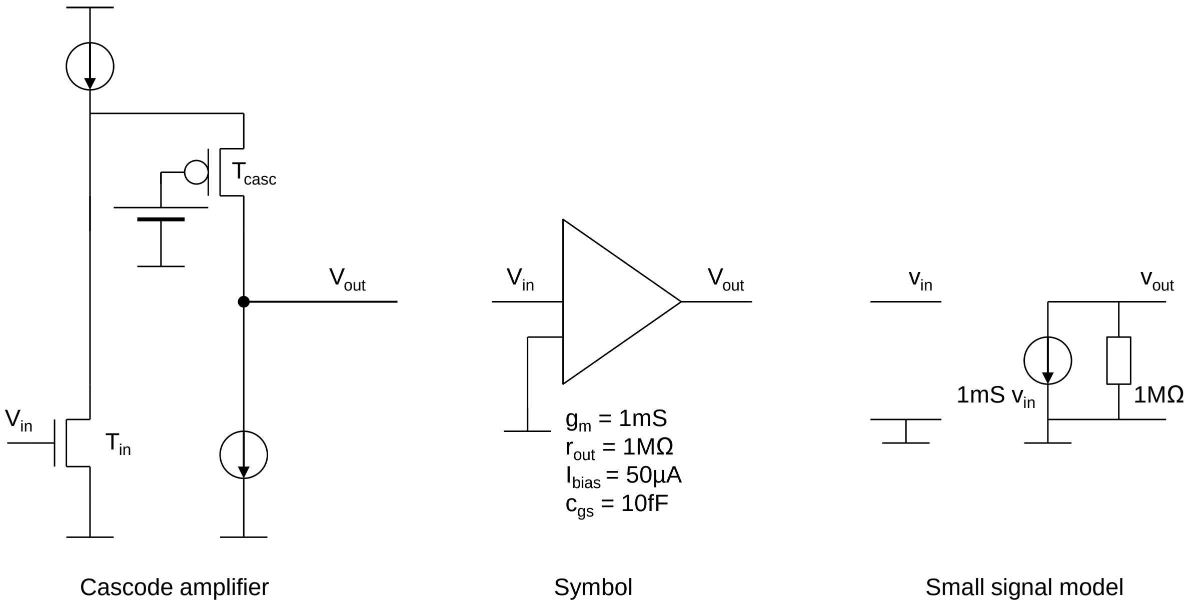


Figure 3: Amplifier with folded cascode - the standard variant with I_{bias} = 50µA

The amplifier presented in Lecture 8 had a transconductance of g_m = 1mS with a bias current of I_{bias} = 50µA. We refer to the amplifier with a bias current of 50µA as the standard amplifier (Figure 3). The standard cascode amplifier has an output resistance of rout = 1MΩ and a voltage gain of $g_m r_{out}$ = 1000.

If this amplifier drives a load resistance of R_{load} = 100Ω, its open-loop gain is reduced to

$A_{OL} = g_m (r_{out} || R_{load}) \sim g_m R_{load} = 0.1$ (Figure 4).

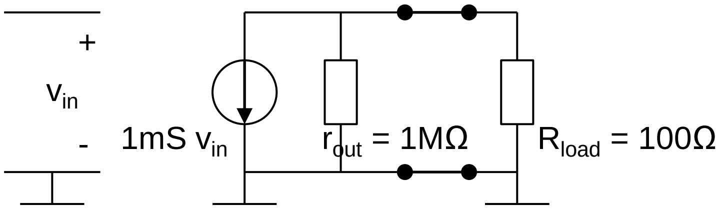


Figure 4: The standard amplifier with load resistance

In order to achieve larger amplification, we have to match the impedances and connect several standard amplifiers in parallel until we reach $r_{out} \sim R_{load}$.

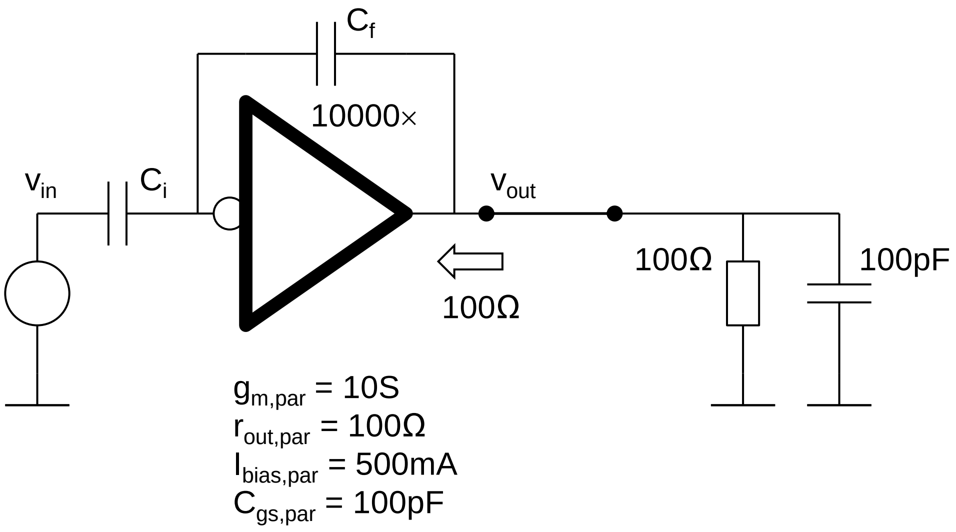


Figure 5: Single-stage amplifier, matching of impedances

If we connect 10000 amplifiers in parallel, the full circuit has the transconductance:

$g_{m,\ par} = 10000 \times g_m = 10$ Si

and the output resistance

$r_{out,\ par} = r_{out} / 10000 = 100\ \Omega$ (Figure 5).

The open loop gain (absolute value) is about:

$|\ A_{OL}\ | = g_{m,\ par}\ (r_{out,\ par}\ ||\ R_{load}) \sim 0.5\ g_{m,\ par}\ R_{load} = 500.$

(One half of the specified) The total bias current is:

$I_{bias,\ par} = 10000 \times I_{bias} = 500$ mA.

We will neglect that the DC current through R_{load} contributes to the transistor bias current and thereby influences its transconductance.

Therefore, we achieve only half of the specified gain and must accept a very large bias current and a large layout area. The large bias current also leads to high power consumption. In addition, the gate capacitance would be large, approximately:

$C_{gs,\ par} = 10000 \times 10$ fF $= 100$ pF.

We could achieve the gain of 50 by choosing $C_i / C_f = 50$. In the case of $C_i << C_{gs,\ par}$ following applies:

$$|\beta A_{OL}| = \frac{C_f}{C_i + C_{gs,par} + C_f}|A_{OL}| \sim \frac{1}{1+\frac{C_{gs,par}}{C_i}}\frac{C_f}{C_i}|A_{OL}| \ll \frac{C_f}{C_i}|A_{OL}| = 10$$

This is small. In this case the closed loop gain (gain with feedback) would the strongly depend on A_{OL}, because the fraction of Mason's gain formula

$$A_{FB} = \frac{A_{IN}A_{OL}}{1+|\beta A_{OL}|}$$

the term + 1 cannot be neglected with respect to $|\beta A_{OL}|$.

For this reason, let us chose:

$C_i = C_{gs,par} = 100$ pF und $C_f = 2$pF.

It follows:

$$|\beta A_{OL}| = 5$$

The rise time of the step response is given by the following formula (Lecture 6):

$$\tau_r \sim \frac{C_{load}(C_{gs}+C_i)}{g_m C_f} \sim 2|A_{FB}|\frac{C_{load}}{g_m} \sim 100\frac{100pF}{10Si} = 1ns \quad (1)$$

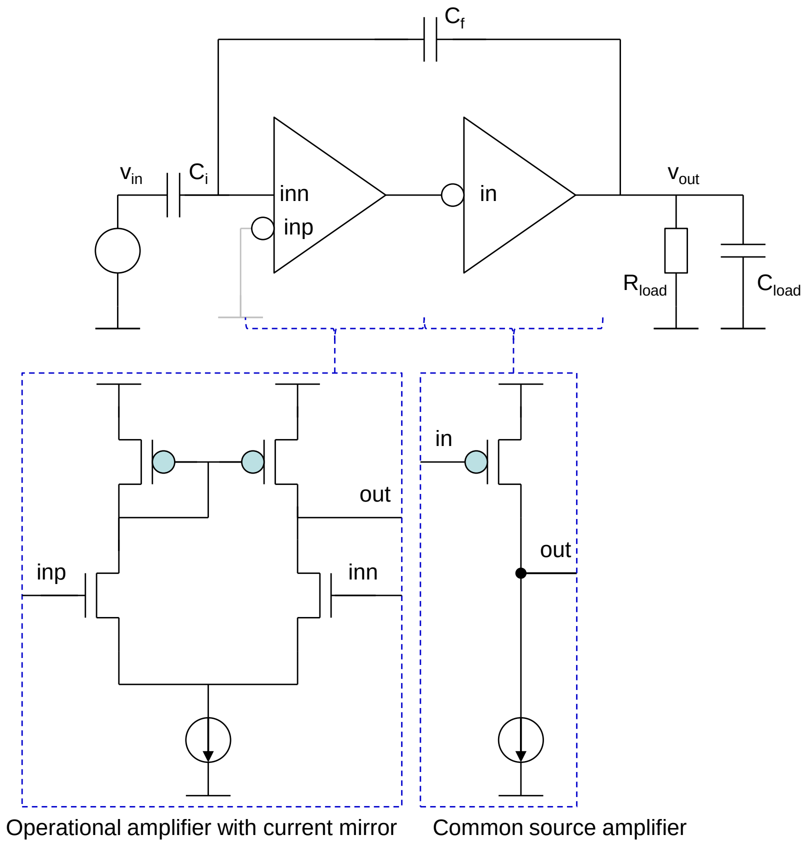
Note that, if the input source has an internal resistance R_i, the time constant at the input is $\tau_i = R_iC_i$. This time constant slows down the amplifier significantly. For $R_i = 100\Omega$, we obtain:

$$\tau_i \sim R_iC_i = 100pF \times 100\Omega = 10ns \quad (2)$$

Disadvantages of the circuit of Figure 5 are a large power consumption, a large layout area and a large capacitive load C_i for the input source.

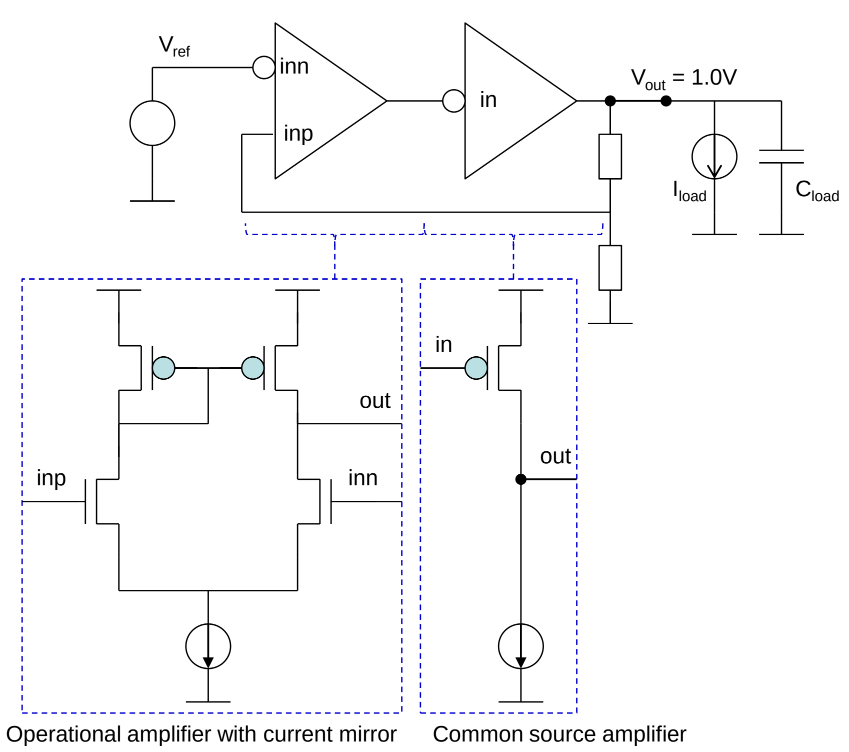
Two-stage amplifiers

Another solution for the implementation of the voltage amplifier and the regulator is to connect two amplifier stages in series.



Voltage amplifier	
Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20

Figure 6: Voltage amplifier implemented with two amplifier stages



LDO regulator	
Parameter	Value
C_{load}	10nF
I_{load}	0-100mA
r_{out}	0.1Ω

Figure 7: Linear regulator implemented with two amplifier stages

Figure 6 shows the voltage amplifier with feedback, which employs two amplifier stages. Figure 7 shows the linear regulator, with the input provided by the reference voltage source V_{ref}. We will discuss the voltage amplifier first.

Voltage amplifier with two stages

Let us derive the transfer function of the two-stage voltage amplifier with feedback. Figure 8 (bottom part) shows the small signal model. We use generic names for the capacitances and resistances at the amplifier outputs C_1, C_2, R_1 and R_2.

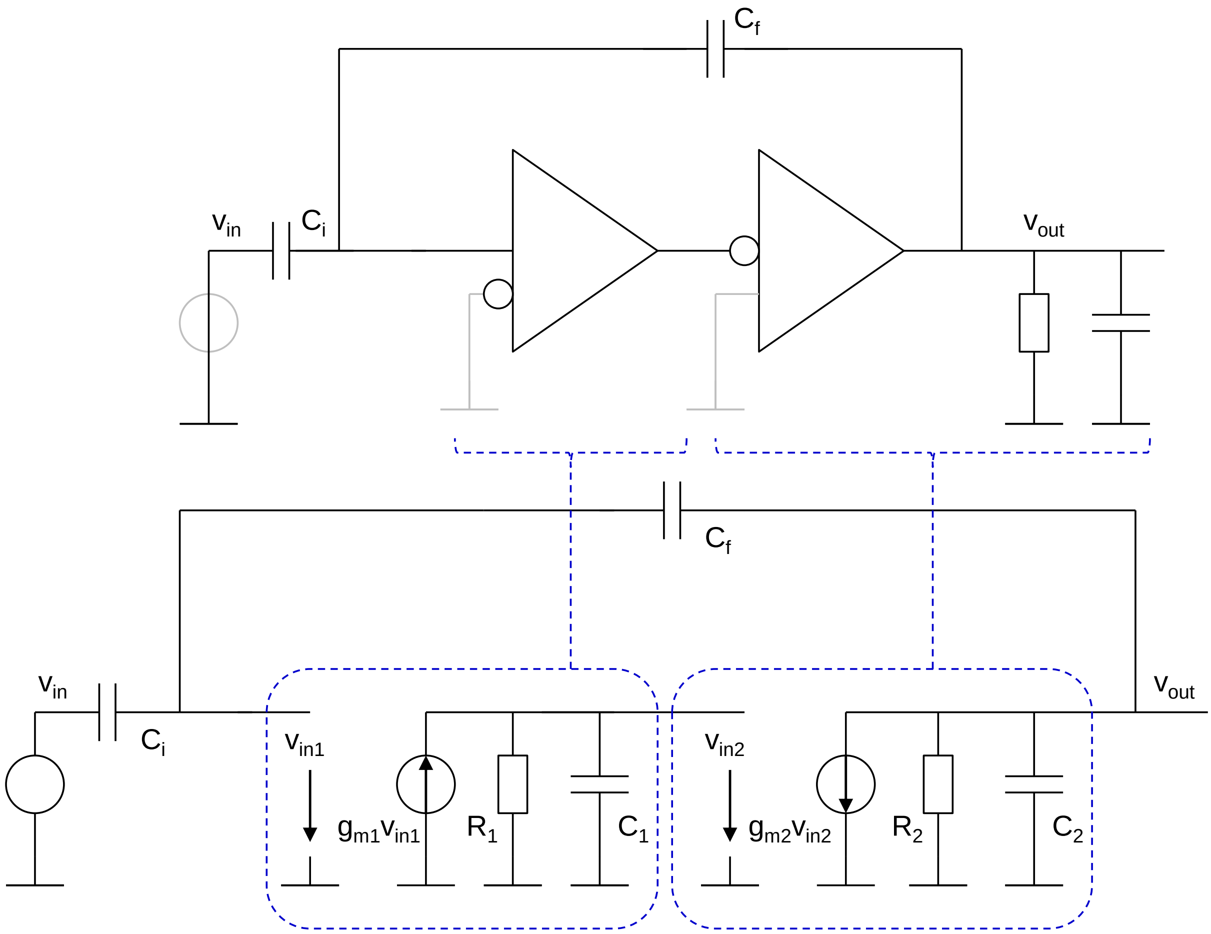


Figure 8: Voltage amplifier based on two amplifying stages and feedback. Top: block circuit. Bottom: small signal model.

The voltage gain with feedback is defined as:

$$A_{FB}(s) = \frac{v_{out}(s)}{v_{in}(s)}$$

It can be calculated using Mason's formula:

$$A_{FB}(s) = \frac{FF + A_{IN}A_{OL}}{1 - \beta A_{OL}} \quad (3)$$

A_{IN} and β are real numbers in our case.

The following applies:

$$\beta = \frac{C_f}{C_f + C_i} \qquad (4)$$

and

$$A_{IN} = \frac{C_i}{C_f + C_i} \qquad (5)$$

Let us make the following assumption: The impedance:

$$Z_2(s) = \frac{1}{sC_2} || R_2 = \frac{R_2}{sR_2C_2 + 1} \qquad (6)$$

is smaller than the other impedances. Therefore it follows:

FF = 0,

and

$$A_{FB}(s) = \frac{A_{IN}A_{OL}}{1 - \beta A_{OL}} \qquad (7)$$

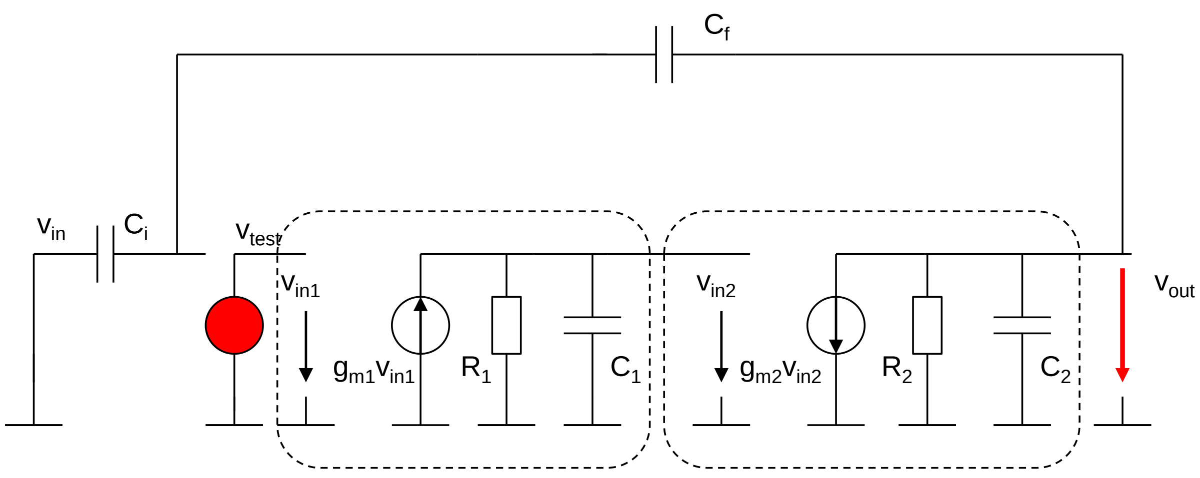


Figure 9: Test circuit for calculation of the open loop gain

Figure 9 shows the test circuit for calculation of the open loop gain.

$$A_{OL}(s) = v_{out(s)}/v_{test}$$

The open loop gain is:

$$A_{OL}(s) = -g_{m1}Z_1g_{m2}Z_2 \qquad (8)$$

Z_1 and Z_2 are the impedances seen by the sources g_{m1} and g_{m2}:

$$Z_1(s) = \frac{1}{sC_1}||R_1 = \frac{R_1}{sR_1C_1+1} \qquad (9)$$

$$Z_2(s) = \frac{1}{sC_2}||\frac{C_f+C_i}{sC_fC_i}||R_2 = \frac{R_2}{sR_2C_2+1} \qquad (10)$$

We have assumed that the serial capacitance of C_f and C_i: $C_f\ C_i/(C_f + C_i) \sim C_f$ is much smaller than C_2.

If we substitute (9) and (10) in (8), we obtain:

$$A_{OL}(s) = \frac{-g_{m1}R_1g_{m2}R_2}{(1+sR_1C_1)(1+sR_2C_2)} \qquad (11)$$

Let us define two time constants and two voltage gains:

$$\tau_1 \equiv R_1C_1,\ \ \tau_2 \equiv R_2C_2,\ \ A_1 \equiv g_{m1}R_1,\ \ A_2 \equiv g_{m2}R_2 \qquad (12)$$

Let us also define the DC open loop gain:

$$A_{OL,DC} \equiv -g_{m1}R_1g_{m2}R_2 \qquad (13)$$

It holds then:

$$A_{OL}(s) = \frac{A_{OL,DC}}{(1+s\tau_1)(1+s\tau_2)} = \frac{A_{OL,DC}}{\tau_1\tau_2s^2+(\tau_1+\tau_2)s+1} \qquad (14)$$

If we insert (4), (5) and (14) in (3) we obtain the transfer function of the circuit with feedback:

$$A_{FB}(s) = \frac{A_{IN}A_{OL,DC}}{1-\beta A_{OL,DC}}\frac{1}{\frac{\tau_1\tau_2}{1-\beta A_{OL,DC}}s^2+\frac{(\tau_1+\tau_2)}{1-\beta A_{OL,DC}}s+1} = A_{FB,DC}\frac{1}{Q(s)} \qquad (15)$$

Q is the characteristic polynomial of the transfer function.

Influence of poles of A_{IN} on step response of A_{FB}

If we replace the complex frequency s with the derivative (d/dt) operator in (15), we obtain the differential equation for the output voltage. The step response has the following form:

$$u_{out,imp}(t) \equiv h(t)(C_0 + C_1 e^{\lambda_1 t} + C_2 e^{\lambda_2 t}) \quad (16)$$

Factors λ_1 and λ_2 are the solutions (roots) of the polynomial Q (s) in (15), or the poles of $A_{FB}(s)$.

$$Q(\lambda) = 0$$

The polynomial Q (s) can be represented in the following canonical form:

$$\frac{\tau_1\tau_2}{1-\beta A_{OL,DC}} s^2 + \frac{(\tau_1+\tau_2)}{1-\beta A_{OL,DC}} s + 1 = \left(\frac{s}{\omega_0}\right)^2 + \left(\frac{1}{Q}\right)\left(\frac{s}{\omega_0}\right) + 1 \quad (17)$$

The factors are:

1) Poles of $A_{IN}(s)$:

$$\omega_1 = \frac{1}{\tau_1};\ \omega_2 = \frac{1}{\tau_2} \quad (18)$$

2) Resonance frequency:

$$\omega_0 = \sqrt{\omega_1\omega_2(1-\beta A_{OL,DC})} \quad (19)$$

3) Quality factor:

$$Q = \frac{\omega_0}{\omega_1+\omega_2} = \frac{\sqrt{\omega_1\omega_2(1-\beta A_{OL,DC})}}{\omega_1+\omega_2} \quad (20)$$

The roots of Q(s) are:

$$\lambda_{12} = -\overline{\omega} \pm \overline{\omega}\sqrt{1-4Q^2};\ \overline{\omega} = \frac{\omega_1+\omega_2}{2} \quad (21)$$

For

$$4Q^2 - 1 > 0 \Rightarrow Q > \frac{1}{2} \quad (22)$$

the step response is **periodic** and contains sine and cosine terms.

$$u_{out,imp}(t) = h(t)\left[A_0 + e^{-\overline{\omega}t}\left(A_1 \cos\left(\sqrt{4Q^2-1}\,\overline{\omega}t\right) + A_2 \sin\left(\sqrt{4Q^2-1}\,\overline{\omega}t\right)\right)\right] \quad (23)$$

with $A_0 = 1$, $A_1 = -1$ und $A_2 = 1/(4Q^2 - 1)^{0.5}$.

For

$4Q^2 - 1 < 0 \Rightarrow Q < \frac{1}{2}$ (24)

the step response is **aperiodic** and exponential with **real time constants**:

$\tau_{1,fb} = -1/\lambda_1$ and $\tau_{2,fb} = -1/\lambda_2$:

$u_{out,imp}(t) = h(t)[C_0 + C_1 e^{-\tau_{1,fb} t} + C_2 e^{-\tau_{2,fb} t}]$ (25)

with $C_0 = 1$, $C_1 = -\lambda_2/(\lambda_2 - \lambda_1)$ und $C_2 = \lambda_1/(\lambda_2 - \lambda_1)$.

The condition (24) leads to the following equation:

$Q = \frac{\sqrt{\omega_1\omega_2(1-\beta A_{OL,DC})}}{\omega_1+\omega_2} < \frac{1}{2}$ (26)

If we assume that the time constants in $A_{OL}(s)$ τ_1 and τ_2 are very different:

$$\tau_1 \gg \tau_2;\ \omega_1 \ll \omega_2$$

and if we assume that $\beta_{AOL,\,DC}$ is negative and has a large amount, the formula (26) simplifies as follows:

$Q \sim \frac{\sqrt{\omega_1\omega_2|\beta A_{OL,DC}|}}{\omega_2} < \frac{1}{2} \Rightarrow \frac{\omega_1|\beta A_{OL,DC}|}{\omega_2} < \frac{1}{4}$

or:

$\tau_2 < \frac{1}{4}\frac{\tau_1}{|\beta A_{OL,DC}|}$ (27)

The second time constant τ_2 must be smaller than the first time constant τ_1 divided by 4 | βA_{DC} |. Since | βA_{DC} | is normally >> 1 (in our example | βA_{DC} | = 20), the second time constant must be much smaller than the first so that the step response does not oscillate. Very different time constants in the open gain lead to exponential behaviour.

If the following holds:

$\tau_2 \ll \frac{1}{4}\frac{\tau_1}{|\beta A_{OL,DC}|}$

It holds also Q << 1.

(Note that Q is always greater than 0.)

The step response is then approximately:

$$u_{out,imp}(t) \sim h(t)\left[1 - e^{-\frac{t}{\tau_r}}\right] \qquad (28)$$

With the rise time:

$$\tau_r = \frac{\tau_1}{\beta A_{OL,DC}} \qquad (29)$$

We define here the bandwidth of amplifier B as

$$B = \frac{1}{2\pi\tau_r} \qquad (30)$$

The larger time constant τ_1 is also called the **dominant time constant**, since it determines the step response.

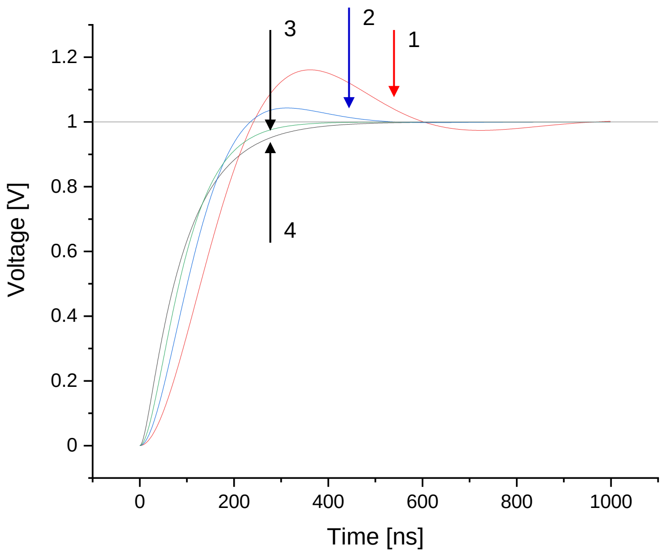


Figure 10: Step responses for different βA_{OL} functions with Q values: 1) Q ~ 1; 2) Q ~ 0.707; 3) Q ~ 0.5 and 4) Q ~ 0.32. βA_{DC} = 100.

Figure 10 shows the step responses which correspond to the βA_{OL} having the parameters from the following table.

Case	**ω_1**	**ω_2**	**Q**	**Ratio τ_1/τ_2 (βA_{DC} = 100)**	**PM**
1	0.1MHz	100×ω_1	1	$\tau_2 > \frac{1}{2}\frac{\tau_1}{\lvert\beta A_{OL,DC}\rvert}$	53°
2	0.1MHz	200×ω_1	0.707	$\tau_2 = \frac{1}{2}\frac{\tau_1}{\lvert\beta A_{OL,DC}\rvert}$	67°
3	0.1MHz	400×ω_1	0.5	$\tau_2 = \frac{1}{4}\frac{\tau_1}{\lvert\beta A_{OL,DC}\rvert}$	77°
4	0.1MHz	1000×ω_1	0.32	$\tau_2 < \frac{1}{4}\frac{\tau_1}{\lvert\beta A_{OL,DC}\rvert}$	85°

The step response (3) for Q = 0.5 that is equivalent to

$$\tau_2 = \frac{1}{4}\frac{\tau_1}{|\beta A_{OL,DC}|}$$

differs only a little from the aperiodic step response for Q < 0.5:

$$u_{out,imp}(t) \sim h(t)\left[1 - e^{-\frac{t}{\tau_r}}\right];\ \tau_r = \frac{\tau_1}{\beta A_{OL,DC}}$$

Note that the step response (2) in Figure 10 for

$$Q = \frac{1}{\sqrt{2}} = 0.707\ \Rightarrow \tau_2 = \frac{1}{2}\frac{\tau_1}{|\beta A_{OL,DC}|}$$

first reaches the amplitude of 1. It has no undershoot.

Interestingly, the two-stage amplifier has real time constants and exhibits exponential time behavior when no feedback is applied. By using feedback, the time response can become oscillatory, as if inductors and capacitors were present in the circuit. This is the reason why it is possible to realize oscillators using feedback, without the need for actual inductors.

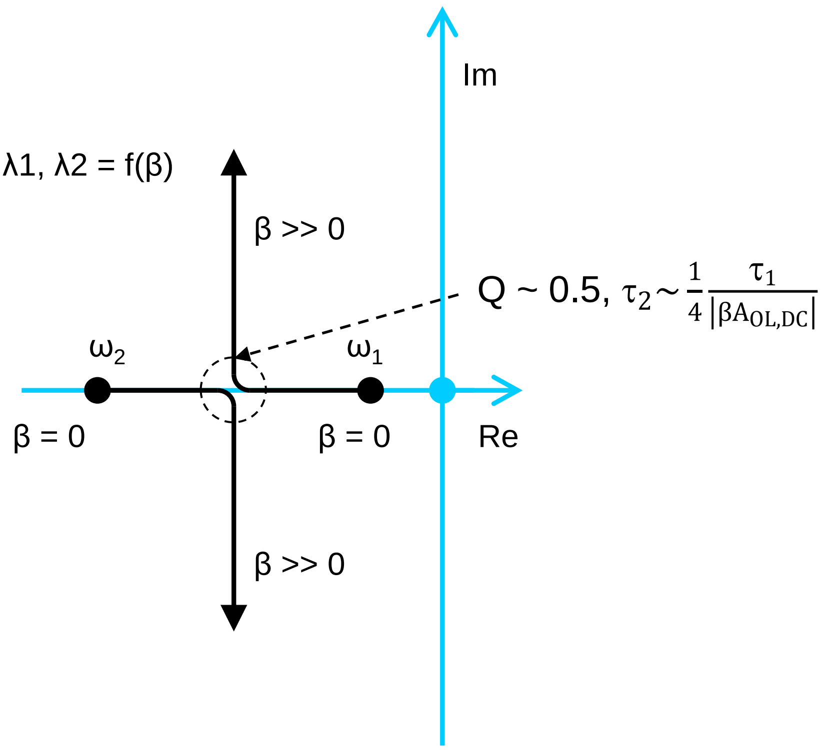


Figure 11: Position of poles of $A_{FB}(s)$ when the strength of the feedback β increases

Figure 11 shows how the roots λ_1 and λ_2 of the characteristic polynomial Q (s) of

$$A_{FB}(s) = \frac{A_{IN}A_{OL}(s)}{1-\beta A_{OL}(s)} \equiv \frac{P(s)}{Q(s)}$$

(poles of A_{FB} (s)) move in a complex plane if we increase the strength of the negative feedback β starting from 0. Without negative feedback (β = 0) the poles of A_{FB} (s) are equal to the poles of A_{OL} (s): $\lambda_1 = \omega_1$ and $\lambda_2 = \omega_2$. The poles are real numbers. When the negative feedback increases, the poles move towards each other (Q increases) until they become equal for Q = 0.5 $\lambda_1 = \lambda_2 = (\omega_1 + \omega_2) / 2$. For Q > 0.5, the poles become complex with a constant real part

= ($\omega_1 + \omega_2$) / 2. The imaginary parts have the same magnitude and opposite signs. The step response contains then sine and cosine terms.

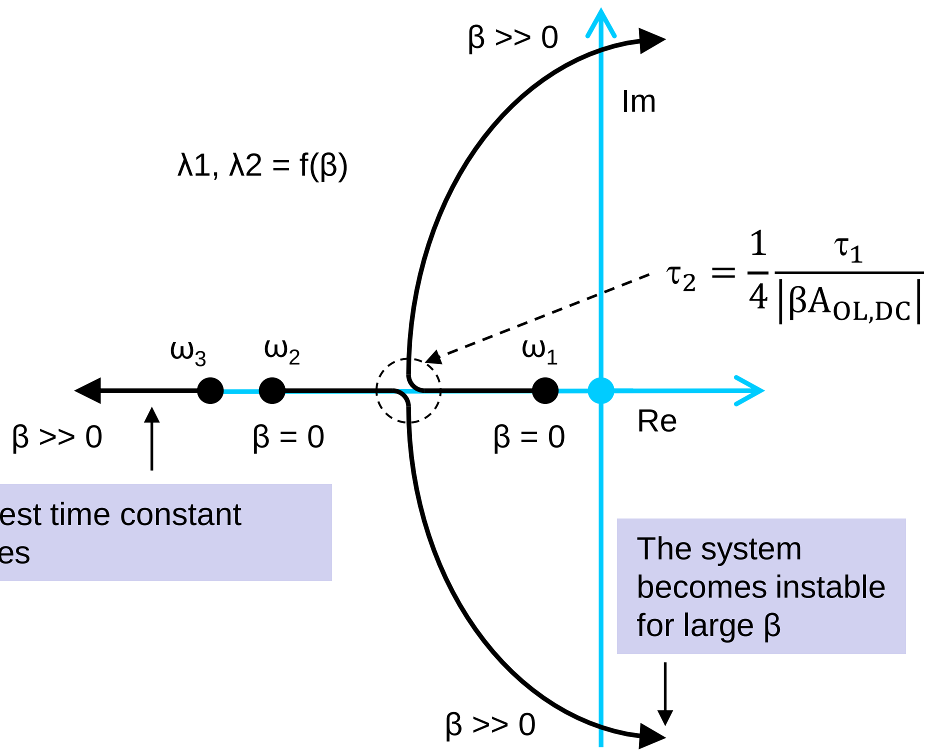


Figure 12: Position of three poles of $A_{FB}(s)$ when the strength of the feedback β increases

Figure 12 shows the case where $A_{IN}(s)$ has three poles ω_1, ω_2 and ω_3. We can perform a similar analysis as above and plot in a complex plane how the poles of $A_{FB}(s)$ move when we increase the strength of the negative feedback β. The poles of $A_{FB}(s)$ are real for $\beta = 0$: $\lambda_1 = \omega_1$, $\lambda_2 = \omega_2$ and $\lambda_3 = \omega_3$. The two smaller poles move towards each other and become complex. The third pole remains real and its magnitude increases, the corresponding time constant gets smaller. The only difference to the second order system is that the real part of the complex poles can also become positive for high β. The amplitude of the oscillation then increases until the circuit is no longer linear. The circuit becomes unstable.

> The conditions for a step response without oscillations are nearly equal for 2nd - and 3rd order systems. This means that all formulas from this lecture can also be used in the case of $A_{IN}(s)$ with three poles.

Nyquist stability criterion

There is a method that allows us to determine, in the general case, whether the poles of:

$$A_{FB}(s) = \frac{A_{IN}(s)A_{OL}(s)}{1-\beta A(s)} \qquad (31)$$

have negative real parts, and therefore whether the corresponding circuit with feedback is stable. The assumption is that all factors have a frequency dependence:

$$\beta A(s) = \frac{L(s)}{M(s)};\ A_{IN}(s)A_{OL}(s) = \frac{N(s)}{O(s)} \qquad (32)$$

This method is known as Nyquist's stability criterion. It is closely related to the Bode diagram.

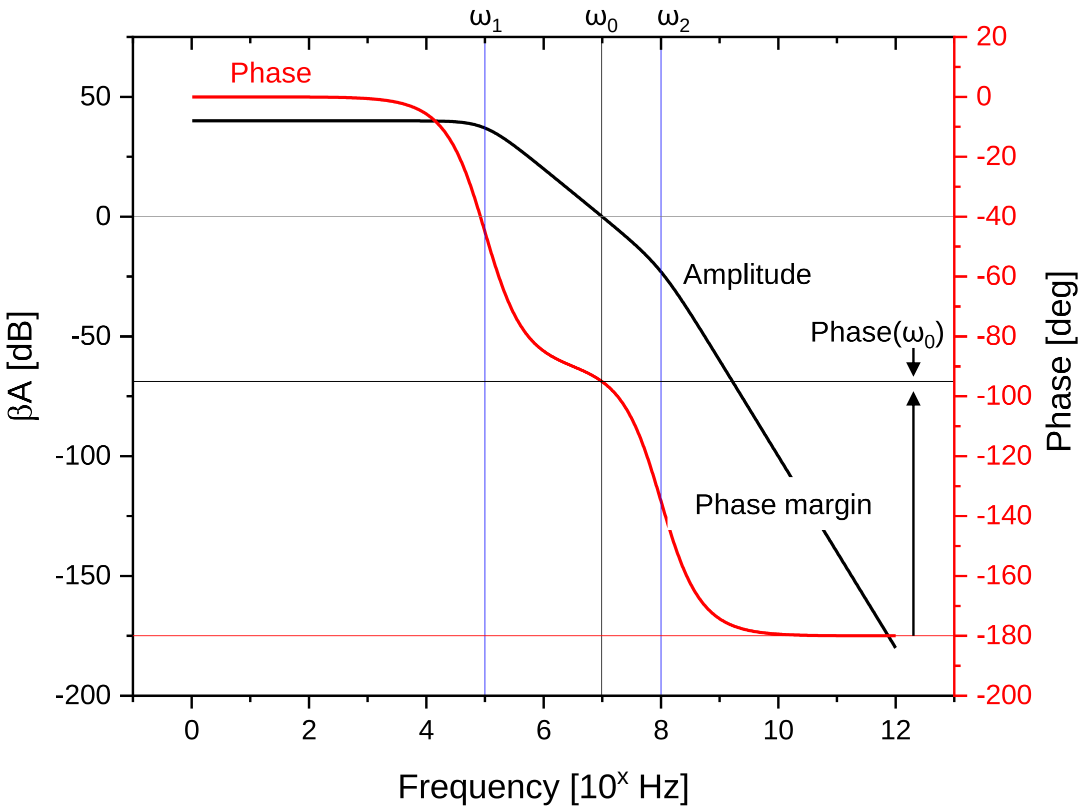


Figure 13: Bode diagram

The Bode diagram of a transfer function βA(jω) with two time constants

$$\beta A(j\omega) = \frac{A}{(j\omega/\omega_1+1)(j\omega/\omega_2+1)} \qquad (33)$$

is shown in Figure 13. The left Y-axis shows $|\beta A(j\omega)|$ in dB or $20 \log(|\beta A(j\omega)|)$.

$$|\beta A(j\omega)| = \frac{A}{\sqrt{\left(\left(\frac{\omega}{\omega_1}\right)^2+1\right)\left(\left(\frac{\omega}{\omega_2}\right)^2+1\right)}} \qquad (34)$$

X–axis is log(ω).

The frequencies ω_1 = 0.1 MHz and ω_2 = 100 MHz are the poles of βA (jω). The slope of the magnitude plot after the first pole is -20dB / decade and after the second pole it is -40dB / decade.

The right Y axis shows the phase of βA (jω):

$$\text{Phase}(\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_1}\right) - \tan^{-1}\left(\frac{\omega}{\omega_2}\right) \qquad (35)$$

The phase changes by approximately -90° around each pole ω, in the region from 0.1 ω to 10 ω.

We define the zero crossing frequency ω_0 as the frequency that satisfies the condition

$|\beta A(j\omega_0)| = 1$ ($|\beta A(j\omega_0)| = 0$ dB)

A circuit with feedback is stable [1] if the absolute value of the phase change of the loop gain βA(iω) from ω = 0 to $\omega = \omega_0$ is less than 180 °.

The difference between 180° and the absolute value of the phase change is called the phase margin (PM) (Figure 13).

The condition for the validity of the Nyquist criterion is that the functions βA(s) and $A_{IN}(s)$ $A_{OL}(s)$ have no poles with a positive real part.

[1] The poles of A_{FB} (iω) have negative real parts

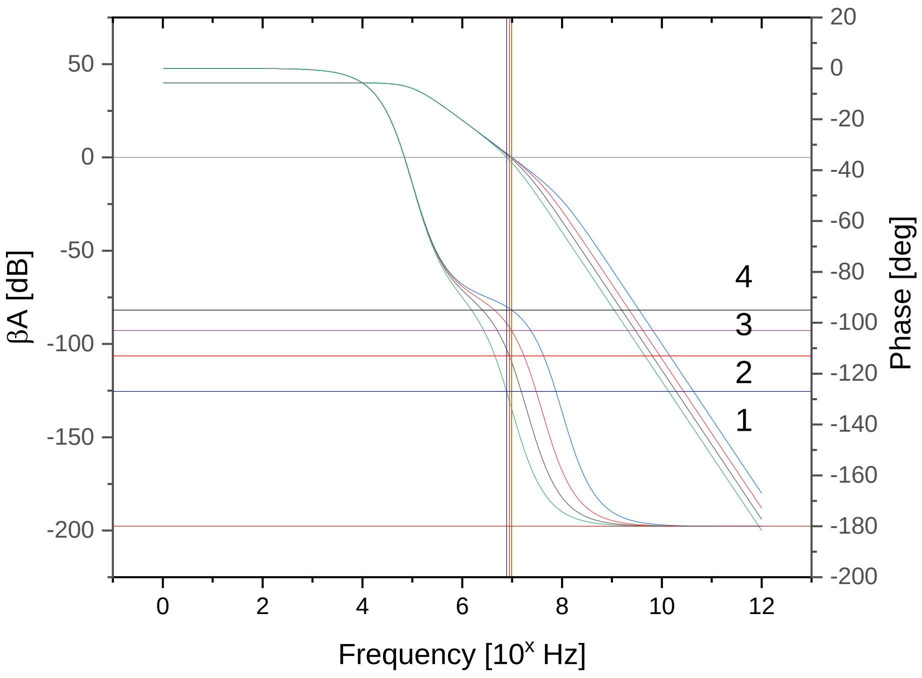


Figure 14: Bode diagrams of βA(s) functions with the parameters from the table

Figure 14 shows Bode diagrams for the βA_{OL} functions with parameters from the table. (It holds $\beta A_{OL,DC} = 100$.) The parameters are the same as in Figure 10. βA_{OL} with phase margin < 67 ° leads to a periodic step response.

Case	ω_1	ω_2	Q	PM
1	0.1MHz	$100\times\omega_1$	1	53°
2	0.1MHz	$200\times\omega_1$	0.707	67°
3	0.1MHz	$400\times\omega_1$	0.5	77°
4	0.1MHz	$1000\times\omega_1$	0.32	85°

The condition for aperiodic step response

$$\tau_2 = \frac{1}{4}\frac{\tau_1}{|\beta A_{DC}|}; Q = 0.5$$

corresponds to a phase margin of = 77 °.

The conditions for the fastest step response

$\tau_2 = \frac{1}{2}\frac{\tau_1}{|\beta A_{DC}|}; Q = 0.707$

corresponds to a phase margin of 67 °.

The greater the separation between the first and second time constants, the larger the phase margin.

First implementation of the two-stage voltage amplifier

We will start with the specifications in the table:

Voltage amplifier	
Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20

We can optimize the amplifier in two ways:

1. The current consumption (and thus power consumption) should be minimal.
2. The bandwidth, as defined by Equation (30), should be as large as possible, so that the rise time of the step response is minimized.

In this lecture, we will focus on optimizing the amplifier for low power consumption.

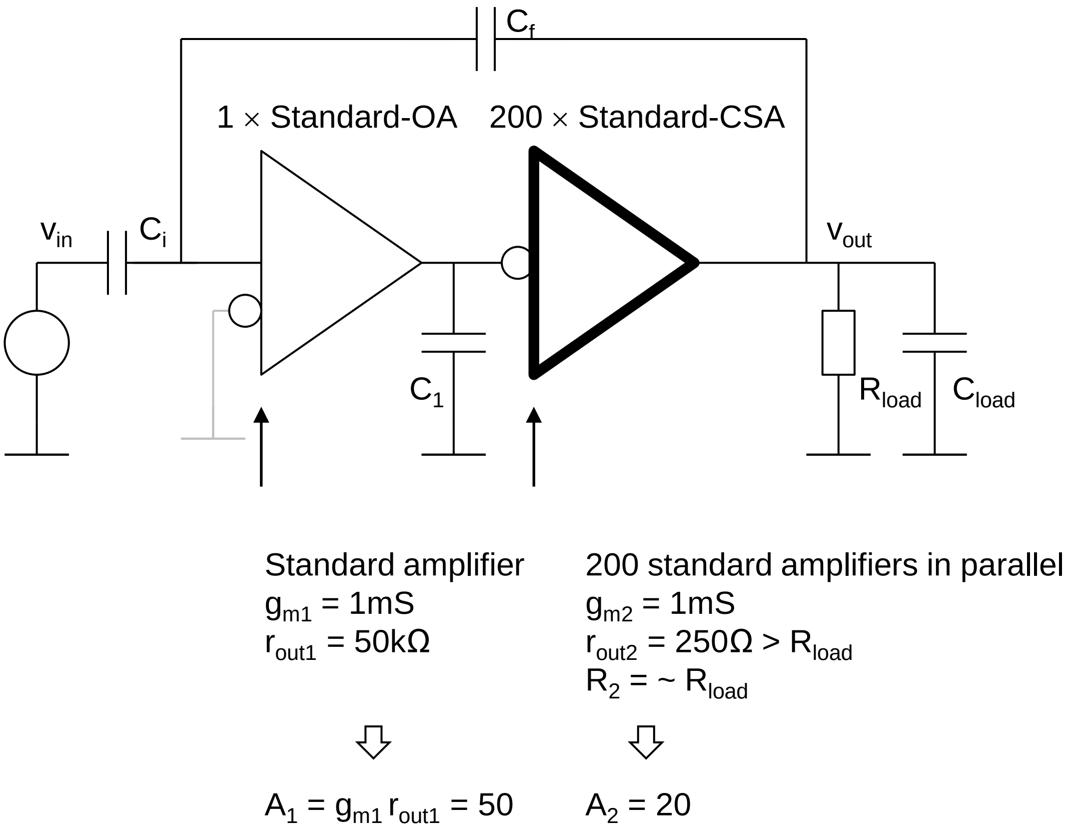


Figure 15: Two-stage voltage amplifier, implementation with the standard amplifiers (amplifier with I_{bias} = 50 µA). The first amplifier stage is implemented with a standard size operational amplifier (OA). The second amplifier stage consists of 200 common source amplifiers (CSA) (each standard size) in parallel.

We use a simple operational amplifier with a current mirror as the first stage, and a common-source amplifier with an active load (without cascode) as the second stage (Figure 15). Our standard amplifiers (standard-size amplifiers) have I_{bias} = 50µA, g_m = 1mS, r_{out} = 50kΩ. The voltage gain of the amplifier without a resistive load is $A = g_m r_{out} = 50$. If we use the standard amplifier as the second stage and connect it to R_{load} = 100 Ω, the voltage gain is reduced to only:

$$A_2 = g_m(r_{out}||R_{load}) \sim g_m R_{load} = 0.1$$

A_2 is defined here as an absolute value, the actual gain of dv_{out} / dv_{in} is negative (= $-A_2$).

In this case, the two-stage amplifier would have a total gain of only

$A = A_1 A_2 = 50 \times 0.1 = 5$.

To achieve the specified total gain of 1000, we need at least $A_2 = 20$.

For the second stage, we will therefore connect multiple common-source amplifiers in parallel until the gain reaches 20:

$$A_2 = g_{m,par}(r_{out,par}||R_{load}) \sim 20$$

We need to use around 200 standard amplifiers (Figure 15).

In this case it holds:

$g_{m2} = g_{m,par} = 200 \times 1mS = 200mS$ (36)

$r_{out2} = r_{out,par} = 50k\Omega/200 = 250\Omega$ (37)

and

$A_2 = g_2(r_{out,2}||R_{load}) \sim g_{m2}R_{load} = 20$ (38)

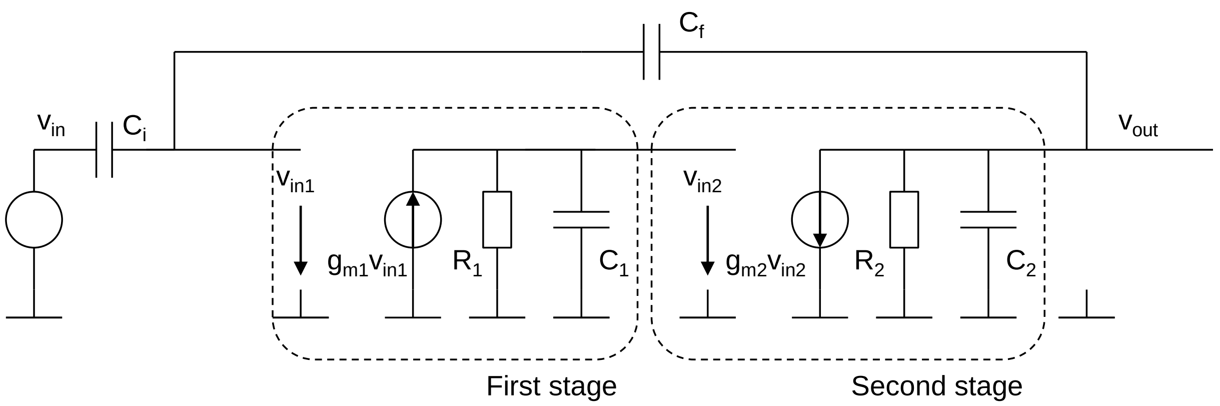


Figure 16: Two-stage voltage amplifier - small signal model

The implemented circuit shown in Figure 15 corresponds to the generic circuit in Figure 16, provided that the values in the following table are applied:

Generic circuit	**Implemented circuit**	**Value**
R_1	r_{out1}	$50k\Omega$
R_2	R_{load}	100Ω
C_2	C_{load}	100pF
C_1	C_1	TBD
g_{m1}	g_{m1}	1mS
g_{m2}	g_{m2}	200mS

A_1	$g_{m1}r_{out1}$	50
A_2	$g_{m1}R_{load}$	20

Let us now calculate the factors β, A_{IN}, and A_{OL}.

We will implement the feedback using two capacitors C_i and C_f. We choose C_i = 50 C_f. The value for C_f can be selected relatively freely, we set C_f = 200 fF. (Larger C_f values result in lower noise.)

In this case, we get:

$$\beta = \frac{C_f}{C_f + C_i} = 0.02 \qquad (39)$$

and

$$A_{IN} = \frac{C_i}{C_f + C_i} \sim 1 \qquad (40)$$

The open loop gain is (s. (14)):

$$A_{OL}(s) = \frac{-g_{m1}r_{out1}g_{m2}R_{load}}{(1+sr_{out1}C_1)(1+sR_{load}C_{load})} = \frac{-A_1A_2}{(1+s\tau_1)(1+s\tau_2)} \qquad (41)$$

This formula is equal to (14).

A_{FB} and the step response are described with formulas (15), (23) and (25).

Stability

Let us now calculate the value of capacitance C_1 required to achieve a step response without oscillations.

The condition for τ_2 to obtain a step response without overshoot is given by Equation (27):

$$\tau_2 < \frac{1}{4}\frac{\tau_1}{|\beta A_{OL,DC}|}$$

The dominant time constant τ_1 is then:

$$\tau_1 > 4|\beta A_{OL,DC}|R_{load}C_{load} = 4 \times 20 \times 10 \text{ ns} = 800 \text{ ns} \qquad (42)$$

This condition can be achieved by suitable C_1:

$$\tau_1 = r_{out1}C_1 > 4|\beta A_{OL,DC}|R_{load}C_{load} \Rightarrow C_1 > \frac{4 \times 20 \times 10\text{ ns}}{50k\Omega} = 16pF \tag{43}$$

The rise time of the step response is then approximately:

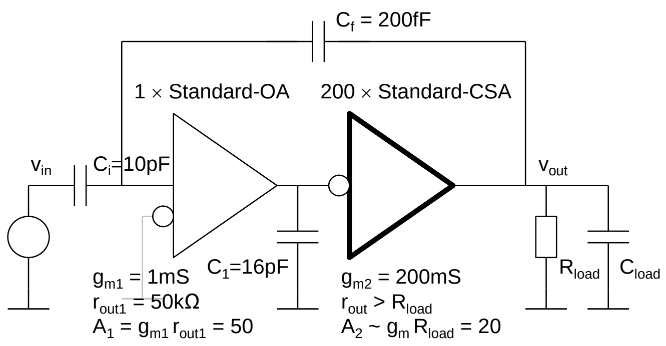
$$\tau_r \sim \frac{\tau_1}{\beta A_{OL,DC}} = \frac{C_1}{\beta g_{m1} A_2} > \frac{4|\beta A_{OL,DC}|R_{load}C_{load}}{\beta A_{OL,DC}} = 4R_{load}C_{load} = 40ns \tag{44}$$

Unfortunately τ_r is relatively long, which makes the step response slow and reduces the bandwidth.

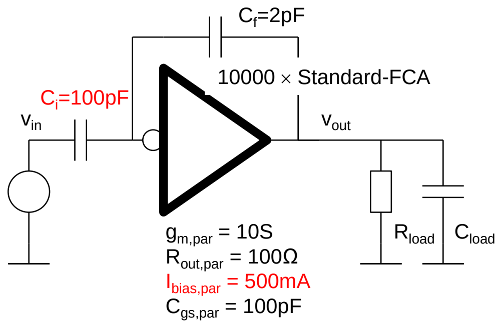
The following table summarizes the results:

Generic circuit	**Implemented circuit**	**Value**
R_1	r_{out1}	50kΩ
R_2	R_{load}	100Ω
C_2	C_{load}	100pF
C_1	C_1	16pF
g_{m1}	g_{m1}	1mS
g_{m2}	g_{m2}	200mS
A_1	$g_{m1}r_{out1}$	50
A_2	$g_{m1}R_{load}$	20
τ_1	$r_{out1}\, C_1$	$4\beta A\tau_2$
τ_2	$R_{load}\, C_{load}$	10ns
βA	$\beta A_1 A_2$	20

Conclusion: The two-stage amplifier meets the specification for open-loop gain and consumes approximately 50 times less power than the single-stage amplifier. However, the minimum rise time of the step response is about 40 times longer than that of the single-stage amplifier. Figure 17 shows a comparison between the two designs.



Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20
τ_r	$4C_{load}R_{load}$ = 40ns
I_{bias}	(201 I_0) 10.1mA



Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	<50
A_{OL}	500
βA	10
τ_r	$2A_{FB}C_{load}/g_m$=1ns
I_{bias}	(10000 I_0) 500mA

Figure 17: Comparison between voltage amplifiers with two stages (top) and with one stage (bottom). Disadvantages are marked in red - e.g. in the case of single-stage amplifier, high power consumption or high input capacitance. OA - operational amplifier, CSA - common source amplifier, FCA - folded cascode amplifier.

Implementation 2 (frequency compensation)

We have seen that a two-stage amplifier can achieve high gain with low power consumption. However, the simple variant shown in Figure 15 has a relatively small bandwidth (Equation 30) when feedback is applied. The bandwidth can be improved by connecting a capacitor C_1 between the input and the output of the second stage (Figure 18). This technique is called frequency compensation. The DC gain of the second stage must be negative. The capacitor between the input and output of the second stage separates the time constants (pole splitting), which reduces oscillations and improves the bandwidth. We will discuss this technique in detail in this chapter.

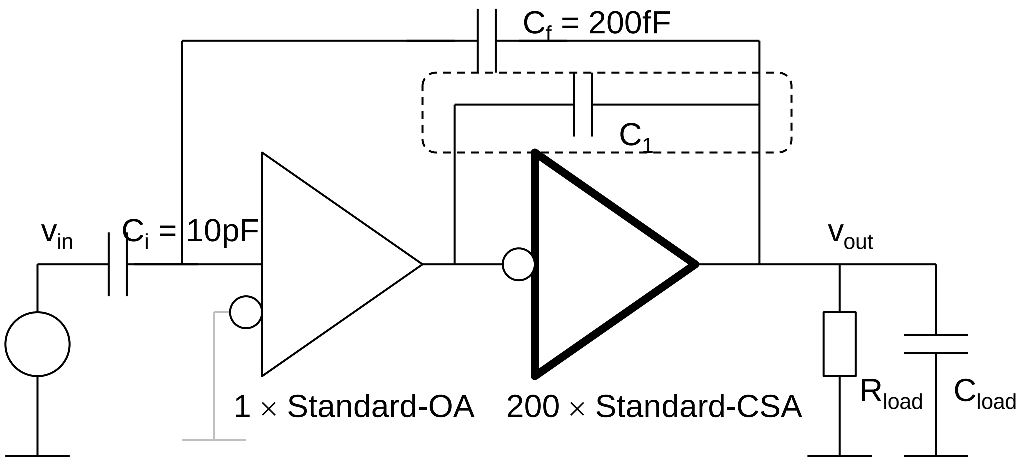


Figure 18: Two-stage amplifier with frequency compensation

We start with the dimensions of the amplifier stages as in the first example:

Generic circuit	Implemented circuit	Value
R_1	r_{out1}	50kΩ
R_2	R_{load}	100Ω
C_2	C_{load}	100pF
C_1	C_1	TBD
g_{m1}	g_{m1}	1mS
g_{m2}	g_{m2}	200mS
A_1	$g_{m1}r_{out1}$	50

A_2	$g_{m1}R_{load}$	20

Let us calculate the factors β, A_{IN}, and A_{OL}.

We set C_i = 10 pF and C_f = 200 fF again. It follows:

$$\beta = \frac{C_f}{C_f + C_i} = 0.02 \qquad (45)$$

and

$$A_{IN} = \frac{C_i}{C_f + C_i} \sim 1 \qquad (46)$$

Let us now calculate A_{OL}. The test circuit is shown in Figure 19.

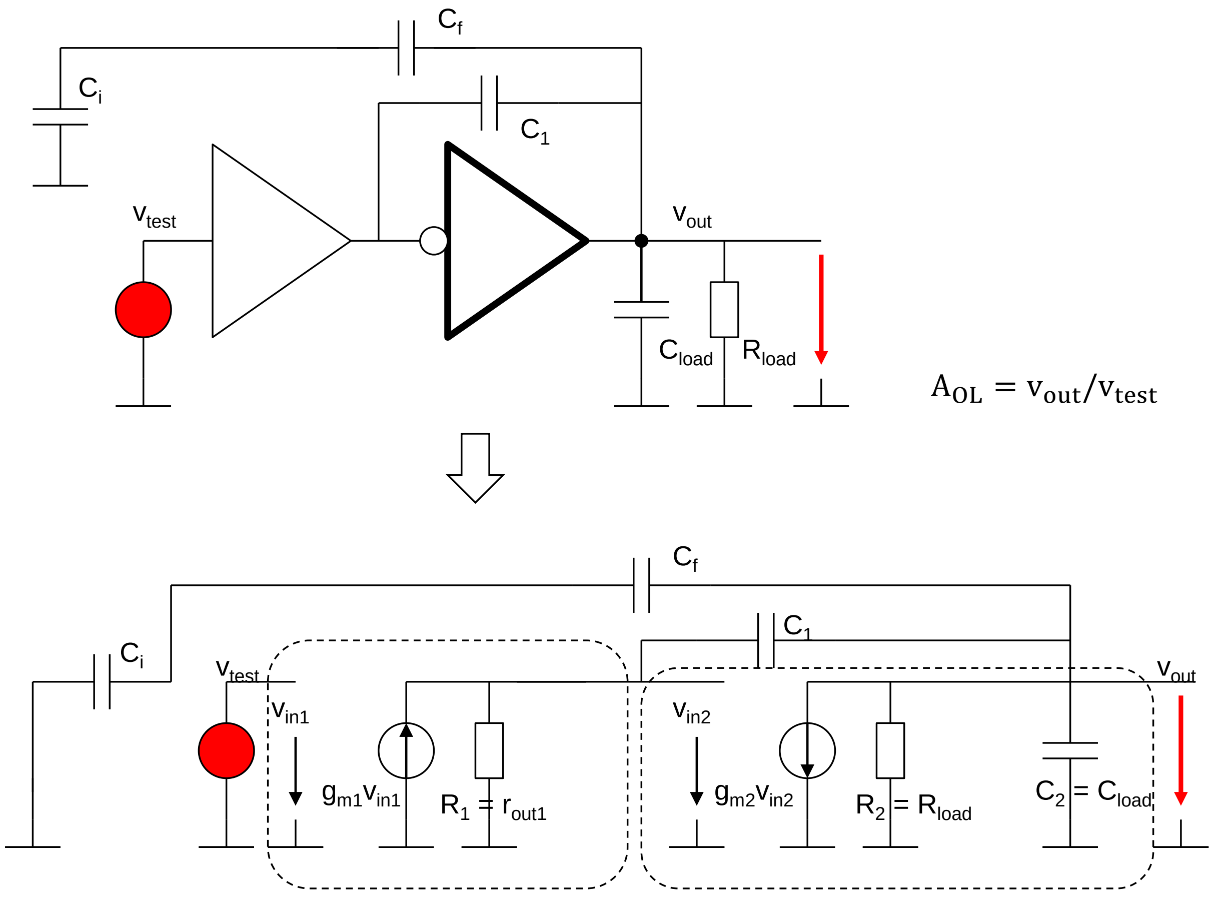


Figure 19: Test circuit for calculating of the open loop gain A_{OL}

If we assume that the serial capacitance $C_f\, C_i / (C_f + C_i) \sim C_f$ is much smaller than C_{load} and if we replace the current source $g_{m1}\, v_{in1}$ with an equivalent voltage source, we obtain a simplified circuit in Figure 20.

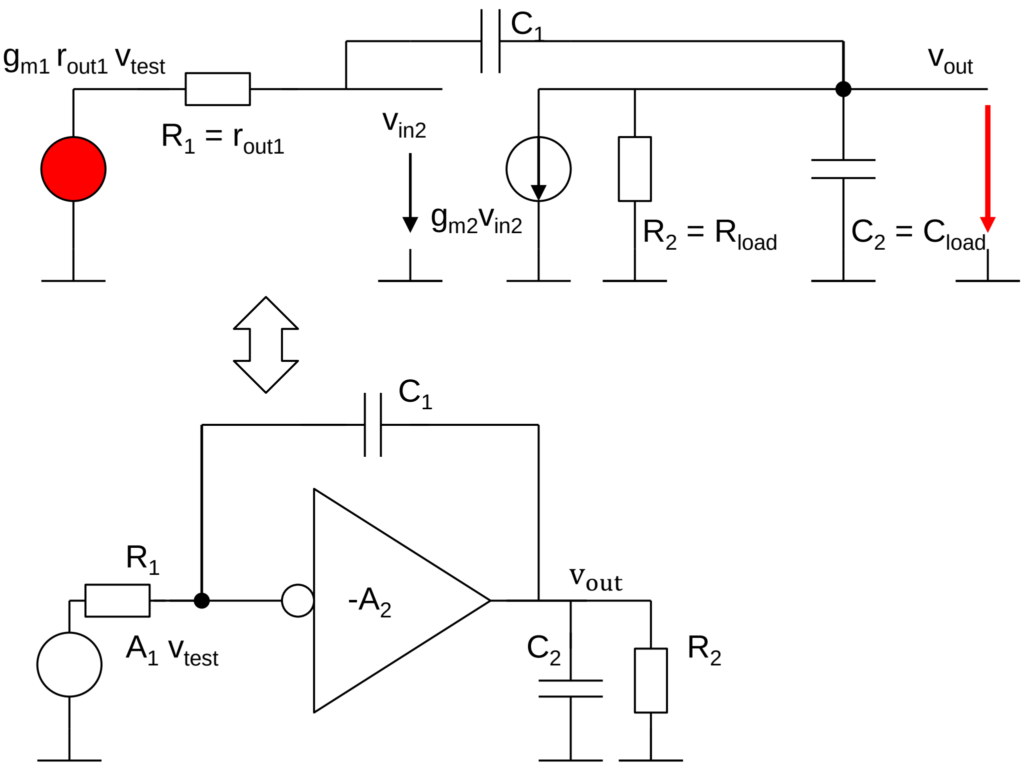


Figure 20: Simplified test circuit for calculating of the open loop gain A_{OL}

The amplification A_{OL} has its own feedback that is created by C_1 and R_1.

We can employ the Mason's formula for A_{OL}:

$$A_{OL}(s) = \frac{A_{IN,AOL}A_{OL,AOL}}{1+\beta_{AOL}A_{OL,OL}} \qquad (47)$$

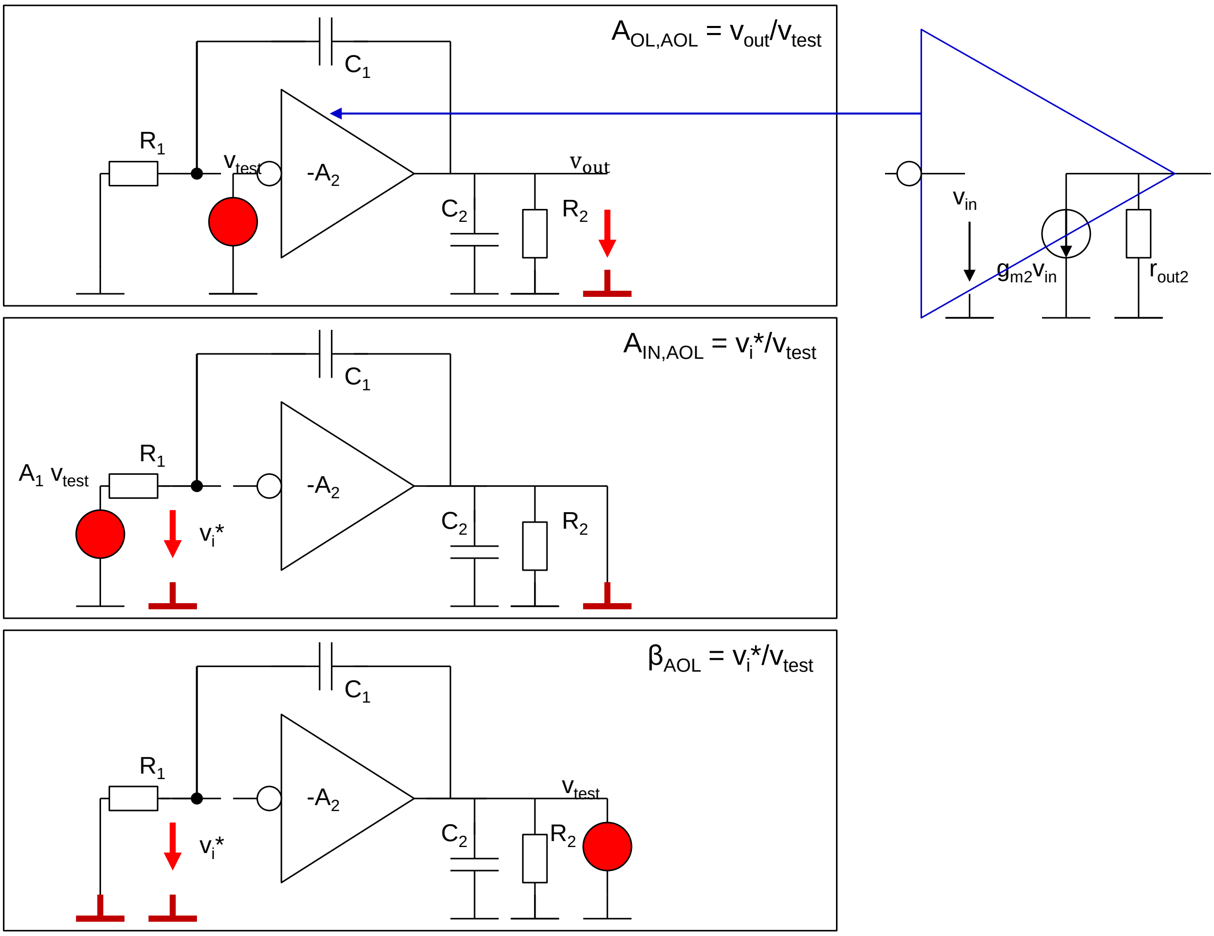


Figure 21: Test circuits for calculating $A_{OL,\,AOL}$ (top), $A_{IN,\,AOL}$ (middle) and β_{AOL} (bottom).

The test circuits for the calculation of factors $A_{OL,\,AOL}$ (top), $A_{IN,\,AOL}$ (middle) and β_{AOL} (bottom) are shown in Figure 21.

The open loop gain $A_{OL,\,AIN}$ is:

$$A_{OL,AOL}(s) = -\frac{g_{m2}R_{load}}{sR_{load}C_{load}+1} \equiv -\frac{A_2}{sT_2+1} \qquad (48)$$

The input gain $A_{IN,AOL}$ is:

$$A_{IN,AOL}(s) = \frac{g_{m1}r_{out1}}{sr_{out1}C_1+1} \equiv \frac{A_1}{sT_1+1} \qquad (49)$$

The time constants T_1 and T_2 are defined as follows:

$T_1 = r_{out1}C_1;\ T_2 = R_{load}C_{load}$

The feedback is:

$$\beta_{AOL}(s) = -\frac{sr_{out1}C_1}{sr_{out1}C_1+1} = \frac{sT_1}{sT_1+1} \qquad (50)$$

If we insert the factors (48) - (50) in the Mason's formula, we get:

$$A_{OL} = -\frac{\frac{A_1}{1+sT_1}\frac{A_2}{1+sT_2}}{1+\frac{A_2}{1+sT_2}\frac{sT_1}{1+sT_1}} \qquad (51)$$

We can rewrite the formula (51) as follows:

$$A_{OL} = -\frac{A_1A_2}{1+sT_2+sT_1+sA_2T_1+s^2T_1T_2}$$

Let us sort the factors in the denominator according to their size and try to simplify the expression. The term sA_2T_1 is much larger than sT_1. Therefore sT_1 can be neglected. We assume that sA_2T_1 is much larger than sT_2. The factor $s^2\,T_1\,T_2$ cannot be omitted because it dominates for high frequencies.

A_{OL} is simplified as follows:

$$A_{OL} = -\frac{A_1A_2}{1+sA_2T_1+s^2T_1T_2}$$

We can add a small term sT_2 / A_2 to the polynomial in denominator - that changes little and allows us to factorize the polynomial. We get:

$$A_{OL} = -\frac{A_1 A_2}{\left(1+s\frac{T_2}{A_2}\right)(1+sA_2 T_1)} = -\frac{A_1 A_2}{(1+s\tau_{2,B})(1+s\tau_{1,B})} \qquad (52)$$

Let us compare A_{OL} in the case when C_1 is connected to ground (case A, without frequency compensation - Figure 22 top) and when C_2 is connected between the input and the output of the second stage (case B, frequency compensation - Figure 22 bottom).

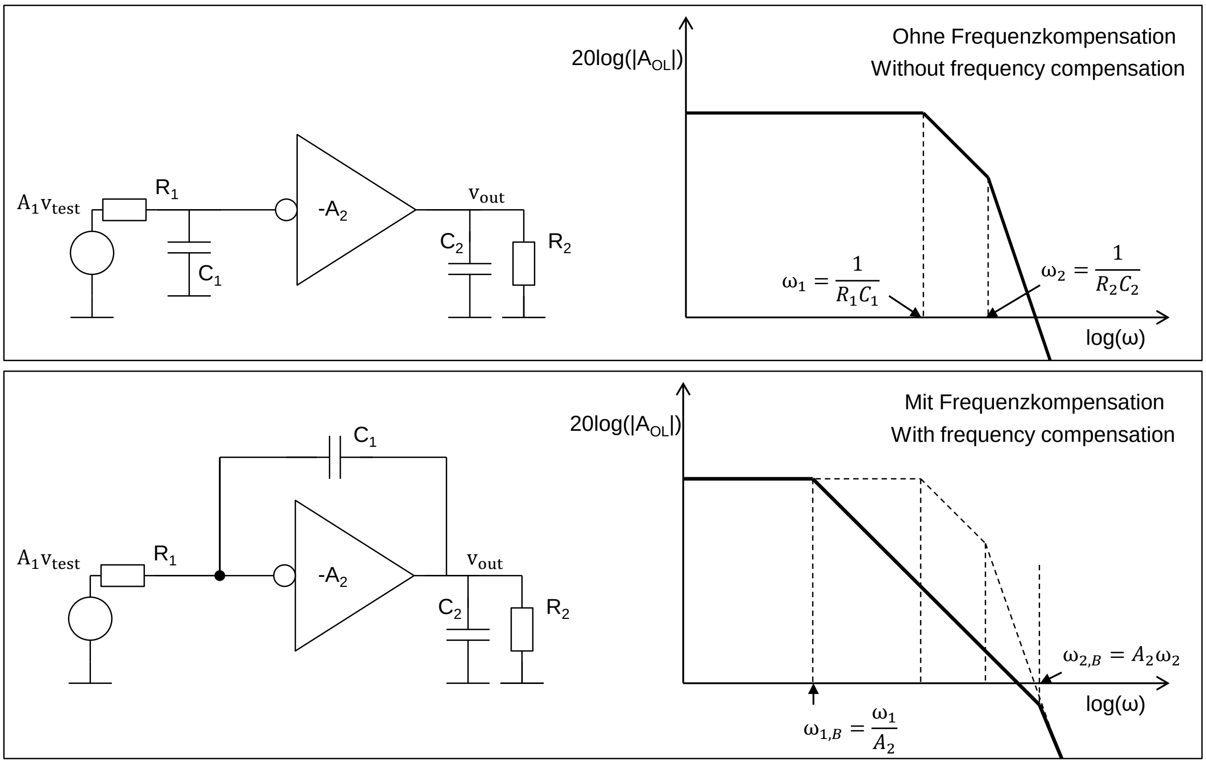


Figure 22: Gain $A_{OL} = v_{out} / v_{test}$ without / with frequency compensation

The frequency compensation separates the poles (pole splitting).

The time constants of A_{OL} (s) without frequency compensation are (41):

$\tau_1 = T_1$; $\tau_2 = T_2$

The time constants of A_{OL} (s) with frequency compensation are (52):

$\tau_{1,B} = A_2 T_1$; $\tau_{2,B} = T_2 / A_2$.

One explanation for longer time constants $\tau_{1,B}$ is the Miller effect. We will explain this effect in the next paragraph.

In the previous analysis we have neglected the input capacitance of the second stage - the gate-source capacitance of transistor T_{in2}. This neglect is only justified if:

$C_1 \gg C_{gs}$ (52b)

Stability

Let us now calculate the parameters of the circuit C_1, g_{m1} and g_{m2} in order to obtain the rise time of 2 ns (comparable to the single-stage amplifier) and a step response without oscillations.

$$\tau_{r,B} = 2\text{ ns} \qquad (52c)$$

The condition for a step response without overshoot is (27):

$$\tau_{2,B} < \frac{1}{4}\frac{\tau_{1,B}}{|\beta A_{OL,DC}|}$$

It follows:

$$\tau_{1,B} > \frac{4|\beta A_{OL,DC}|R_{load}C_{load}}{A_2} = 4\beta A_1 R_{load}C_{load} \qquad (53)$$

This condition can be achieved by dimensioning C_1 as follows:

$$\tau_{1,B} = A_2 r_{out1}C_1 > 4\beta A_1 R_{load}C_{load} \Rightarrow C_1 > \frac{4\beta g_{m1}}{g_{m2}}C_{load} \qquad (54)$$

The rise time of step response is:

$$\tau_{r,B} \sim \frac{\tau_{1,B}}{\beta A_{OL,DC}} = \frac{A_2 r_{out1}C_1}{\beta g_{m1} r_{out1} A_2} = \frac{C_1}{\beta g_{m1}} > \frac{4\beta g_{m1}C_{load}}{\beta g_{m1} g_{m2}} = \frac{4C_{load}}{g_{m2}} \qquad (55)$$

From the right-hand side of (55) we obtain the necessary transconductance g_{m2} to achieve the minimum time constant of 2 ns:

$$\frac{4C_{load}}{g_{m2}} = 2\text{ns} \Rightarrow g_{m2} = 4\frac{100\text{pF}}{2\text{ns}} = 200\text{mS}$$

This is the same as our initial value.

Let us now calculate the gate-source capacitance of T_{in2}. To achieve the transconductance of 200 mS we need 200 standard amplifiers in parallel. We assume that a standard amplifier for the second stage has the capacitance C_{gs} of about 10 fF. The total gate-source capacitance of T_{in2} (consists of 200 standard transistors in parallel) is then:

$$C_{gs2} = 200 \times C_{gs,standard} = 200 \times 10\text{ fF} = 2\text{ pF}$$

In order for our formulas to be correct, condition (52b) must be fulfilled:

$$C_1 \gg C_{gs} = 2\text{ pF}$$

We set C_1 = 4 pF.

From the left-hand side of Equation (55), we can determine the transconductance g_{m1} required to achieve a time constant of 2ns while also ensuring a step response without oscillations.

$$\frac{C_1}{\beta g_{m1}} = 2\mathrm{ns} \Rightarrow g_{m1} = \frac{4\ \mathrm{pF}}{0.02 \times 2\ \mathrm{ns}} = 100\ \mathrm{mS}$$

Since a standard amplifier has the transconductance of 1mS, we need to connect 100 amplifiers in parallel for the first stage.

The following table summarizes the results:

Generic circuit	**Implemented circuit**	**Value**
R_1	r_{out1}	50kΩ/100
R_2	R_{load}	100Ω
C_2	C_{load}	100pF
C_1	C_1	4pF
g_{m1}	g_{m1}	1mS×100
g_{m2}	g_{m2}	200mS
A_1	$g_{m1}r_{out1}$	50
A_2	$g_{m1}R_{load}$	-20
βA	$\beta A_1 A_2$	20

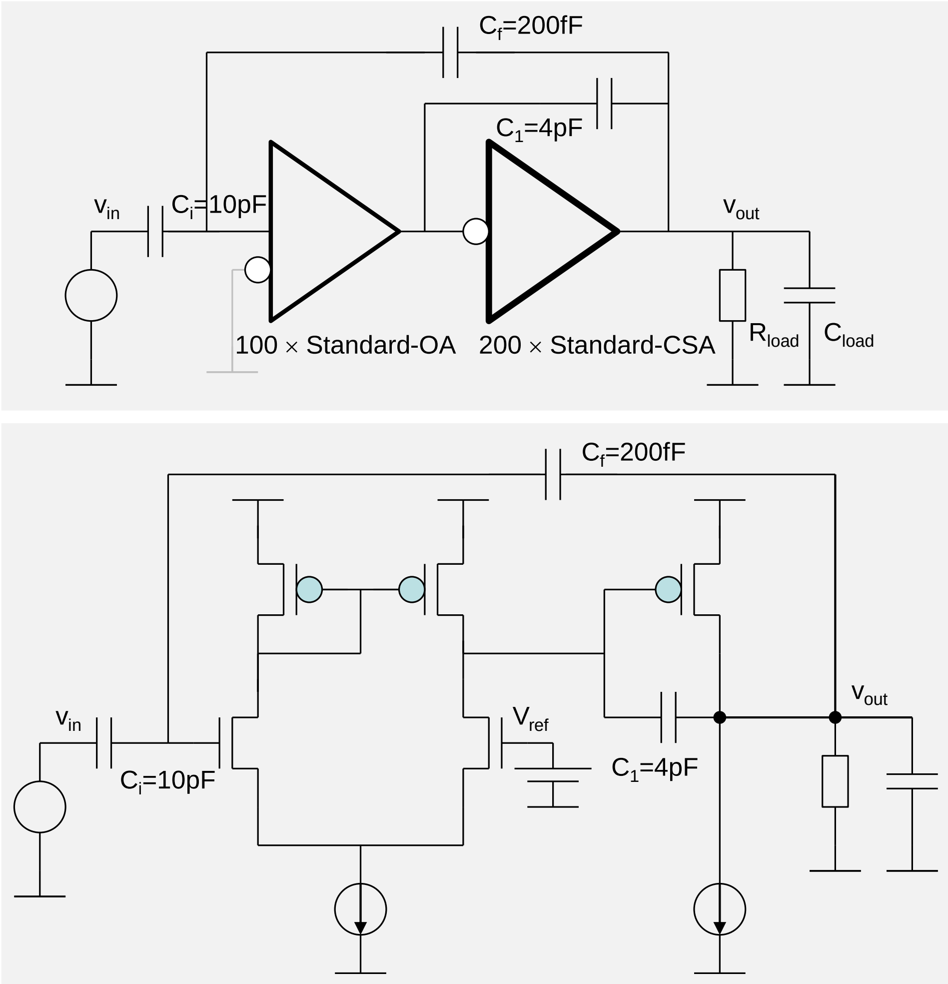
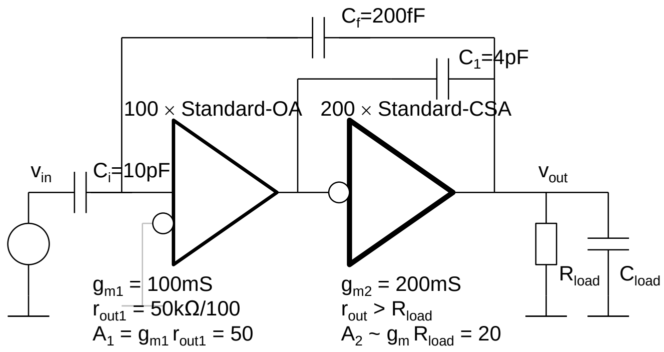


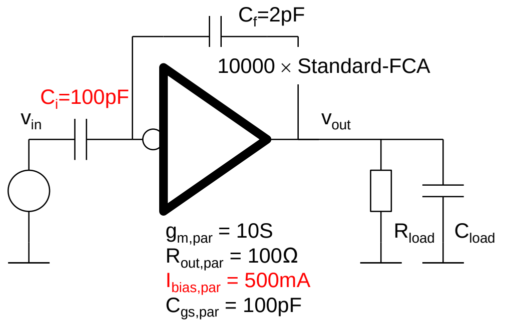
Figure 23: Inverting voltage amplifier with two amplifying stages - complete circuit diagram

Figure 23 shows the complete circuit. The DC voltage source V_{ref} can be implemented as a voltage divider (connected to GND and VDD).

Conclusion: The two-stage amplifier meets the specifications for open loop amplification and has about 33× less power consumption than the single-stage amplifier. The rise time is 2× larger than that of the single-stage amplifier.



Parameter	Wert
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20
τ_r	$4C_{load}/g_{m2}$ = 2ns
I_{bias}	(300 I_0) 30mA



Parameter	Wert
C_{load}	100pF
R_{load}	100Ω
A_{FB}	<50
A_{OL}	500
βA	10
τ_r	$2A_{FB}C_{load}/g_m$=1ns
I_{bias}	(10000 I_0) 500mA

Figure 24: Comparison between voltage amplifiers with two stages and frequency compensation (top) and with one stage (bottom). Disadvantages are marked in red. OA - operational amplifier, CSA - common source amplifier, FCA - folded cascode amplifier.

Miller effect

If the capacitor C is connected between the input and the output of a voltage amplifier with negative gain (-A), its capacitance is increased by ~ A (Figure 25).

A resistor R connected to this circuit creates the time constant

$\tau_1 = R \times A \times C$.

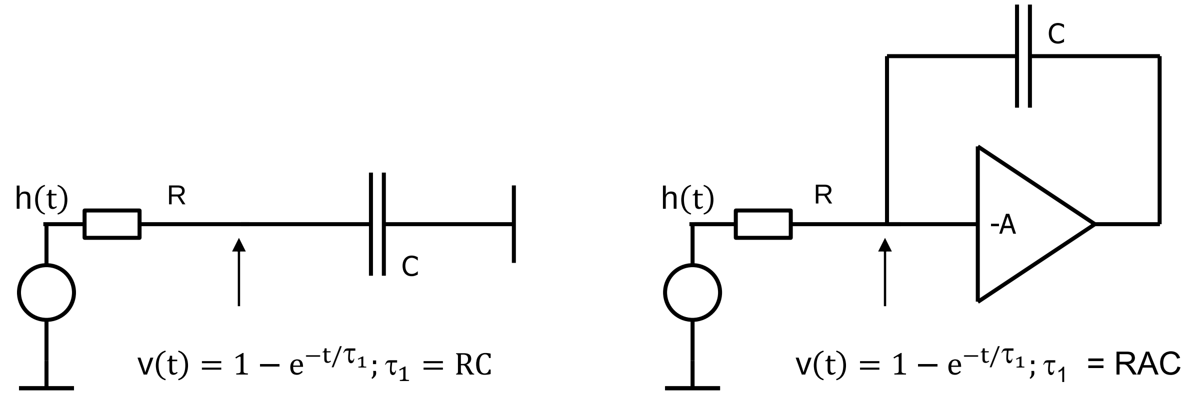


Figure 25: Comparison between time constants. Left: R sees capacitance C. Right: R sees larger capacitance.

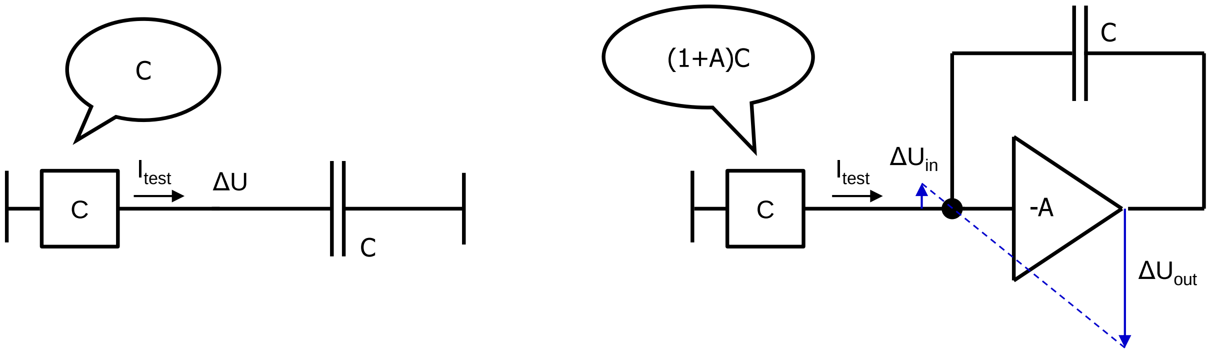


Figure 26: Miller effect, increase of C

Figure 26 shows why the capacitance is increasing.

A **C-meter** measures capacitance by generating a test current I_{test} and measuring how much the voltage across the capacitor (ΔU) increases during a time interval ΔT (Figure 26, left). The capacitance is determined by

$$I_{test} = C\frac{\Delta U}{\Delta T} \Rightarrow C = I_{test}\frac{\Delta T}{\Delta U}$$

A smaller voltage change therefore corresponds to a larger capacitance.

Let us now assume that exactly the same current flows into the capacitor **with** the amplifier (Figure 26, right). The voltage **across the capacitor itself** after the time interval ΔT is the same as in the case without the amplifier, because the same current charges the same physical capacitor.

$$\Delta U = \frac{I_{test}}{C} \Delta T$$

The voltage at the input of the amplifier changes by approximately:

$$\Delta U_{in} = \frac{\Delta U}{A+1} \ll \Delta U$$

The voltage at the output changes by:

$$\Delta U_{out} = -\Delta U \frac{A}{A+1} \sim \Delta U$$

The difference ΔU_{in} - ΔU_{out} is U.

Since the C-meter measures a voltage change that is A + 1 smaller than ΔU, it interprets this as a capacitance that is A + 1 larger than C.

If we connect a resistor to the input of the amplifier with C, the amplifier behaves as a large capacitor with the capacitance (A + 1) C. The resulting time constant is correspondingly large. This increase in apparent capacitance is known as the Miller effect.

Let us examine the circuit of Figure 20 again and try to understand its behavior.

The transfer function was given in Equation (52):

$$A_{OL} = -\frac{A}{\left(1 + s\frac{T_2}{A_2}\right)(1 + sA_2T_1)} = -\frac{A}{(1 + s\tau_{2,B})(1 + s\tau_{1,B})}$$

with

$T_1 = R_1 C_1$; $T_2 = R_2 C_2$; $A_2 = g_{m2}R_2$

The derivation of this transfer function was relatively long. Since we introduced the Miller effect, we can better understand the time constants. The circuit of Figure 20 can have been drawn in a simplified manner as in Figure 27.

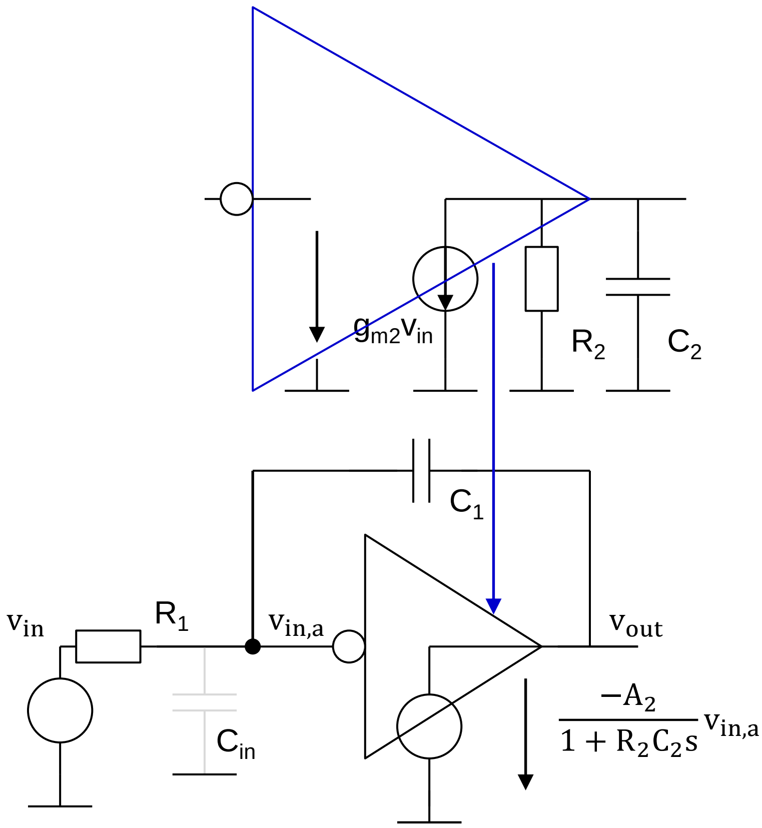


Figure 27: Integrator

The first time constant $\tau_{1,B}$, B arises because R_1 is connected to the capacitors. As described above, the capacitance C_1 is increased by a factor of $1 + A_2 \sim A_2$ due to the Miller effect. Resistor R_1 therefore "sees" capacitance $A_2\, C_1$. The time constant is $\tau_{1,B}$, B is:

$$\tau_{1,B} = R_1C_1A_2$$

The shorter time constant $\tau_{2,B}$ is due to feedback. Without feedback, the time constant would be $T_2 = R_2C_2$. We have seen in previous lectures that negative feedback influences the output resistance (or output impedance) by reducing the impedance by $1 - \beta A(i\omega)$[2]. If $\beta A(i\omega)$ is a real number $\beta A(i\omega) \equiv \beta A$, the time constant associated with the output resistance is also reduced by the same factor $1 - \beta A$. In our example this means:

$\tau_{2,B} = \frac{T_2}{1-\beta A}$

It holds $\tau_{2,B} < T_1$. For $\omega > 1/T_1$ the loop gain is real number:

$\beta A(i\omega) \equiv \beta A = -A_2$

R_1 can be neglected in the serial connection of R_1 and C_1.

Therefore:

$\tau_{2,B} = \frac{T_2}{-\beta A} = \frac{T_2}{A_2}$

If we have an input capacitance C_{in} (this capacitance would be e. g. the gate-source capacitance of the input transistor), the time constants change as follows:

Resistor R_1 now sees the effective capacitance A_2C_1 in parallel with C_{in}. Therefore, the first time constant becomes:

$$\tau_{1,B} \sim R_1(A_2C_1 + C_{in}) = A_2T_1\left(1 + \frac{C_{in}}{C_1A_2}\right)$$

The capacitance C_{in} also affects $\beta A(s)$. For $\omega > 1/T_1$, we have:

$$\beta A(s) \equiv \beta A \sim -A_2\frac{C_1}{C_1 + C_{in}}$$

The second time constant then becomes:

$$\tau_{2,B} \sim \frac{T_2}{-\beta A} = \frac{T_2}{A_2}\left(1 + \frac{C_{in}}{C_1}\right)$$

We see that the input capacitance has a relatively strong influence on the second time constant.

The circuit consisting of a voltage amplifier with capacitive feedback (Figure 27) is an important example. It is a slow voltage amplifier with a large DC gain ($-A_2$) and a long time constant $A_2R_1C_1$. For time intervals that are much shorter than the time constant τ_1, the circuit behaves like an integrator.

The following applies:

[2] See the section Blackman's formula in DAS_2025_Text_8_casc_English.docx

$$u_{out}(s) = \frac{A_2}{(sA_2R_1C_1+1)\left(s\frac{T_2}{A_2}+1\right)} u_{in}(s) \xrightarrow{A_2=\infty} u_{out}(s) = \frac{u_{in}(s)}{sR_1C_1} \quad (56)$$

Or in time domain:

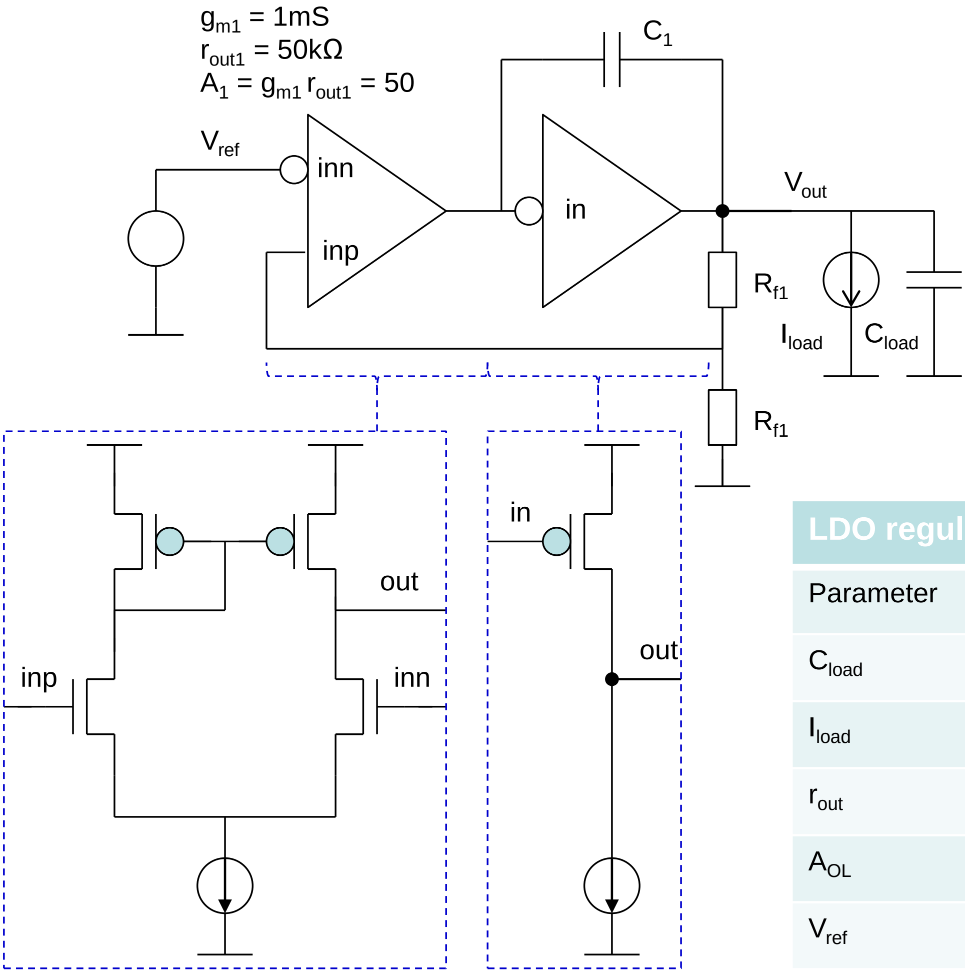
$$u_{out}(t) = \frac{1}{RC}\int u_{in}(t)dt \quad (57)$$

τ is the time constant of the amplifier. In the case of the second amplifier stage:

$$u_{out}(t) = \frac{1}{R_1C_1}\int u_{in}(t)dt \quad (58)$$

Linear regulator

Figure 28 shows the linear regulator implemented as a two-stage amplifier with frequency compensation.



LDO regulator	
Parameter	Wert
C_{load}	10nF
I_{load}	0-100mA
r_{out}	0.1Ω
A_{OL}	1000
V_{ref}	1V

Figure 28: Linear regulator with a two-stage amplifier and frequency compensation

The first stage (an operational amplifier with a current mirror) has the same dimensions as in the voltage amplifier:

g_{m1} = 1 mS

r_{out1} = 50 kΩ

$A_1 = g_{m1}\, r_{out1} = 50$

The second stage is based on the common source amplifier with an open loop gain of 50.

The overall gain is then:

$A = A_1\, A_2 = 2500.$

In order to simplify the analysis, let us choose the following values:

$R_{f1} = 0$ and $R_{f2} = \infty$. (59)

We will determine the transconductance g_{m2} required to achieve an output resistance with feedback of 0.1 Ω:

$r_{out} = 0.1\ \Omega$. (60)

First, let us calculate the DC voltage V_{out} using Mason's formula. Figure 29 shows the test circuits for calculating A_{IN}, β and A_{OL}.

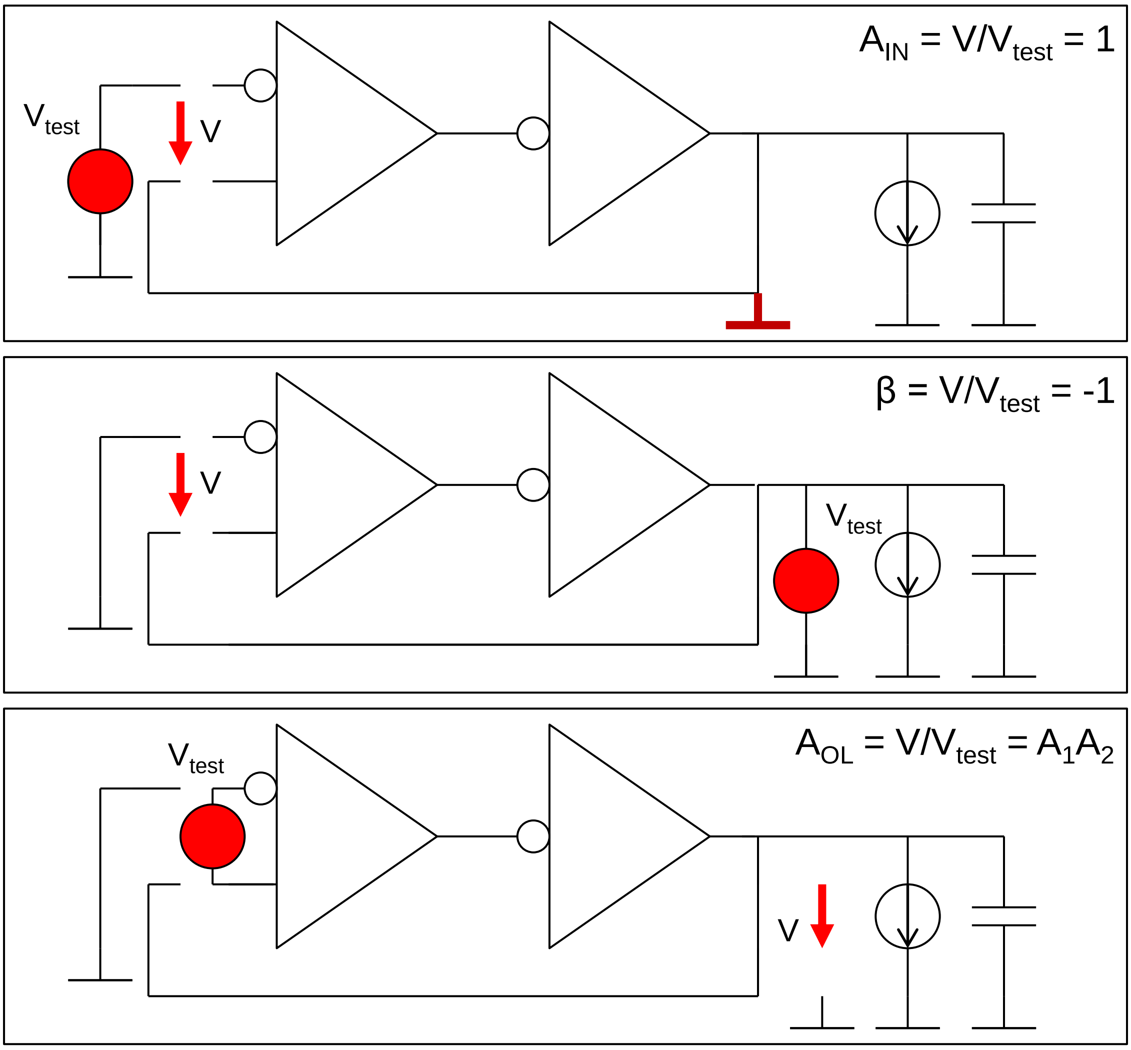


Figure 29: Linear regulator - test circuits for A_{IN}, β and A_{OL}

The following applies:

A_{IN} = 1 (Figure 29, top),

β = -1 (Figure 29, middle),

$A_{OL} = A_1A_2$ (Figure 29, bottom)

If we insert these terms into Mason's formula, we obtain:

$$V_{out} = \frac{A_1A_2}{1+A_1A_2}V_{in} \sim V_{in} \qquad (61)$$

Let us calculate the output resistance (small signal resistance). We use Blackman's formula.

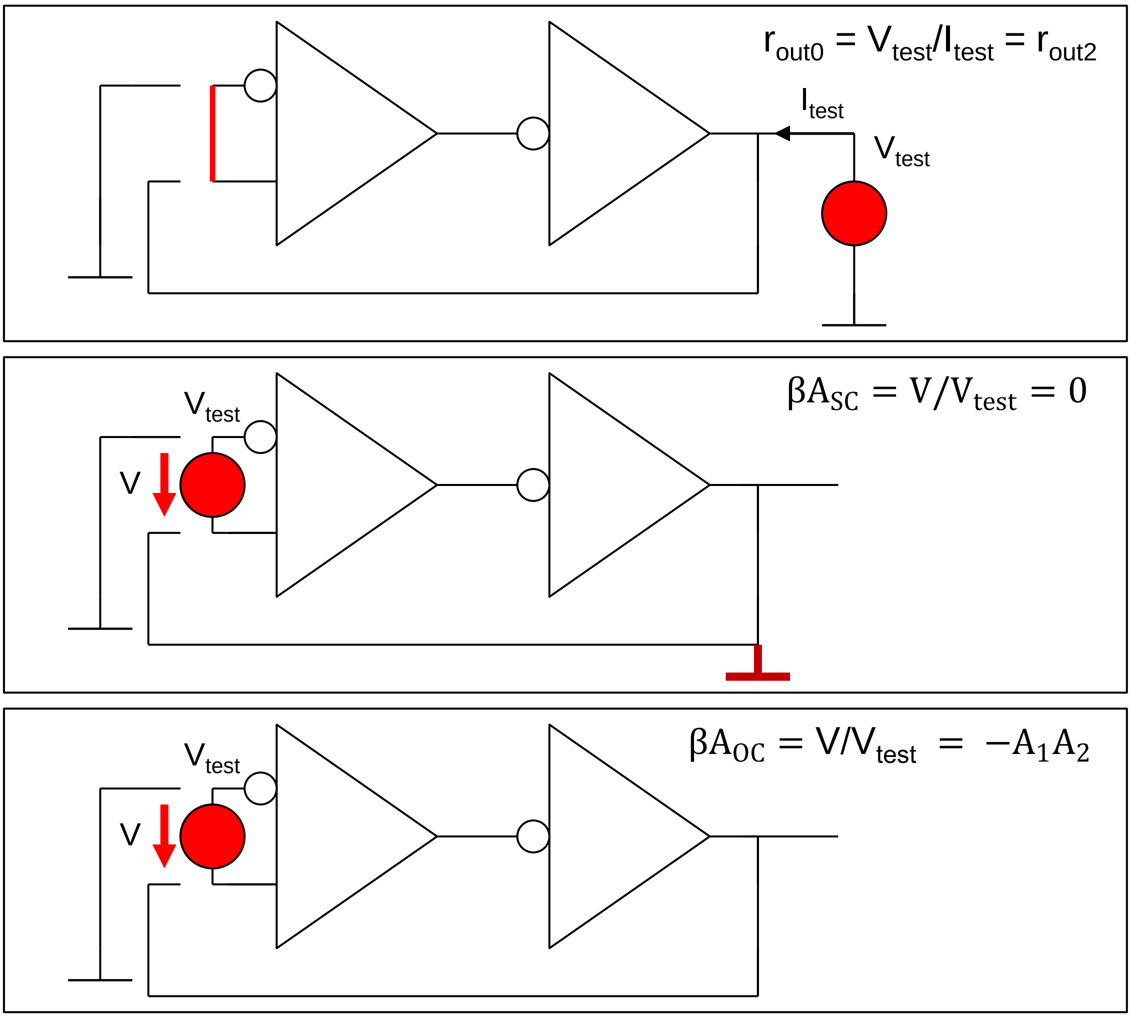


Figure 30: Linear regulator - test circuits for r_{out0}, βA_{SC} and βA_{OC}

$$r_{out} = r_{out0}\frac{1-\beta A_{SC}}{1-\beta A_{OC}} \quad (62)$$

Figure 30 shows the test circuits for calculation of r_{out0}, βA_{SC} and βA_{OC}.

The factors have the following values:

$$r_{out0} = r_{out2};\ \beta A_{SC} = 0;\ \beta A_{OC} = -A_1 A_2 \quad (63)$$

If we insert these terms into Blackman's formula (61) we obtain:

$$r_{out} = \frac{r_{out2}}{A_1 A_2} = \frac{1}{A_1 g_{m2}} \quad (64)$$

Assuming $A_1 = 50$, we can calculate the required transconductance g_{m2} to achieve $r_{out} = 0.1\ \Omega$.

$$0.1\Omega = \frac{1}{50 g_{m2}} \Rightarrow g_{m2} = 200\text{mS} \qquad (65)$$

We need to connect 200 standard amplifiers (each gm = 1mS) in parallel.

Recall that the second amplifier stage has $r_{out} = 250\Omega$.

The feedback allows us to achieve a much lower output resistance.

Stability

Let us dimension C_1 to prevent oscillations. From Equation (54), we calculate:

$$C_1 > \frac{4\beta g_{m1}}{g_{m2}} C_{load} = 4\frac{1\text{mS}}{200\text{mS}} 10\text{nF} = 200\text{pF} \qquad (66)$$

The rise time of the step response can be calculated using Equation (55):

$$\tau_r = \frac{C_1}{\beta g_{m1}} > \frac{4C_{load}}{g_{m2}} = \frac{4\times 10\text{nF}}{200\text{mS}} = 200\text{ns} \qquad (67)$$

The time constant τ_r indicates, among other things, how quickly the regulator can respond to changes in the load current I_{load}.

We can achieve a faster rise time by increasing g_{m2} and g_{m1}.

Input capacitance

Using Blackman's formula, it can also be calculated that the input source sees a very small capacitive load:

$$C_{in} = \frac{C_{gs,par}}{1+A_1 A_2} \quad (68)$$

$C_{gs,ser}$ is the series combination of the gate-source capacitances of the two input transistors in the operational amplifier. This result is valid for frequencies smaller than $1/\tau_r$.

How can we explain that the input capacitance is smaller than $C_{gs,ser}$? The feedback regulates $V_{ref} = V_{out}$ so that the charge stored in $C_{gs,ser}$ does not change. Because of this, the input source does not see the effect of $C_{gs,ser}$ (Figure 31).

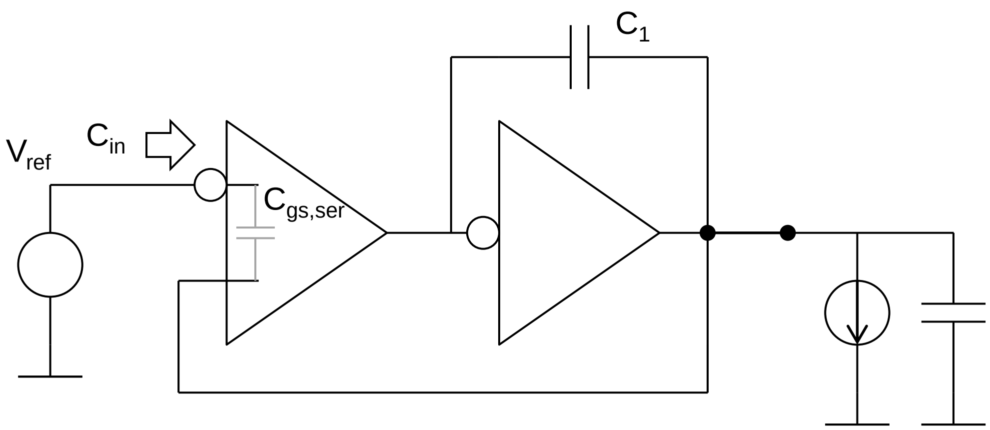
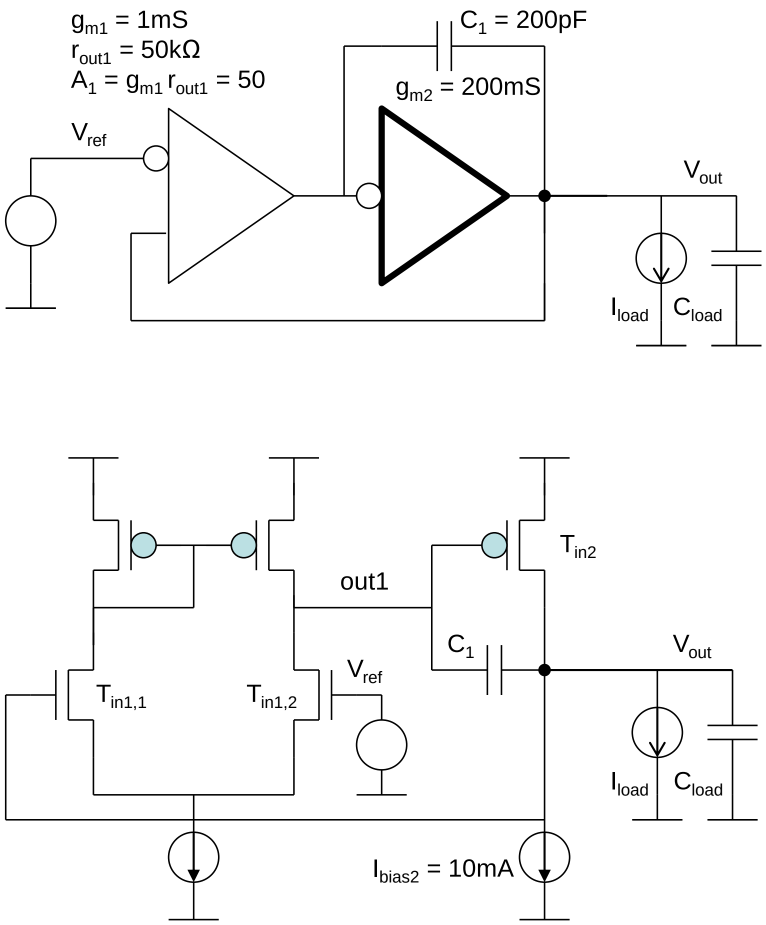


Figure 31: Input capacitance



LDO regulator	
Parameter	Value
C_{load}	10nF
I_{load}	0-100mA
r_{out}	0.1Ω
A_{OL}	1000
V_{ref}	1V
g_{m1}	1mS
g_{m2}	200mS
C_1	200pF
τ_r	200ns

Figure 32: Linear regulator - complete circuit diagram

Figure 32 shows the complete circuit diagram of the linear regulator.

DC analysis

So far, we have focused on small-signal analysis and have not considered that the load current can influence the operating point of the second amplifier stage.

Note that the load current I_{load} also flows through the transistor T_{in2}. The transconductance of T_{in2} (g_{m2}) is proportional to I_{load}, for I_{load} > 10 mA.

This has a beneficial effect on the circuit: the gain A_2 increases and the output resistance r_{out} decreases.

Transistor T_{in2} must be dimensioned so that its width-to-length ratio (W/L) is large enough to ensure that, at $I_{load} = I_{load, max}$ its $| V_{gs} |$ does not become too large. Otherwise, $T_{in1,2}$ might leave saturation, causing A_1 to decrease significantly.

Additional Topics

Source Follower

Figure 33 shows the source follower.

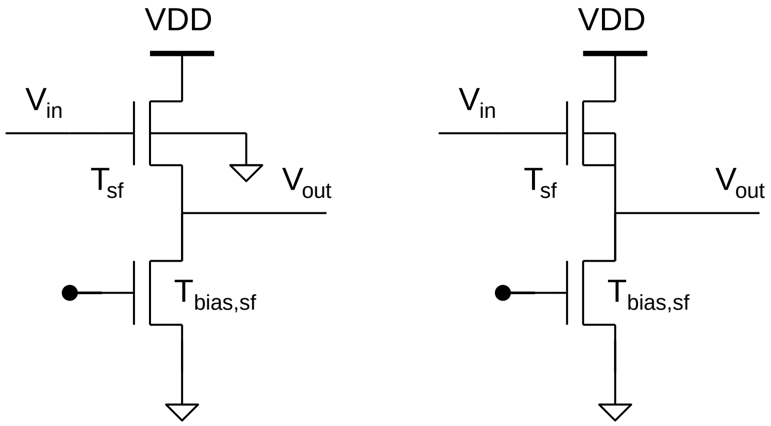


Figure 33: Source Follower. Left: Variant with $V_{b,sf}$=0 V. Right: Variant with $V_{b,sf}$=$V_{s,sf}$.

Alternatively, this circuit is called a common-drain amplifier. The circuit consists of an NMOS transistor T_{sf} and an NMOS current source $T_{bias,sf}$. The drain of T_{sf} is connected to a constant potential (e.g., the supply voltage VDD). This ensures that T_{sf} operates in saturation.

DC Analysis

Let us first perform the DC analysis.

We have:

$$V_{out} = V_{in} - V_{gs,sf} \quad (69)$$

First, assume that the substrate of T_{sf} is connected to ground (Figure 33, left). The source potential, however, is not zero. Therefore, the body effect plays a role in this circuit, and we will take it into account in the analysis.

The transistor current $I_{DS,sf}$ is given by:

$$I_{ds,sf} = \frac{1}{2}\mu C'_{ox}\frac{W}{L}\left(V_{gs,sf} - V_{thsb}\right)^2 = \frac{1}{2}\mu C'_{ox}\frac{W}{L}\left(V_{gs,sf} - (n-1)V_{sb} - V_{th}\right)^2 \quad (70)$$

with

$$V_{out} = V_{sb}$$

The factor n is the slope factor, typically 1.25.

The term in parentheses can be simplified as follows:

$$V_{gs,sf} - (n-1)V_{sb} - V_{th} = V_{in} - V_{out} - (n-1)V_{out} - V_{th} = V_{in} - nV_{out} - V_{th} \qquad (71)$$

The current $I_{DS,sf}$ is constant because a constant current source ($T_{bias,sf}$) is connected to Tsf:

$$I_{ds,sf} = I_{bias} \quad (72)$$

Therefore, the term in parentheses in (70) is constant. Substituting (70) into (69) and considering (71), we get:

$$V_{in} - nV_{out} - V_{th} = \sqrt{\frac{2I_{bias}L}{\mu C'_{ox}W}}$$

From this, it follows:

$$V_{out} = \frac{1}{n}\left(V_{in} - V_{th} - \sqrt{\frac{2I_{bias}L}{\mu C'_{ox}W}}\right) \qquad (73)$$

The voltage gain is then:

$$dV_{out}/dV_{in} = 1/n \qquad (74)$$

As mentioned, a typical value for n is 1.25.

In some CMOS processes, it is possible to isolate the NMOS substrate from the p-type wafer and from other NMOS substrates (Figure 34). The NMOS transistor is then placed in a p-well. A deep n-well isolates the p-well from the p-type wafer. In this case, the NMOS substrate (p-well) can have a different potential than the ground potential. We can then connect the source and substrate together to avoid the body effect (Figure 33, right).

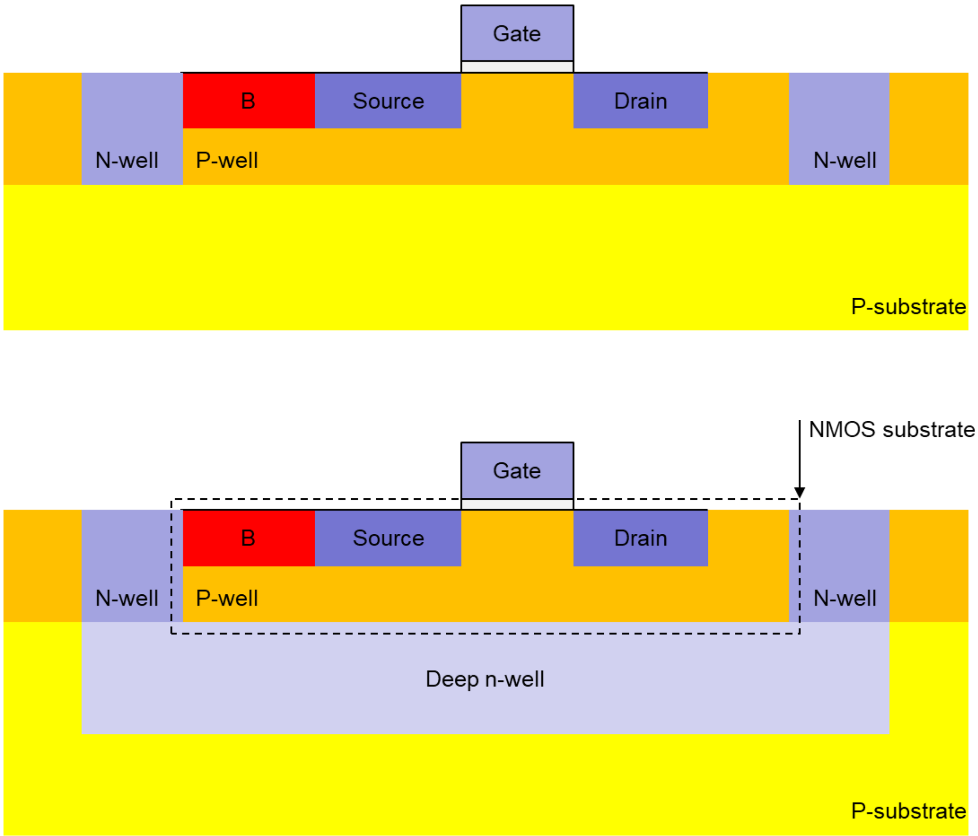


Figure 34: Top: Standard NMOS. Bottom: NMOS substrate isolated from the p-type wafer using a deep n-well.

This leads to $V_{SB} = 0$. In this case, we have:

$$V_{out} = (V_{in} - V_{th} - \sqrt{\frac{2I_{bias}L}{\mu C'_{ox}W}})$$

The gain of the source follower is then 1. Since the source potential follows the input potential, the circuit is called a source follower. A source follower also acts as a level shifter.

AC Analysis

Figure 35 shows the small-signal circuit. The schematic is similar to that of a non-inverting amplifier with feedback.

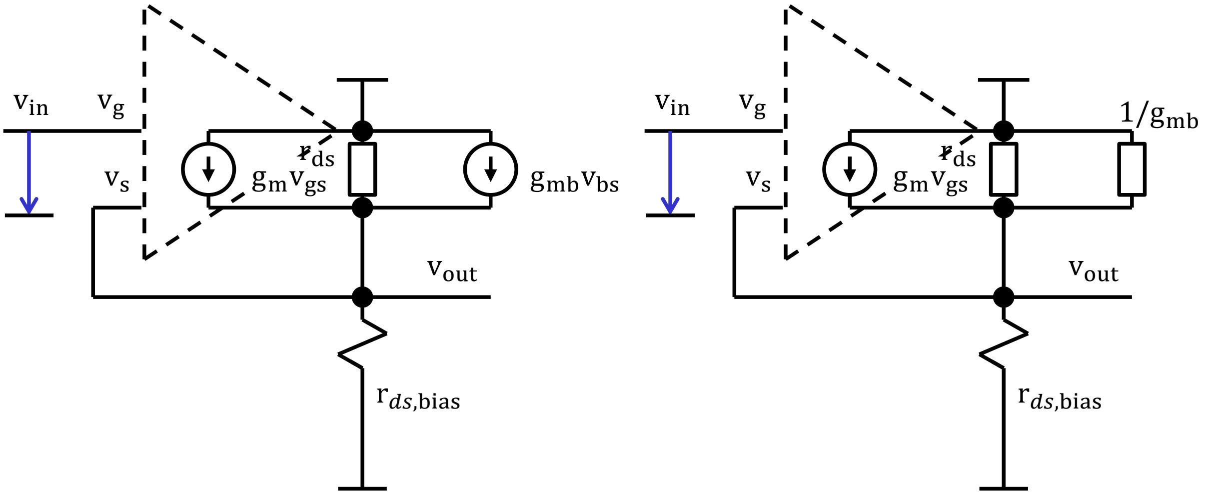


Figure 35: Source follower small-signal model. Left: Body effect modeled with a current source. Right: Body effect modeled with a resistor.

The current source $g_{mb}v_{BS}$ models the body effect (Figure 35, left). This current source can be replaced by a resistor $1/g_{mb}$ (Figure 35, right).

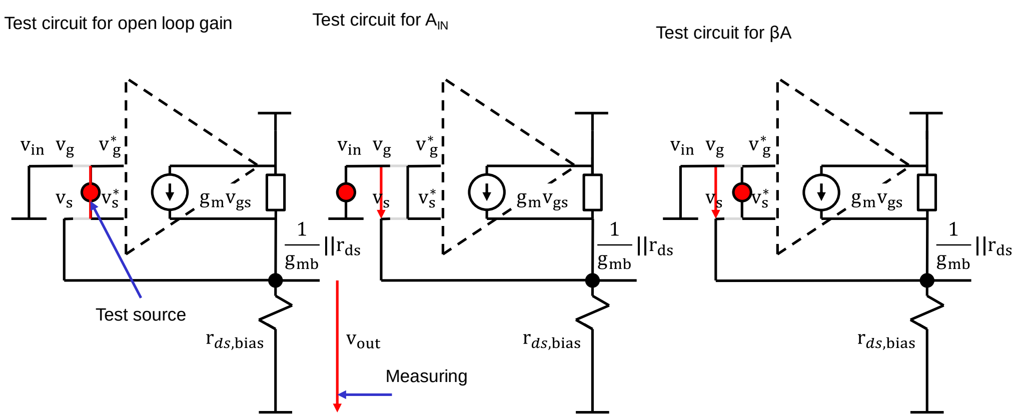


Figure 36: Test circuits for calculating the gain of the source follower.

Let us first calculate the gain with feedback. We use Mason's formula:

$$A_{fb} = \frac{A_{IN}A_{OL}}{1-\beta A}$$

Figure 36 shows the circuits used to calculate A_{OL}, A_{IN}, and βA.

The terms are:

$$A_{OL} = g_m\left(\frac{1}{g_{mb}}||r_{ds,bias}||r_{ds}\right) \sim \frac{g_m}{g_{mb}} = \frac{1}{n-1}$$

$$A_{IN} = 1$$

$$\beta A = -g_m\left(\frac{1}{g_{mb}}||r_{ds,bias}||r_{ds}\right) \sim -\frac{g_m}{g_{mb}} = -\frac{1}{n-1}$$

Substituting these terms into Mason's formula gives:

$$A_{fb} = \frac{\frac{1}{n-1}}{1+\frac{1}{n-1}} = \frac{1}{n} \qquad (75)$$

This is the same result as in Equation (73).

If we can short the source and substrate, the resistance $1/g_{mb}$ disappears, and the formulas for A_{OL} and βA simplify:

$$A_{OL} = g_m(r_{ds}||r_{ds,bias})$$

$$\beta = -g_m(r_{ds}||r_{ds,bias})$$

The gain of the source follower then becomes:

$$A_{fb} = \frac{g_m(r_{ds}||r_{ds,bias})}{1+g_m(r_{ds}||r_{ds,bias})} \sim 1$$

We would also obtain this result from Equation (74) by setting n = 1.

The output resistance can be calculated using Blackman's formula:

$$r_{out} = r_{out0}\frac{1-\beta A_{SC}}{1-\beta A_{OC}}$$

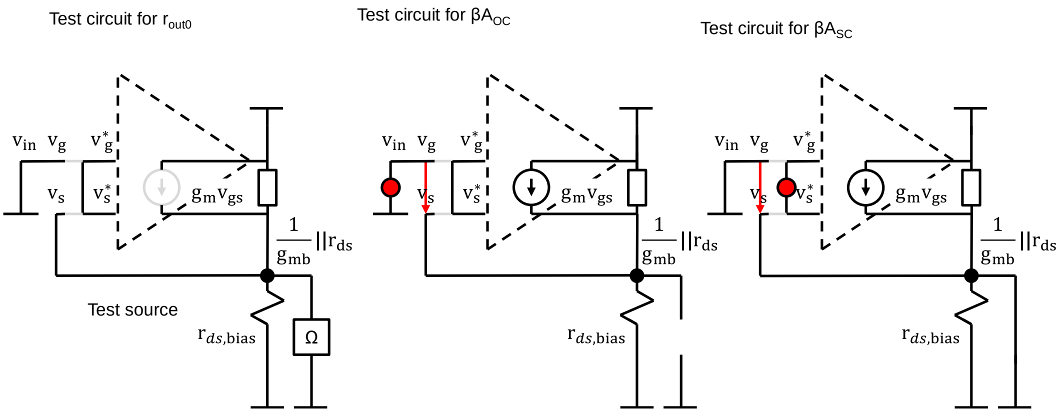


Figure 36: Test circuits for calculating r_{out}.

Figure 37 shows the test circuits for calculating r_{out0}, βA_{OC} und βA_{SC}.

The factors have the following values:

$$r_{out0} = \frac{1}{g_{mb}}||r_{ds,bias}||r_{ds} \sim \frac{1}{g_{mb}} = \frac{1}{g_m}\frac{1}{n-1}; \ \beta A_{SC} = 0; \ \beta A_{OC} \sim -\frac{g_m}{g_{mb}} = -\frac{1}{n-1}$$

If we insert these terms into Blackman's formula, we get:

$$r_{out} = \frac{1}{g_m}\frac{1}{n-1}\frac{1}{1+\frac{1}{n-1}} = \frac{1}{g_m}\frac{1}{n} \quad (76)$$

The output resistance is therefore relatively small.

In the case where $V_S = V_B$, we have:

$$r_{out} = \frac{1}{g_m}$$

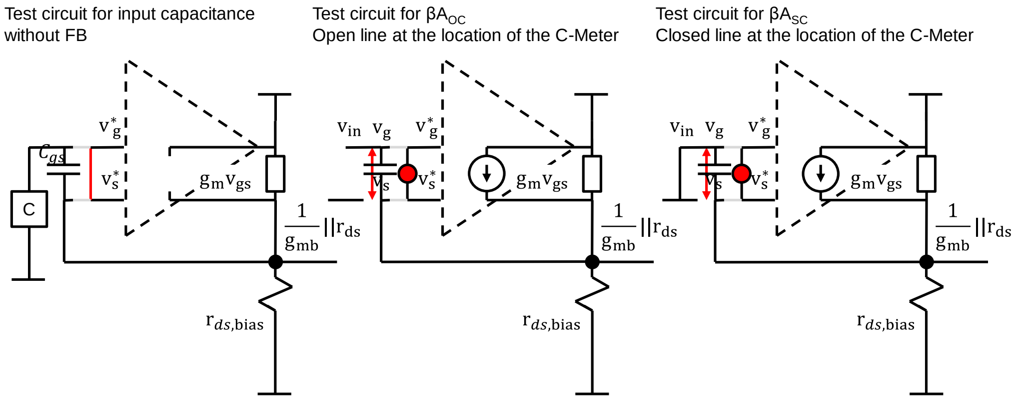


Figure 37: Test circuits for calculation of C_{in}.

Using Blackman's formula, we can also calculate the capacitive load C_{in} seen by the input source. Figure 38 shows the test circuits for the corresponding factors.

For the case $V_B = 0$, we have:

$$C_{in} = \frac{C_{gs,in}}{1+\frac{g_m}{g_{mb}}} = \frac{C_{gs,in}}{1+\frac{1}{n-1}} = \frac{n-1}{n}C_{gs,in} \quad (77)$$

For the case $V_S = V_B$, we get:

$$C_{in} = \frac{C_{gs,in}}{1+g_m(r_{ds}||r_{ds,bias})} \sim \frac{C_{gs,in}}{g_m(r_{ds}||r_{ds,bias})} \quad (78)$$

The input capacitance is therefore relatively small.

The source follower has a voltage gain of approximately 1, a low output resistance, and a high input impedance. The circuit functions as an impedance converter. It is used to "buffer" a signal source. Another term for an impedance converter with a gain of 1 is a buffer. The circuit protects a signal source from the effects of load impedances.

Application

The main application of the source follower is as the output stage of an amplifier. All amplifier types presented so far had no dedicated output stage. Their output was the drain of the input or load transistor, so rout was proportional to r_{ds} and relatively high.

Such amplifiers are called transconductance amplifiers, because they behave like current sources. For example, the operational amplifier with a current mirror could also be called an operational transconductance amplifier (OTA) — Figure 39, left. By adding an output stage to the OTA, we obtain a true low-output-impedance operational amplifier — Figure 39, right.

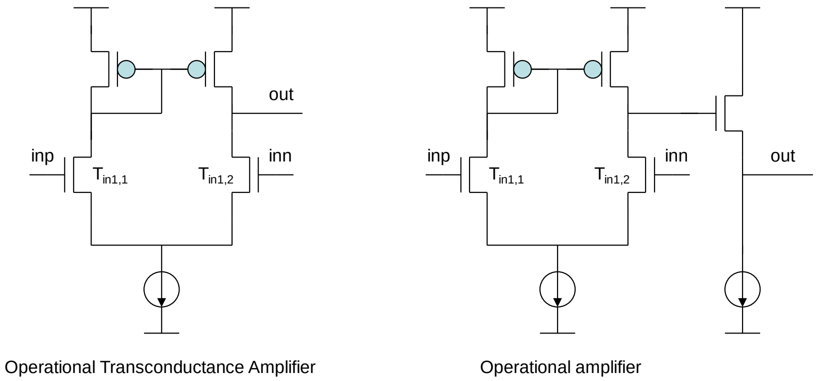


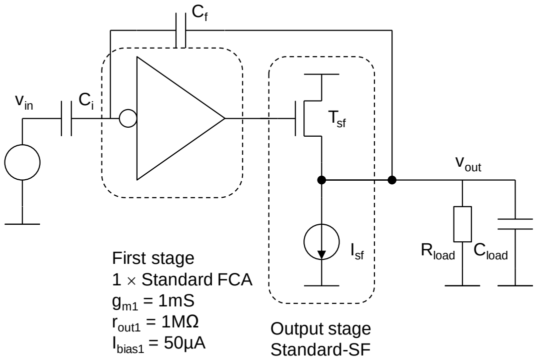
Figure 38: Transconductance amplifier (left) and standard voltage amplifier (right).

Let us illustrate the effect of an output stage with the following example.

Voltage amplifier based on an amplifier with an output stage

In previous chapters, we described the implementation of a voltage amplifier using a single-stage amplifier. The load capacitance and resistance were C_{load} = 100 pF and R_{load} = 100 Ω. We had to connect 10,000 standard amplifiers (folded cascodes) in parallel to reduce the output resistance. This resulted in very high current consumption. A two-stage amplifier performed better.

Now, let us try another solution. We use a folded cascode as the input stage and connect a source follower as the output stage to its output (Figure 40).



Voltage amplifier	
Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20

Figure 40: Voltage amplifier with a folded cascode (FCV) as the input stage and a source follower (SF) as the output stage.

We start with a standard source follower, which has a bias current I_{sf} = 50 µA and a transconductance $g_{m,sf}$ = 1 mS.

Assume that the substrate of T_{sf} is connected to ground.

The voltage gain of the source follower is:

$$A_{sf} = \frac{g_{m,sf}R_{sf}}{1+g_{m,sf}R_{sf}} \qquad (79)$$

with the resistance:

$$R_{sf} = R_{load} || \frac{1}{g_{mb,sf}} r_{ds,sf}\, r_{bias,sf} \approx R_{load} || \frac{1}{g_{mb,sf}} = R_{load} || \frac{1}{(n-1)g_{m,sf}} \qquad (80)$$

We will dimension the source follower so that the following condition holds:

$$R_{load} > \frac{1}{(n-1)g_{m,sf}}; \Rightarrow \ g_{m,sf} > \frac{1}{(n-1)R_{load}} = \frac{1}{0.25 \times 100\Omega} = 40mS \qquad (81)$$

In this case, Equation (79) simplifies to:

$$R_{sf} \sim \frac{1}{(n-1)g_{m,sf}} \qquad (82)$$

Substituting (81) into (78), we obtain the formula for the voltage gain:

$$A_{sf} \sim \frac{\frac{g_{m,sf}}{g_{mb,sf}}}{1+\frac{g_{m,sf}}{g_{mb,sf}}} = \frac{1}{n} \qquad (83)$$

The output resistance of the source follower is given by Equation (75):

$$r_{out,sf} = \frac{1}{n}\frac{1}{g_{m,sf}} \qquad (84)$$

From (79), it follows that:

$$r_{out,sf} < R_{load} \qquad (85)$$

Let us now calculate A_{OL} of the amplifier with the output stage. Figure 40 shows the test circuit

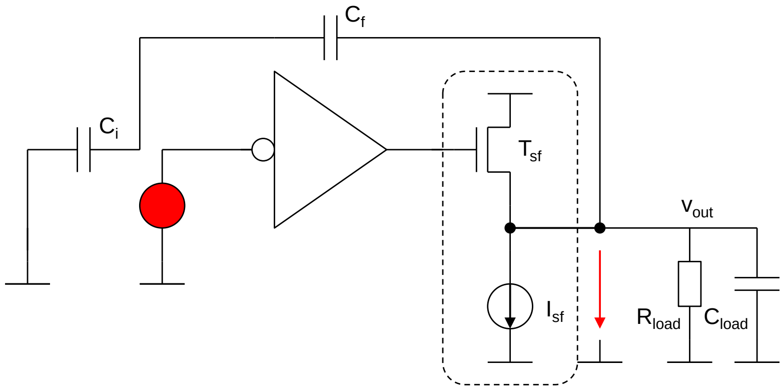


Figure 39: Test circuit A_{OL}.

The circuit is equivalent to the generic circuit of Figure 16 when the values from the following table are used:

Generic circuit	**Implemented circuit**
R_1	r_{out1}
R_2	$1/(ng_{m,sf})$
C_2	C_{load}
C_1	$C_{in,sf}$
g_{m1}	g_{m1}
g_{m2}	g_{m2}
A_1	$g_{m1}r_{out1}$
A_2	$1/n$

The open-loop gain is (see Equation 14):

$$A_{OL}(s) = \frac{-g_{m1}r_{out1}/n}{(1+sr_{out1}C_1)\left(1+\frac{sC_{load}}{ng_{m,sf}}\right)} = \frac{A_1/n}{(1+s\tau_{2,C})(1+s\tau_{1,C})} \qquad (86)$$

where C1 is the input capacitance of the source follower:

$$C_1 = C_{in,sf} \qquad (87)$$

Let us now calculate the circuit parameters g_{m1} and $g_{m,sf}$ in order to achieve a rise time of 2 ns and a step response without oscillations.

The condition for a step response without overshoot is (Equation 27):

$$\tau_{2,C} < \frac{1}{4}\frac{\tau_{1,C}}{|\beta A_{OL,DC}|}$$

From this it follows

$$\tau_{1,C} > \frac{4|\beta A_{OL,DC}|C_{load}}{ng_{m,sf}} = \frac{4\beta A_1 C_{load}}{g_{m,sf}}$$

and:

$$\tau_{1,C} = r_{out1}C_1 > \frac{4\beta A_1 C_{load}}{g_{m,sf}} \Rightarrow C_1 > \frac{4\beta g_{m1}}{g_{m,sf}}C_{load}$$

The rise time of the step response is:

$$\tau_{r,C} \sim \frac{\tau_{1,C}}{\beta A_{OL,DC}} = \frac{r_{out1}C_1}{\beta g_{m1} r_{out1}} = \frac{C_1}{\beta g_{m1}} > \frac{4\beta g_{m1} C_{load}}{\beta g_{m1} g_{m,sf}} = \frac{4C_{load}}{g_{m,sf}} \qquad (88)$$

From the right-hand side of (87), we get the required transconductance $g_{m,sf}$ to achieve a minimum time constant of 2 ns:

$$\frac{4C_{load}}{g_{m,sf}} = 2\text{ns} \Rightarrow g_{m,sf} = 4\frac{100\text{pF}}{2\text{ns}} = 200\text{mS} \qquad (89)$$

This value also satisfies the condition in (80).

Next, we calculate the gate-source capacitance of T_{sf}. To achieve a transconductance of 200mS, we need 200 standard source followers in parallel. The total gate-source capacitance of T_{sf} (consisting of 200 standard transistors, each with C_{gs} = 10fF) is:

$$C_{gs,sf} = 200 \times C_{gs,standard} = 200 \times 10 \text{ fF} = 2 \text{ pF}$$

The input capacitance of the source follower is then:

$$C_{in,sf} = \frac{n-1}{n} C_{gs,sf} = \frac{1.25-1}{1.25} 2 \text{ pF} = 400 \text{ fF}$$

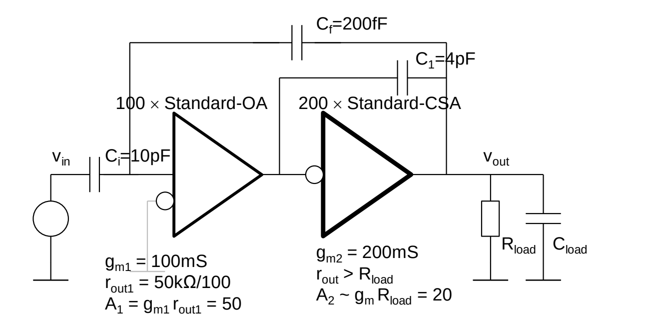
Hence:

$$C_1 = C_{in,sf} = 400 \text{ fF}$$

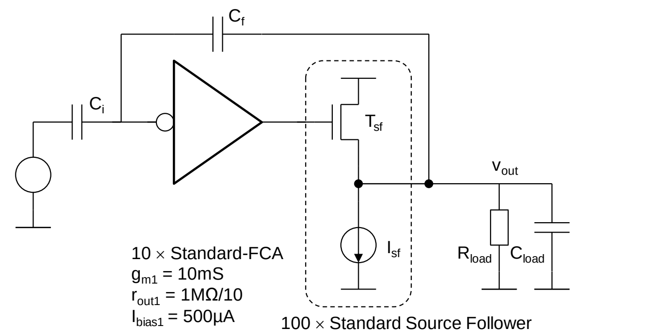
From the left-hand side of (87), we get the required transconductance g_{m1} to achieve the 2 ns time constant while avoiding oscillations in the step response:

$$\frac{C_1}{\beta g_{m1}} = 2\text{ns} \Rightarrow g_{m1} = \frac{400 \text{ fF}}{0.02 \times 2 \text{ ns}} = 10 \text{ mS}$$

Since a standard amplifier has a transconductance of 1 mS, we must connect 10 amplifiers in parallel for the input stage.



Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20
τ_r	$4C_{load}/g_{m2}$ = 2ns
I_{bias}	(201 I_0) 10mA



Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	<50
A_{OL}	500
βA	10
τ_r	$4C_{load}/g_{msf}$ = 2ns
I_{sf}	10mA

Figure 42: Comparison between the two-stage voltage amplifier with frequency compensation (top) and the amplifier with a folded cascode as the input stage and a source follower as the output stage (bottom). Disadvantages are marked in red. OV – operational amplifier, CSV – common-source amplifier, FCV – folded cascode amplifier.

Figure 42 shows the comparison between the two-stage voltage amplifier with frequency compensation (top) and the amplifier with a source follower as the output stage (bottom). Both circuits have the same rise time and similar current consumption.

In the case of the amplifier with an output stage, the input stage must be implemented as a folded cascode, and its gain must be very high. In the case of the two-stage amplifier, the gains of the individual stages can be lower.

The two-stage amplifier has a larger dynamic range at the output, as shown in Figure 43.

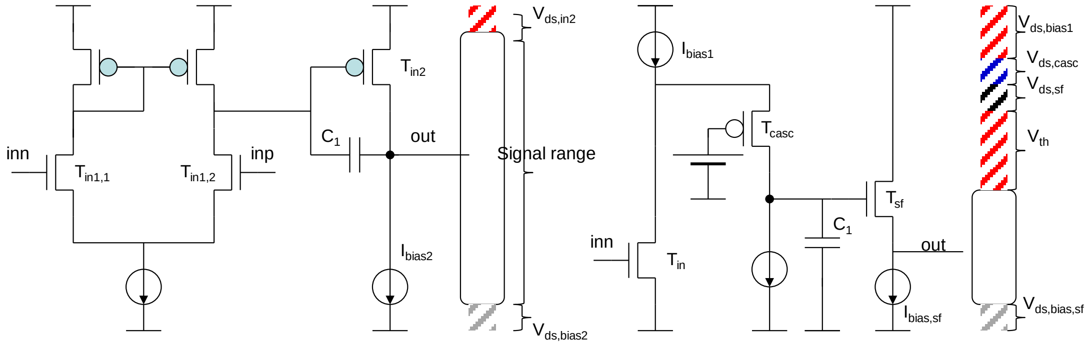


Figure 43: Signal range (dynamic range) for the two-stage amplifier (left) and the amplifier with a source follower (right).

Reference Voltage Generator

In this chapter, we will present a realization of the generator of reference voltage (the reference voltage source).

The reference voltage source should generate a voltage that is relatively independent of the supply voltage V_{IN} and of temperature.

Figure 40 shows the schematic.

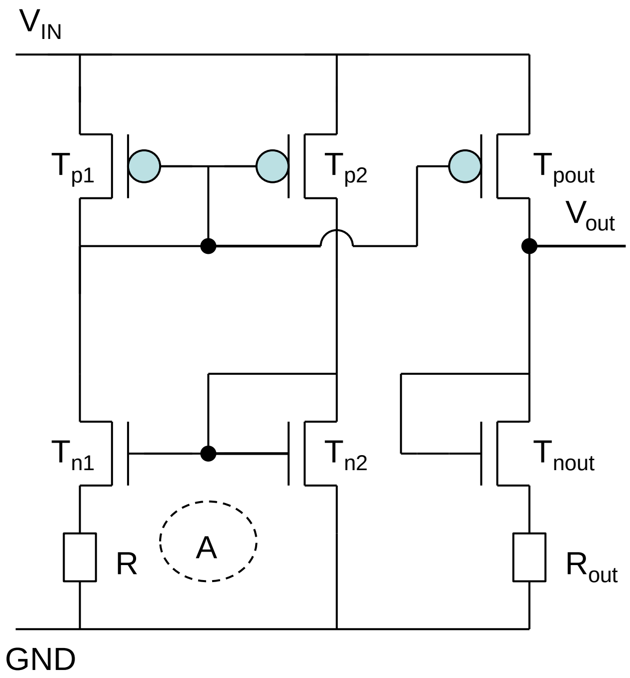


Figure 40: Reference Voltage Generator

Transistor T_{n1} has W/L ratio N times greater than T_{n2}.

The output voltage is formed at the T_{nout} and R_{out}.

The current mirror (transistors T_{p1}, T_{p2} and T_{pout}) ensures that the currents through T_{n1}, T_{n2} and T_{nout} are equal:

$$I_{n1} = I_{n2} = I_{nout} = I \qquad (90)$$

We refer to the supply voltage as V_{IN}.

Let us calculate the current I.

We use the Kirchhoff's law for the contour A. The following applies:

$$RI + V_{gs,n1} = V_{gs,n2} \qquad (91)$$

Let us assume that all transistors are in saturation and in weak inversion. The transistor current is then:

$$I_{ds,sat} = \frac{W}{L}\mu C'_{ox}U_T^2(n-1)e^{(V_{gs}-V_{th})/nU_T} = \frac{W}{L}I_0 e^{(V_{gs}-V_{th})/nU_T} \quad (92)$$

with

$$I_0 \equiv \mu C'_{ox}U_T^2(n-1) \sim 100nA$$

μ is the mobility of the charge carriers, n is slope factor, U_T the thermal voltage: $U_T = kT/e$, C'_{ox} is the oxide capacitance per area ($\varepsilon_0\, \varepsilon_{sio2}/t_{ox}$).

From (R3) we get for T_{n1}, T_{n2} and T_{nout}:

$$V_{gs,n1} = V_{th} + nU_T\ln\left(\frac{I}{I_0 W_{n1}/L_{n1}}\right)$$

$$V_{gs,n2} = V_{th} + nU_T\ln\left(\frac{I}{I_0 W_{n2}/L_{n2}}\right)$$

$$V_{gs,n2} = V_{th} + nU_T\ln\left(\frac{I}{I_0 W_{nout}/L_{nout}}\right) \quad (93)$$

Note that for weak inversion $I_{ds,sat} = I < I_0\, W/L$. The logarithms in (93) are negative.

If we substitute (93) in (94), we get:

$$RI + V_{th} + nU_T\ln\left(\frac{I}{I_0 W_{n1}/L_{n1}}\right) = V_{th} + nU_T\ln\left(\frac{I}{I_0 W_{n2}/L_{n2}}\right)$$

It follows:

$$RI = nU_T\ln\left(\frac{W_{n1}/L_{n1}}{W_{n2}/L_{n2}}\right)$$

Since the transistor T_{n1} has W/L by factor N larger:

$$I = \frac{nU_T}{R}\ln(N) = \frac{nkT}{e}\ln(N) \quad (95)$$

The current I is independent of supply voltage V_{IN}. As a first approximation, the current increases linearly with temperature. We neglect the temperature dependence of the slope factor n.

Now let us calculate the output voltage. The following applies (we use the result (94)):

$$V_{out} = R_{out}I + V_{gs,nout} = nU_T\frac{R_{out}}{R}\ln(N) + V_{th} + nU_T\ln\left(\frac{I}{I_0 W_{nout}/L_{nout}}\right) \quad (96)$$

The temperature dependence of V_{out} is complicated. However, it is relatively easy to see that the first term:

$$nU_T\frac{R_{out}}{R}\ln(N) = \frac{nkT}{e}\frac{R_{out}}{R}\ln(N) \quad (97)$$

increases linearly with the rise of T.

Let us look at the third term:

$$nU_T \ln\left(\frac{I}{I_0 W_{nout}/L_{nout}}\right) \qquad (98)$$

The logarithm is negative and $U_T = kT/e$ increases with temperature. Therefore, the third term causes V_{out} to become smaller as the temperature rises.

How does the threshold voltage depend on temperature?

We will use the following approximate formula for V_{th}:

$$V_{th} = \frac{2C_{dep,ac}}{C_{ox}} \times V_{cont} \sim \frac{1}{2} V_{cont} \qquad (99)$$

N_a is the density of acceptor atoms in the channel region, V_{cont} is the contact voltage between n and p silicon (for equal n and p doping strengths):

$$V_{cont} = 2U_T \ln\left(\frac{N_a}{n_i}\right) \qquad (100)$$

N_i is the intrinsic density of charge carriers:

$$n_i = \sqrt{N_c N_v} e^{\frac{-E_g}{2eU_T}} \qquad (101)$$

N_c und N_v are the effective densities of quantum states in conduction band and valence band:

$$N_c = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2} \sim 2.4 \times 10^{19}\ \mathrm{cm}^{-3}$$

$$N_v = 2\left(\frac{2\pi m_h^* kT}{h^2}\right)^{3/2} \sim 1.5 \times 10^{19}\ \mathrm{cm}^{-3}$$

E_g is the energy of the bandgap.

We will assume that $\frac{2C_{dep,ac}}{C_{ox}} \sim 0.5$ and is independent of temperature.

The threshold voltage

$$V_{th} = \frac{2C_{dep,ac}}{C_{ox}} \times V_{cont} \sim \frac{1}{2} V_{cont} \qquad (102)$$

becomes smaller with temperature increase, because V_{cont} (99) becomes smaller.

Let us try to roughly calculate the temperature dependence of contact voltage:

We use:

$$V_{cont} = 2U_T \ln(\frac{N_a}{n_i}) \quad (103)$$

and

$$n_i = \sqrt{N_c N_v e^{\frac{-E_g}{2eU_T}}} \quad (104)$$

It follows:

$$V_{cont} = \frac{2kT}{e}\left[\ln\left(N_a/\sqrt{N_c N_v}\right) + \frac{E_g}{2eU_T}\right] = 2U_T \ln\left(\frac{N_a}{\sqrt{N_c N_v}}\right) + \frac{E_g}{e}$$

$\ln\left(N_a/\sqrt{N_c N_v}\right)$ ist negative! Why?

The contact voltage is smaller than the bandgap expressed in volts and the density of ionized acceptors is smaller than the density of quantum states in valence and conduction band.

It follows that the threshold voltage decreases with temperature increase:

$$V_{th} = \sim \frac{1}{2} V_{cont} = \frac{1}{2}\frac{2kT}{e} \ln\left(\frac{N_a}{\sqrt{N_c N_v}}\right) + \frac{E_g}{2e}$$

Let us insert this result into (95)

$$V_{out} = \frac{E_g}{2e} + nU_T \frac{R_{out}}{R} \ln(N) + 2U_T \ln\left(\frac{N_a}{\sqrt{N_c N_v}}\right) + nU_T \ln\left(\frac{I}{I_0 W_{nout}/L_{nout}}\right)$$

We rewrite it as follows:

$$V_{out} = \frac{E_g}{2e} + nU_T \frac{R_{out}}{R} \ln(N) - 2U_T \ln\left(\frac{\sqrt{N_c N_v}}{N_a}\right) - nU_T \ln\left(\frac{\frac{I_0 W_{nout}}{L_{nout}}}{I}\right)$$

Both logarithms are now positive. It is therefore possible to set the parameters of the circuit (R_{out}, R, N, W_{out}/L_{out}) in such a way that the temperature increase of the first term is compensated by the second and third terms. Correct dimensioning can be determined in simulations. Often it is also necessary to adjust the circuit again after production. After that, a second design iteration is made and tested.

To find the initial values, the derivative of V_{out} over T can be calculated.

$$\frac{dV_{out}}{dT} = \frac{nk}{e}\frac{R_{out}}{R} \ln(N) - \frac{2k}{e} \ln\left(\frac{\sqrt{N_c N_v}}{N_a}\right) - \frac{nk}{e} \ln\left(\frac{\frac{I_0 W_{nout}}{L_{nout}}}{I}\right) \quad (105)$$

If the derivative is 0, the function $V_{out}(T)$ has a saddle point and a weak temperature dependence.

This is fulfilled under the following conditions (we neglect $\frac{2k}{e} \ln\left(\frac{\sqrt{N_c N_v}}{N_a}\right)$):

$$R_{out} = R$$

and

$$\frac{I_0 W_{nout}/L_{nout}}{I} \sim N \Rightarrow I \sim \frac{1}{N}\frac{W_{nout}}{L_{nout}} I_0$$

The output voltage in this case is approximately:

$$V_{out} \sim \frac{E_g}{2e} \sim 0.5V$$

The output voltage is about 1/2 voltage of the band gap. This is the reason why this type of reference voltage generator is called band-gap reference. It is interesting that the output voltage of one circuit reflects one quantum property of the semiconductor, the band gap energy.