Lecture 11

The topic of this lecture is **clocked analog circuits**.
The lecture is structured as follows:

- Track-and-hold circuit based on a switch and a capacitor
- Clocked amplifier
- Comparator

Introduction

In modern circuits, signal processing is mostly performed digitally. The input and output quantities are usually analog. When converting analog signals into digital signals, both time and amplitude are discretized.

The sample-and-hold circuit samples the signal at discrete moments in time (Figure 1).

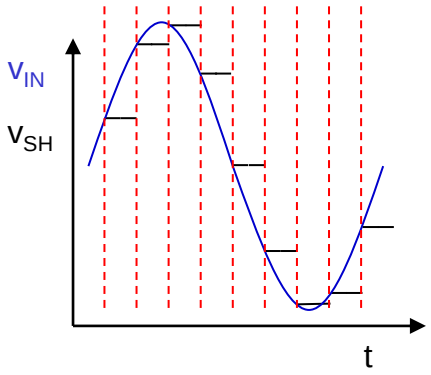


Figure 1: *Sample-and-Hold Circuit, Input and Output Signals*

In this lecture, we will use the following notation for voltages:

- Voltage at node **out**: $v_{OUT}(t)$
- DC level: V_{out}
- Small-signal component: $v_{out}(t) = v_{OUT}(t) - V_{out}$

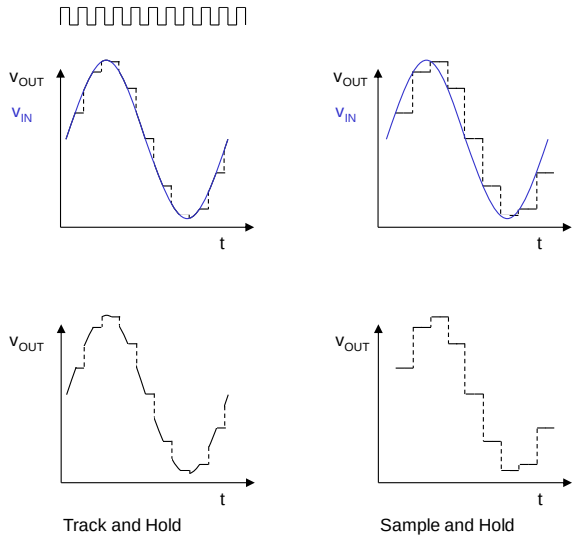


Figure 2: Difference between a track-and-hold circuit (left) and a sample-and-hold circuit (right).

Figure 2 shows the difference between the operation of a **track-and-hold** circuit (left) and a **sample-and-hold** circuit (right).
In this lecture, we will present the simplest track-and-hold circuit, which is based on a switch

and a capacitor. We will also describe a clocked amplifier that can operate as a sample-and-hold circuit.

Track-and-Hold Circuit

Figure 3 shows the simplest track-and-hold circuit. The circuit consists of a MOS transistor (MOS switch) T_{sw} and a sampling capacitor C. The gate of the transistor is connected to the signal **track**.

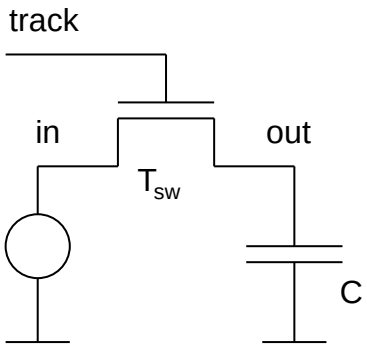


Figure 3: track and hold circuit

The signal **track** is a CMOS digital signal. In logic state 1, the potential of **track** is equal to VDD (positive supply voltage, e.g. 1.2 V). In logic state 0, V_{track} = 0 V (GND, ground potential).

Note that the signal **track** can be considered both as a digital signal and as an analog signal. For example, one can write **track = 1** (track is logic 1). Alternatively, one can write **track = VDD** when treating **track** as an analog signal.

One could denote the signal **track** in the digital domain as track,d and in the analog domain as track,a, and imagine a DA component that converts track,d into track,a.

The following table defines the conversion from the digital value to the analog voltage:

track,d	track,a
0	GND 0 V
1	VDD 1.2 V

Mixed-signal simulators (mixed-mode simulators) use such components. **Figure 4 (top)** shows the test bench for the track-and-hold circuit in a mixed-signal simulator.

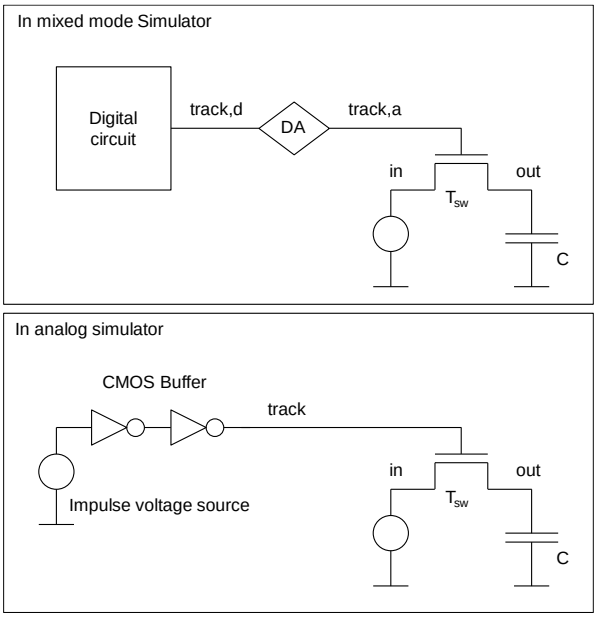


Figure 4: Testbench for the track-and-hold circuit in a mixed-signal simulator (top) and in an analog simulator (bottom).

When using an analog simulator, the circuit would be simulated using **transient simulation**. The signal **track** can be generated using a pulse source. To make the simulation more realistic, a CMOS buffer (two inverters connected in series) can be connected to the voltage source in order to obtain a more realistic rise time.

Figure 4 (bottom) shows the test bench for the track-and-hold circuit in an analog simulator.

Operation of the Track-and-Hold Circuit

Figure 5 illustrates the operation. When the signal **track** is logically 1, the NMOS transistor T_{sw} conducts and the output voltage v_{OUT} follows the input voltage v_{IN}. When **track** is logically 0, the transistor is off and v_{OUT} remains at the value of v_{IN} at the moment the **track** signal changes ($t=t_0$).

Note that a capacitor stores a voltage as long as no current flows into or out of it.

Therefore the track-and-hold circuit samples the value of v_{IN} at time t_0.

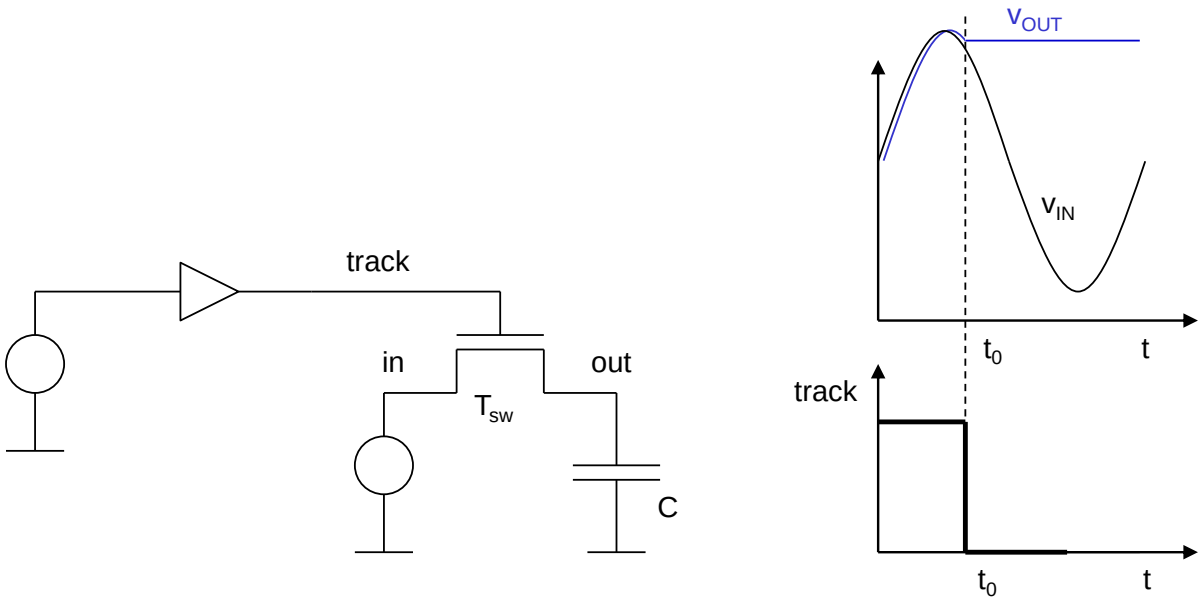


Figure 5: Operation of the track-and-hold circuit.

More Detailed Analysis of the Track-and-Hold Circuit

The circuit deviates from ideal behavior due to several effects.

Small-Signal On-Resistance

The small-signal on-resistance of the MOS switch is determined by the following expression:

$$\frac{1}{r_{on}} = \left(\frac{dI_{ds}}{dV_{ds}}\right)_{V_{ds}=0} \qquad (1)$$

In the analysis, we will take the **substrate effect** into account, since the voltage between the source and the substrate is not zero.

The expression for the transistor drain current is:

$$I_{ds} = \frac{W}{L}\mu C'_{ox}\left(\left(V_{gs} - V_{thsb}\right)V_{ds} - n\frac{V_{ds}^2}{2}\right) \quad (2)$$

From (1) and (2), it follows that:

$$r_{on} = \frac{1}{\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})} \quad (3)$$

During the **track phase**, Vg=V_{track}=VDD. Therefore, the gate-to-source voltage is:

$$V_{gs} = VDD - V_{in} \quad (4)$$

The threshold voltage including the substrate effect is:

$$V_{thsb} = V_{th} + (n-1)V_{sb} = V_{th} + (n-1)V_{in} \quad (5)$$

The factor n=1.25n=1.25 is the slope factor.

Substituting (4) and (5) into (3), we obtain:

$$r_{on} = \frac{1}{\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})} = \frac{1}{\mu C'_{ox}\frac{W}{L}(VDD - V_{in} - V_{th} - (n-1)V_{in})} = \frac{1}{\mu C'_{ox}\frac{W}{L}(VDD - nV_{in} - V_{th})} \quad (6)$$

The following table lists the parameter values of the MOS transistors:

μ (NMOS)	Mobility	2.64×10^{-2} m^2/Vs @ 300 K
μ (PMOS)	Mobility	1.45×10^{-2} m^2/Vs @ 300 K
I_0 (NMOS)	Subthreshold current	59 nA
I_0 (PMOS)	Subthreshold current	33 nA
C'_{ox} (NMOS und PMOS)	Oxide-capacitance	13.28 fF/μm or 0.01328F/m^2
U_T = kT/e	Thermal voltage	26mV @ 300K
n (NMOS und PMOS)	Slope factor	1.25 @ 300 K
V_{th} (NMOS und PMOS)	Threshold voltage	0.5V @ 300 K

Example

Let us calculate the resistance for:

$$V_{gs} - V_{thsb} = VDD - nV_{in} - V_{th} = 100\text{mV}$$

This yields:

$$r_{on} = \frac{28\text{k}\Omega}{W/L}$$

From equation (6), we see that the resistance increases for larger values of the input voltage V_{in}.

For

$$V_{gs} - V_{thsb} = VDD - nV_{in} - V_{th} = 0 \Rightarrow V_{in} = \frac{VDD - V_{th}}{n} = \frac{1.2V - 0.5V}{1.25} = 0.56 \qquad (7)$$

the resistance becomes infinite according to equation (6).

This result is not correct, because for voltages

$$V_{gs} - V_{thsb} < 3U_T \Rightarrow V_{in} > \frac{VDD - V_{th} - 3U_T}{n} = 0.5\ V \qquad (8)$$

the transistor operates in **weak inversion**.

Let us now calculate the resistance when the transistor operates in **weak inversion**. This derivation may be skipped.

The expression for the NMOS transistor drain current in weak inversion is:

$$I_{ds} = \frac{W}{L} I_0 e^{\frac{V_{gs} - V_{thsb}}{nU_T}} \left(1 - e^{\frac{-V_{ds}}{U_T}}\right) \qquad (9)$$

with

$$I_0 \equiv \mu C'_{ox} U_T^2 (n-1) \sim 59\ nA$$

Substituting (9) into (1), we obtain the expression for the on-resistance in weak inversion:

$$\frac{1}{r_{on,weak}} = \frac{W}{L} \frac{I_0}{U_T} e^{\frac{V_{gs} - V_{thsb}}{nU_T}}$$

or

$$r_{on,weak} = \frac{L}{W} \frac{U_T}{I_0} e^{-\frac{V_{gs} - V_{thsb}}{nU_T}} = \frac{L}{W} \frac{U_T}{I_0} e^{\frac{nV_{in} + Vth - VDD}{nU_T}} \sim \frac{L}{W} 440\ k\Omega \times e^{\frac{nV_{in} + Vth - VDD}{nU_T}} \qquad (10)$$

For W=L, the resistance reaches 1 GΩ when

$$V_{thsb} - V_{gs} = nV_{in} + Vth - VDD > nU_T \ln\left(\frac{1G}{440k}\right) \sim 250mV$$

or

$$V_{in} > \frac{(VDD - V_{th} + 250mV)}{n} = \frac{(1.2 - 500mV + 250mV)}{n} = 0.76\ V \qquad (11)$$

For higher values of V_{in}, one can assume that the transistor is always off.

Figure 6 shows the different operating regions of the NMOS sampling transistor.

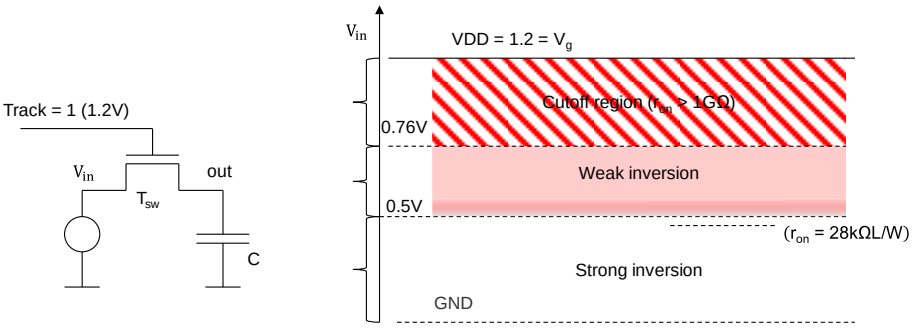


Figure 6: Different operating regions of the sampling transistor (NMOS).

The following table summarizes the results.

Operation region	Condition	Condition	r_{on}
Cut-off	$V_{thsb} - V_{gs} > 250\text{mV}$	$V_{in} > 0.76\ \text{V}$	$> \frac{1\text{G}\Omega}{W/L}$
Weak inversion	$V_{gs} - V_{thsb} < 3U_T$	$V_{in} > 0.5\ \text{V}$	$\frac{L}{W} 440\ \text{k}\Omega \times e^{\frac{nV_{in}+Vth-VDD}{nU_T}}$
Strong inversion	$V_{gs} - V_{thsb} > 3U_T$	$V_{in} < 0.5\ \text{V}$	$\frac{1}{\mu C'_{ox} \frac{W}{L} (VDD - nV_{in} - V_{th})}$

Bandwidth

The resistance of the switch causes a **low-pass behavior** of the circuit:

$$V_{out}(s) = \frac{1}{sr_{on}C+1} V_{in}(s) \qquad (12)$$

The bandwidth is:

$$f_0 = \frac{1}{2\pi \times r_{on}C} \qquad (13)$$

Example

Switch dimensions T_{sw}:
W=1 µm, L=65 nm

C = 100 fF

$$V_{gs} - V_{thsb} = VDD - nV_{in} - V_{th} = 100mV$$

$$r_{on} = \frac{28k\Omega}{W/L} = 1.82\ k\Omega$$

Bandwidth:

$$f_0 = \frac{1}{2\pi \times r_{on}C} = 874MHz$$

Since the resistance r_{on} increases with increasing V_{in}, the circuit also becomes slower. **Figure 7** illustrates this effect. For $V_{in} > 0.76$, the transistor is off and V_{out} can no longer follow V_{in}.

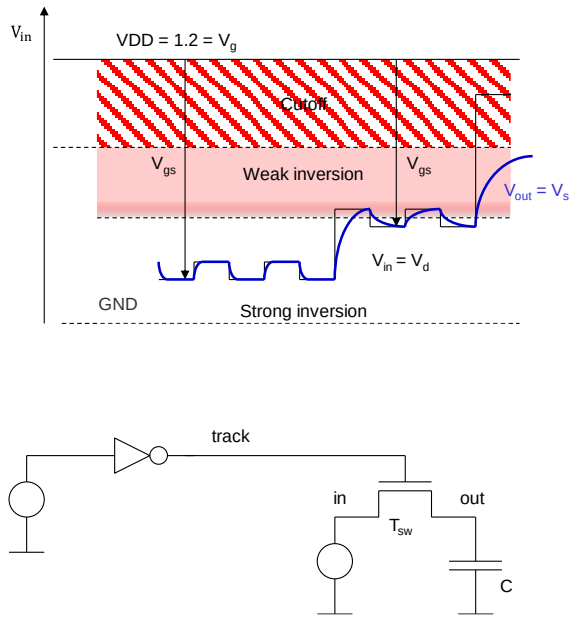


Figure 7: Track-and-hold circuit behaves like a low-pass filter.

Sampling Error

When the transistor is in **strong inversion**, the transistor channel contains the following charge:

$$|Q_{ch}| = WLC'_{ox}(V_{gs} - V_{thsb}) = WLC'_{ox}(VDD - nV_{in} - V_{th}) \quad (14)$$

The charge is **negative** in the case of an NMOS transistor.

When the transistor switch is turned off, this charge must be released. The charge distributes approximately **half to the input source** and **half to the capacitor C** (Figure 8). This charge causes a voltage change V_{serr} across the capacitor C:

$$|V_{serr}| = \frac{1}{2}\frac{|Q_{ch}|}{C} = \frac{1}{2}\frac{WLC'_{ox}(VDD - nV_{in} - V_{th})}{C} \quad (15)$$

This voltage change distorts the signal. It represents a **sampling error due to charge injection**.

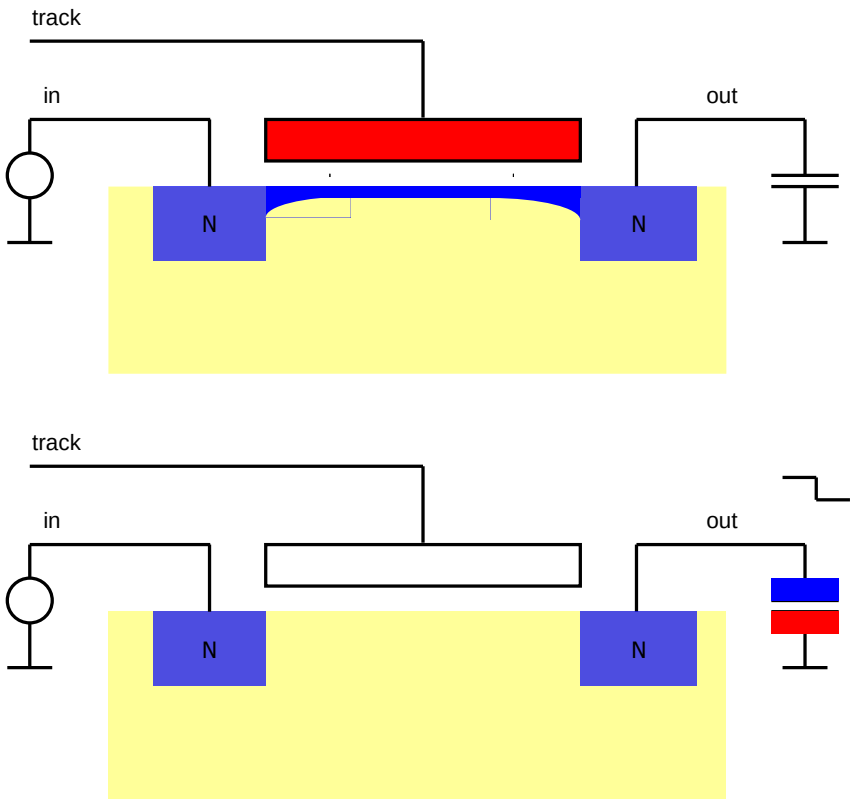


Figure 8: Charge injection and sampling error.

Note that the **sampling error** depends on the signal level (Figure 9). This error leads to a **nonlinear characteristic**.

In addition to the error in (15), the **gate-drain overlap capacitance** C_{ovl} introduces a constant sampling error:

$$\left|V_{serr,overlap}\right| = \frac{C_{ovl}}{C} VDD \quad (16)$$

When the transistor conducts in **weak inversion**, the error contribution from the overlap capacitance dominates.

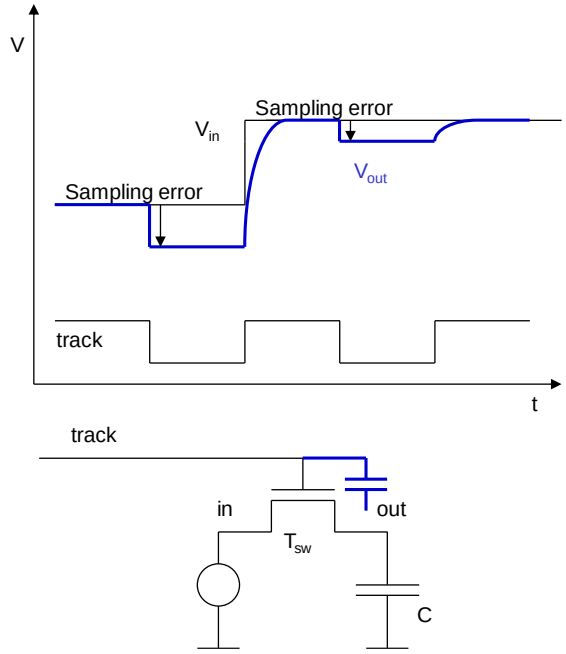


Figure 9: Sampling error depends on V_{in}.

Dimensioning

Normally, **sampling transistors** are designed with the **minimum gate length** in order to **reduce gate capacitance and sampling error** and to **maximize bandwidth**. The **gate width** is chosen to ensure sufficient bandwidth according to (13).

Example:
For the switch dimensions

W = 1 µm, L = 65 nm, and a sampling capacitor C = 100 fF the **maximum sampling error** is:

$$|V_{serr}| = \frac{1}{2}\frac{WLC'_{ox}(VDD - 0 - V_{th})}{C} = 3\ \text{mV}$$

Dummy Switch

The **sampling error** due to charge injection can be reduced by adding a **dummy switch** (Figure 10). Figure 10 shows the sampling circuit with the dummy switch T_d. The dummy switch presents a capacitance C_d. The gate of T_d is connected to the **inverted trackB signal**.

When the switch T_{sw} is turned off, **trackB** rises from 0 to VDD. This generates the following **gate charge** in the dummy switch:

$$|Q_{ch,d}| = W_d L_d C'_{ox}(VDD - nV_{in} - V_{th})$$

This charge is subtracted from the charge on the main capacitor C. Therefore, the **sampling error** becomes:

$$|V_{serr}| = \frac{1}{2}\frac{WLC'_{ox}(VDD - V_{in} - V_{th})}{C} - \frac{W_d L_d C'_{ox}(VDD - V_{in} - V_{th})}{C}$$

If the dummy switch has approximately **half the area** of the main switch ($W_d L_d = 1/2$ WL), the sampling error due to charge injection is **almost zero**. Figure 11 illustrates this effect.

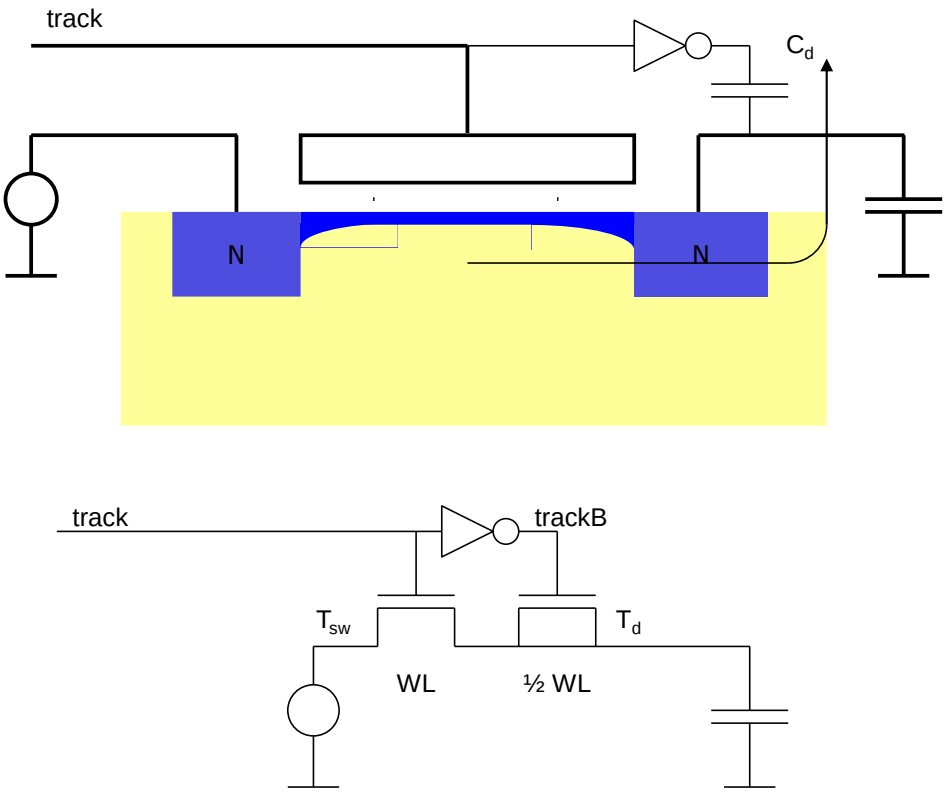


Figure 10: Dummy switch

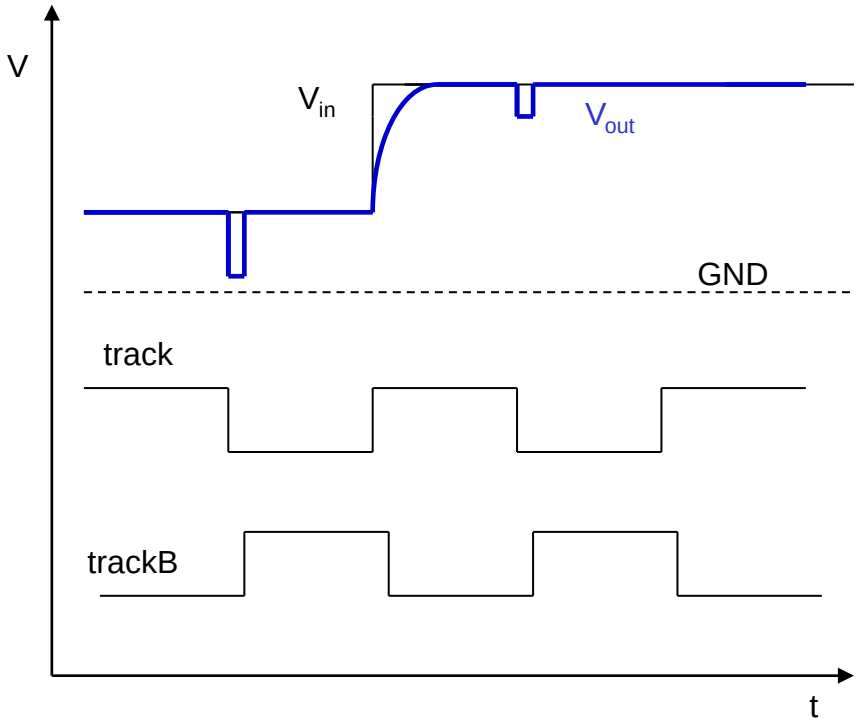


Figure 11: Dummy switch can compensate for charge injection

PMOS Switch

We have shown in (6) that **NMOS switches conduct worse for higher V_{in} voltages**.
A **PMOS** switch, on the other hand, conducts better for **lower V_{in}.** The gate of the PMOS switch must be connected to the **inverted signal trackB**. It is also said that the signal **trackB is active low**. During the **track phase**, trackB = 0.

This derivation can be skipped.

The **on-resistance** of the PMOS switch is:

$$r_{on,pmos} = \frac{1}{\mu_p C'_{ox}\frac{W}{L}(|V_{gs}|-|V_{thsb}|)} = \frac{1}{\mu_p C'_{ox}\frac{W}{L}(|V_{gs}|-|V_{th}|-(n-1)|V_{sb}|)} = \frac{1}{\mu C'_{ox}\frac{W}{L}(V_{in}-|V_{th}|-(n-1)(VDD-V_{in}))} = \frac{1}{\mu C'_{ox}\frac{W}{L}(nV_{in}-|V_{th}|-(n-1)VDD)}$$

A PMOS switch is in **strong inversion** for:

$$|V_{gs}| - |V_{thsb}| = nV_{in} - |V_{th}| - (n-1)VDD > 3U_T \Rightarrow V_{in} > \frac{|V_{th}|+(n-1)VDD+3U_T}{n} = 0.7V$$

Recall the result for the NMOS switch. An NMOS switch is in strong inversion for:

$$V_{in} < \frac{VDD-V_{th}-3U_T}{n} = 0.50V = VDD - 0.7V$$

The following table summarizes the **operating regions of a PMOS switch**:

Operation range	Condition	Condition	r_{on}
Cut-off	$V_{thsb} - V_{gs} > 250mV$	$V_{in} < 0.64\ V$	$> \frac{1.8\ G\Omega}{W/L}$
Weak inversion	$\lvert V_{gs}\rvert - \lvert V_{thsb}\rvert < 3U_T$	$V_{in} < 0.7\ V$	$\frac{L}{W} 790\ k\Omega \times e^{\frac{-nV_{in}+\lvert V_{th}\rvert+(n-1)VDD}{nU_T}}$
Strong inversion	$\lvert V_{gs}\rvert - \lvert V_{thsb}\rvert > 3U_T$	$V_{in} > 0.7\ V$	$\frac{1}{\mu_p C'_{ox} \frac{W}{L}(nV_{in} - \lvert V_{th}\rvert - (n-1)VDD)}$

Figure 12 shows operating regions of an NMOS switch (left) and a PMOS switch (right).

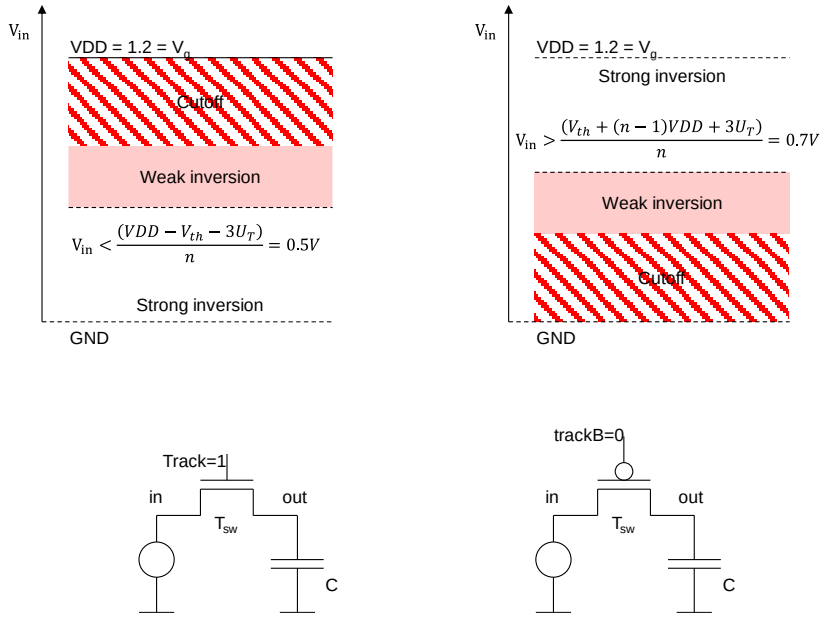


Figure 12: Operating regions of an NMOS switch (left) and a PMOS switch (right).

Transmission Gate

It is common to implement the switch using a **PMOS and NMOS transistor in parallel**. In this case, the overall circuit conducts relatively well for most values of V_{in}. Only in the region around $V_{in} \sim 1/2VDD$ are **both transistors in weak inversion** (Figure 12). The exponent in the current equation is small, and r_{on}<1 MΩ.

The signals **track** and **trackB** are complementary. This combined switch is called a **transmission gate (TG)**.

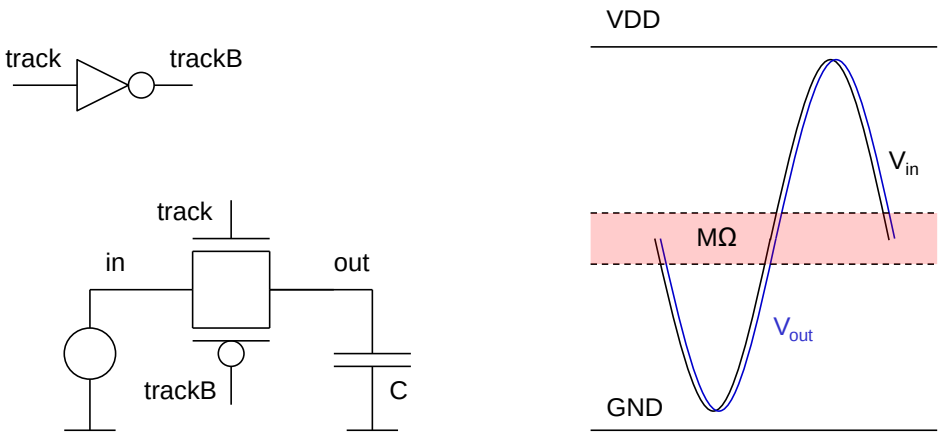


Figure 13: Transmission gate

The **resistance R_{on}** is given by the following formula:

$$R_{on} = \frac{r_{on,nmos} r_{on,pmos}}{r_{on,nmos} + r_{on,pmos}} = \frac{k_p k_n (VDD - nV_{in} - V_{th})(nV_{in} - |V_{th}| - (n-1)VDD)}{k_p (VDD - V_{in} - V_{th}) + k_n (nV_{in} - |V_{th}| - (n-1)VDD)} \quad (17$$

with

$$k_n \equiv \mu_n C'_{ox} \frac{W_n}{L_n}$$

$$k_p \equiv \mu_p C'_{ox} \frac{W_p}{L_p}$$

For equal gate widths, the PMOS switch in our example has an **on-resistance approximately μ_n/μ_p = 1.8 ×smaller**.

From (17), we can see that a **transmission gate** also has an **unequal resistance**, which becomes particularly high for $V_{in} \sim 1/2VDD$.

The circuit described in the following paragraph has a **resistance that is independent of V_{in}.**

Bootstrapped Switch

If the **gate potential in the ON state** is:

$$V_{g,on} = V_{in} + V_{on}$$

then r_{on} is approximately **independent of V_{in}**. V_{on} is a constant voltage, usually V_{on} = VDD. The on-resistance is:

$$r_{on} = \frac{1}{\mu C'_{ox}\frac{W}{L}(V_{gs}-V_{thsb})} = \frac{1}{\mu C'_{ox}\frac{W}{L}(V_g - V_{th} - nV_{in})} = \frac{1}{\mu C'_{ox}\frac{W}{L}(V_{on} - V_{th} - (n-1)V_{in})} \quad (18)$$

Equation (18) shows that even this switch is not **perfect**, since the **threshold voltage depends on V_{in}** due to the substrate effect.

Ideally, one would have:

$$V_{g,on} - V_{th} - nV_{in} = \text{const} \Rightarrow V_{g,on} = nV_{in} + V_{on}$$

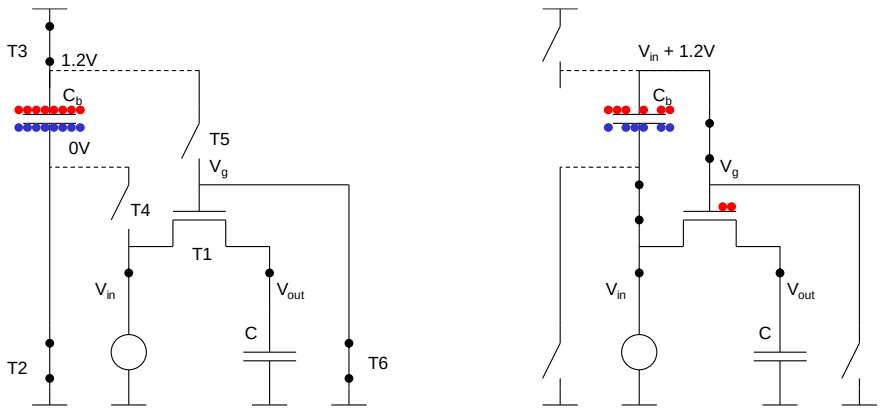
However, this is difficult to realize. Having $V_{g,on} = V_{in} + V_{on}$ is usually **good enough for most applications**.

In this chapter, we will present a circuit that generates:

$$V_{g,on} = V_{in} + VDD$$

Note that $V_{g,on}$ can be **higher than VDD**. If a circuit, powered by VDD, produces a potential higher than VDD, this is called **"bootstrapping"**.

The name suggests the idea that the task seems impossible—like someone trying to lift themselves up by pulling on their own boots.



Hold:
The capacitor C_b is first charged between VDD and GND.

Track:
Capacitor is connected to V_{in}

Figure 14: Bootstrapped switch – concept.

Figure 14 shows the concept for realizing a **bootstrapped switch**. Bootstrapping is done with a **capacitor C_b**.

The capacitor C_b is **charged between VDD and GND** during the **hold phase** (Figure 14, left).

In the **track phase**, the **negative terminal** of C_b is connected to V_{in} (Figure 14, right).
The **positive terminal** of C_b then has the potential:

V_{in} + VDD (V_{in} + 1.2 V)

and can be used to generate $V_{g,on}$.

The capacitor C_b acts like a **battery** that provides the voltage VDD.

Note that C_b must be able to **charge the gate capacitance** from $V_{g,off}$ = 0 V to $V_{g,on}$ = V_{in} + VDD. This requires a charge of:

$Q = (V_{in} + VDD)\, C_{gate}$

which must be supplied by C_b. Therefore, C_b must be **much larger than C_{gate}**; otherwise, C_b will discharge and the voltage V_{in} + VDD cannot be reached.

When V_{in} changes in **track mode**, $V_{g,on}$ **automatically adapts** (Figure 15).

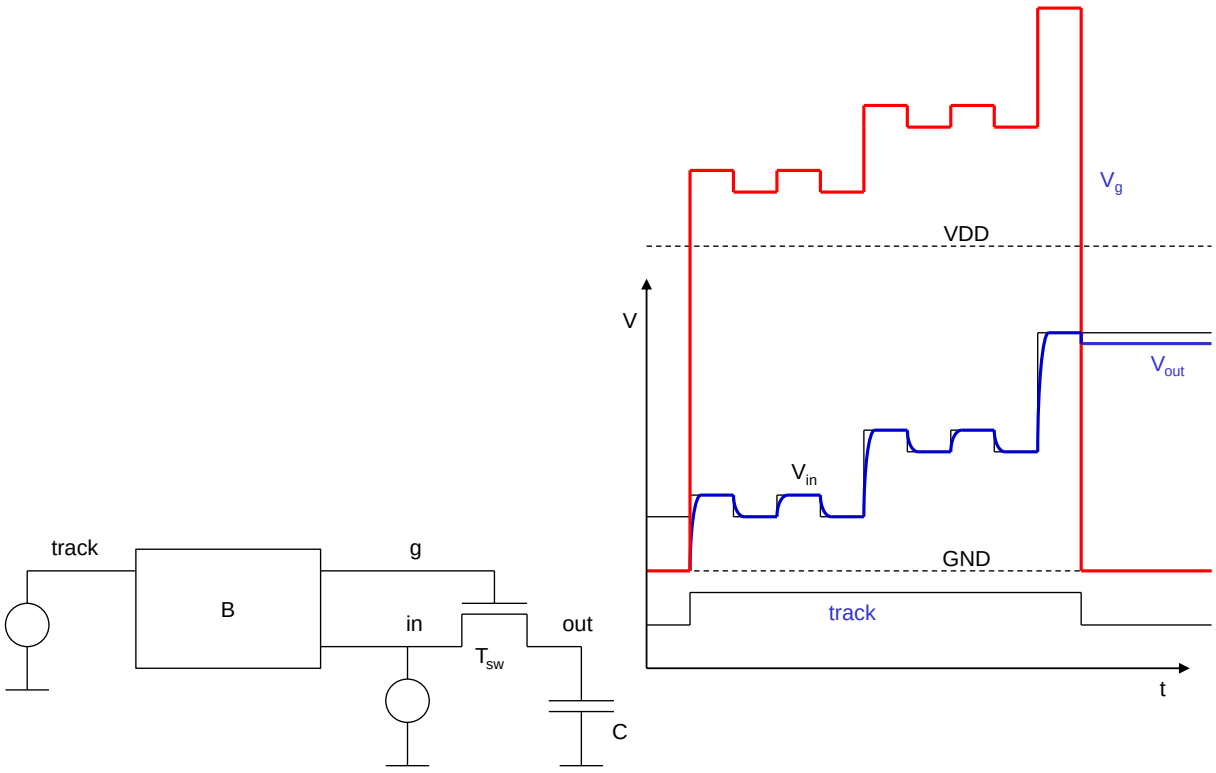


Figure 15: Bootstrapped switch – signal waveforms

In the case of a **bootstrapped switch**, the **sampling error** is relatively **constant**.

Here too, the **substrate effect** has an influence. The sampling error is:

$$|V_{serr}| = \frac{1}{2}\frac{|Q_{ch}|}{C} = \frac{1}{2}\frac{WLC'_{ox}(V_{on}-(n-1)V_{in})}{C}$$

Implementation (Optional)

Designing a **bootstrapped switch** is challenging. Here we show one possible implementation.

Let's start with the circuit in **Figure 16**.

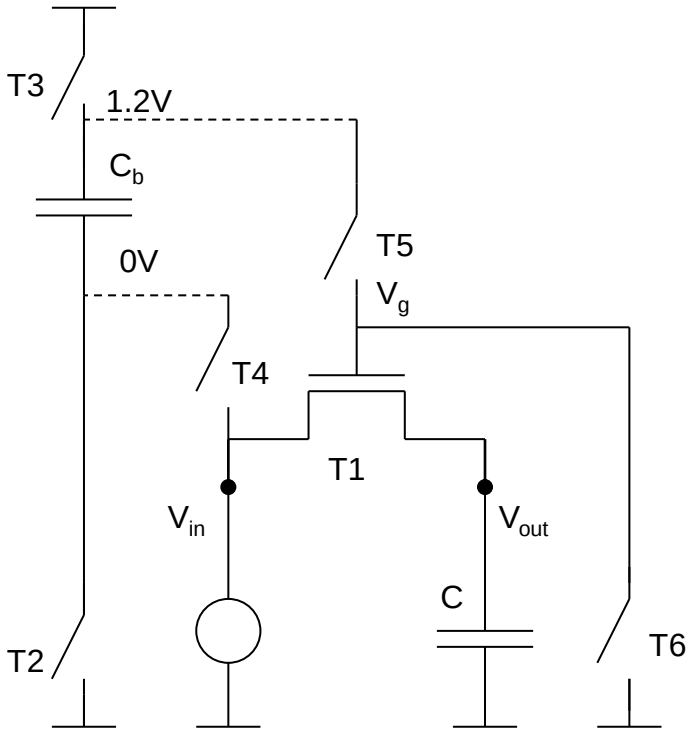
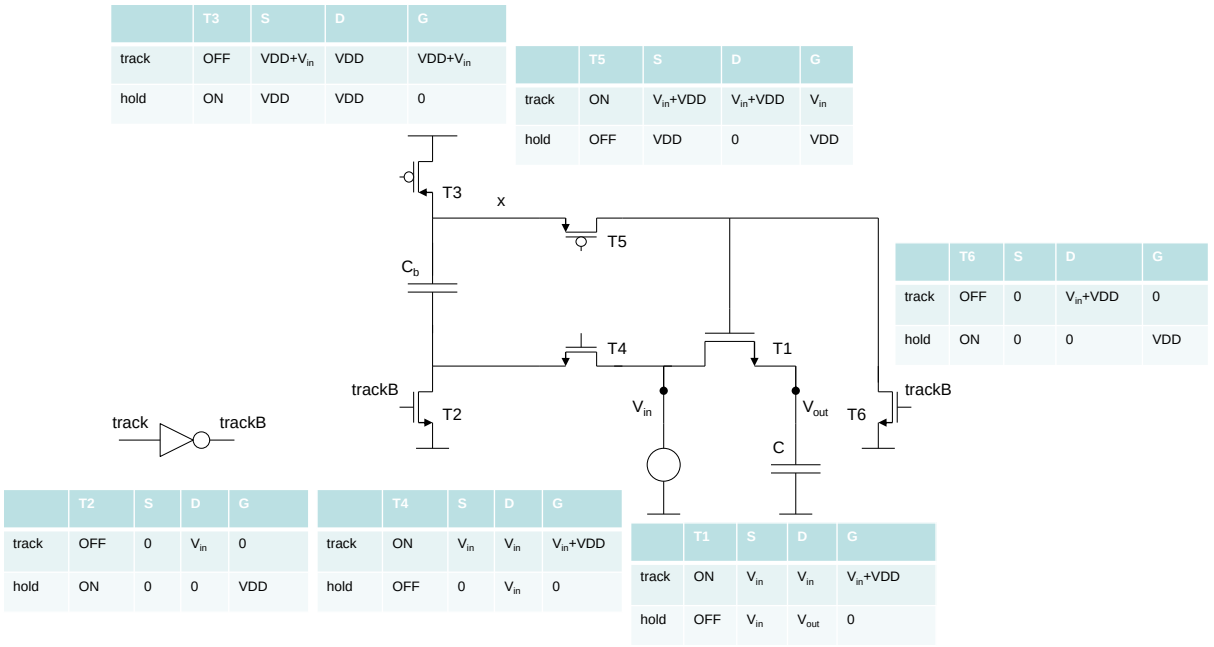


Figure 16: Bootstrapped switch – schematic diagram.

We implement switches T3 and T5 with **PMOS transistors**, since these switches have high potentials at their source and drain. The other switches are **NMOS transistors**.

Next, we determine the **gate potentials** in the track and hold states for each transistor.



	T3	S	D	G
track	OFF	VDD+V_{in}	VDD	VDD+V_{in}
hold	ON	VDD	VDD	0

	T5	S	D	G
track	ON	V_{in}+VDD	V_{in}+VDD	V_{in}
hold	OFF	VDD	0	VDD

	T6	S	D	G
track	OFF	0	V_{in}+VDD	0
hold	ON	0	0	VDD

	T2	S	D	G
track	OFF	0	V_{in}	0
hold	ON	0	0	VDD

	T4	S	D	G
track	ON	V_{in}	V_{in}	V_{in}+VDD
hold	OFF	0	V_{in}	0

	T1	S	D	G
track	ON	V_{in}	V_{in}	V_{in}+VDD
hold	OFF	V_{in}	V_{out}	0

Figure 17: Bootstrapped switch – implementation. Arrows in transistor symbols indicate the source.

Figure 17 shows a table for all transistors, listing the **source, drain, and gate potentials** in track and hold phases, as well as the **transistor state (ON/OFF)**.

We now supplement the circuit with the structures that generate the gate voltages:

- **Transistors T2 and T6** have V_G=0 in the track state and V_G=VDD in the hold state. We can therefore directly connect the **trackB signal** to the gates of T2 and T6.
- **Transistors T1, T3, and T4** have the **same gate potential in both phases**. We can therefore **tie the gates of T1, T3, and T4 together** (Figure 18). The capacitor C_b generates the gate potential for T1, and thus also for T3 and T4.
- Only the **gate of T5** remains. Its potential is V_{in} in the track phase and VDD in the hold phase.

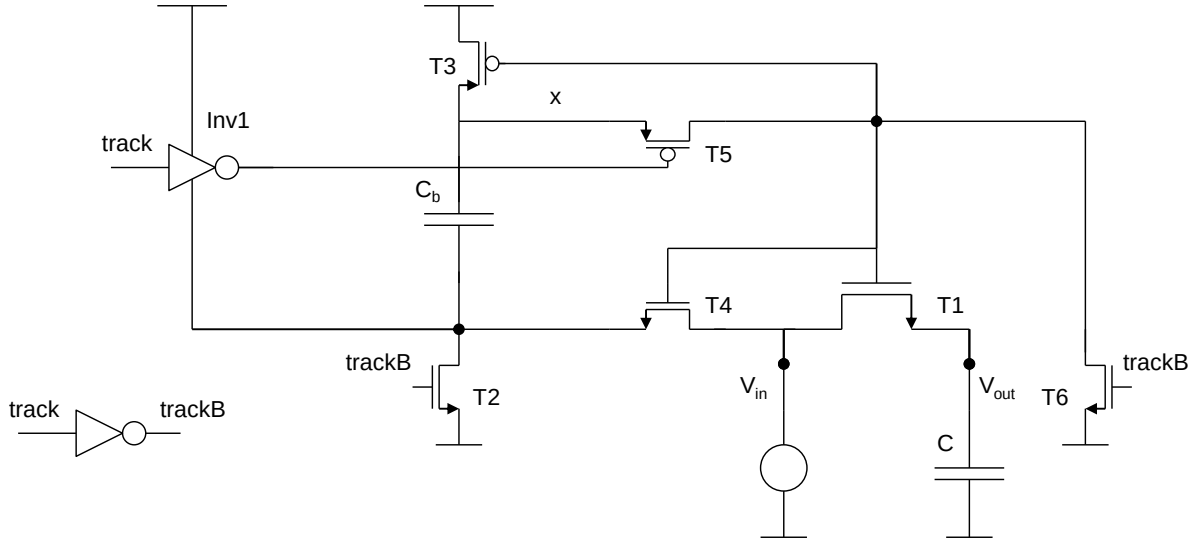


Figure 18: Bootstrapped switch – implementation.

This potential can be generated using an **inverter-like circuit Inv1** (Figure 18). The ground of this inverter is connected to the **source of T4**, since this potential is also V_{in} in the track state.

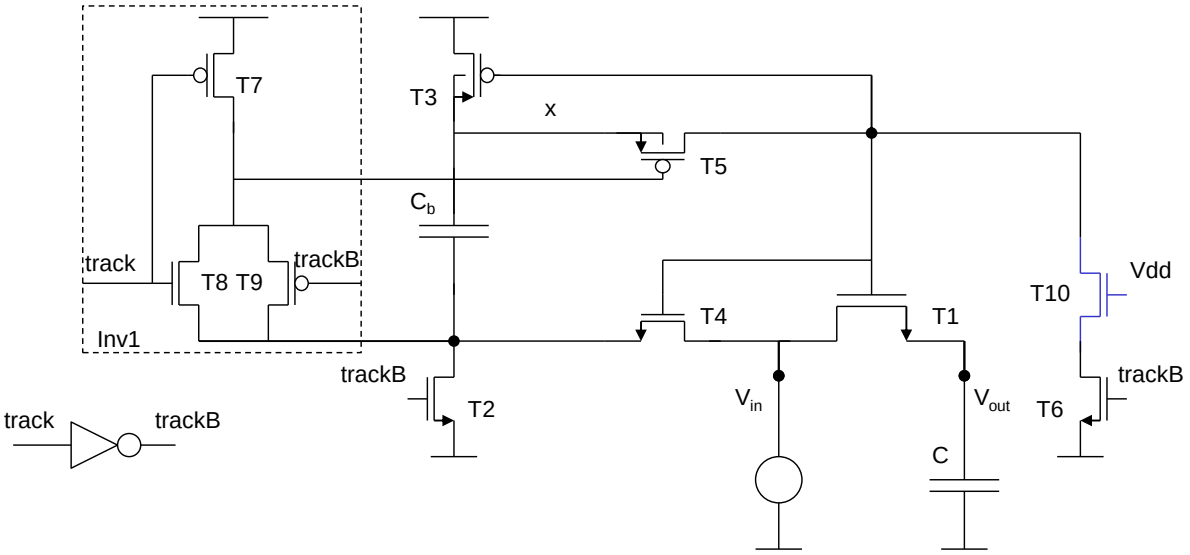


Figure 19: Bootstrapped switch – complete circuit. If the substrate contact is missing in the symbol, the substrate is connected either to GND (NMOS) or VDD (PMOS).

Figure 19 shows the **complete circuit**, including the **implementation of the Inv1 circuit**.

Next, we determine the **potentials of the N- and P-wells**.

- Particularly critical are the **PMOS transistors** T3 and T5, which have **source and drain potentials higher than VDD** in the track state (VDD+V_{in}). The **N-well potential (substrate)** for these transistors must also be V_{in}+VDD in the track phase; otherwise, the **source/drain–substrate diodes** would conduct.
- In the hold phase, the wells of T3 and T5 should be at VDD. One solution is to connect the **N-wells of both transistors** to node x, since V_x provides the required potential (Figure 19).
- The wells of the other PMOS transistors are connected to VDD, and the wells of all NMOS transistors are connected to GND.

For circuits that **generate potentials higher than VDD**, there is a risk that some transistors experience **overvoltage**, i.e., a voltage between gate, source, and drain that exceeds VDD. Such overvoltage could **damage the transistors**.

From the tables, we see that **T6** has a voltage of V_{in}+VDD between drain and source in the track state. This problem can be solved by inserting **T10** (Figure 19). Transistor T10 **protects T6** by preventing the drain potential of T6 from rising above approximately VDD $-V_{th}$.

Switched Voltage Amplifier

In previous lectures, we introduced an **inverting amplifier** with feedback based on a **capacitor C_f** and a **resistor R_f**. In Lecture 7, we derived the **transfer function** and **impulse response** of this amplifier. We saw that the amplifier exhibits **high-pass behavior**.

Here, we will introduce a **switched (clocked) inverting amplifier**.[1] The advantage of this amplifier compared to the inverting voltage amplifier from previous lectures is that it can also **amplify slow or DC signals**.

The switched amplifier can also operate as a **sample-and-hold circuit**.

An amplifier **without a clock signal** but with feedback based on R or C is called a **continuous-feedback amplifier**.

Operation

Figure 20 shows the **schematic of the clocked amplifier** (bottom) and the **waveforms of important signals** (top).

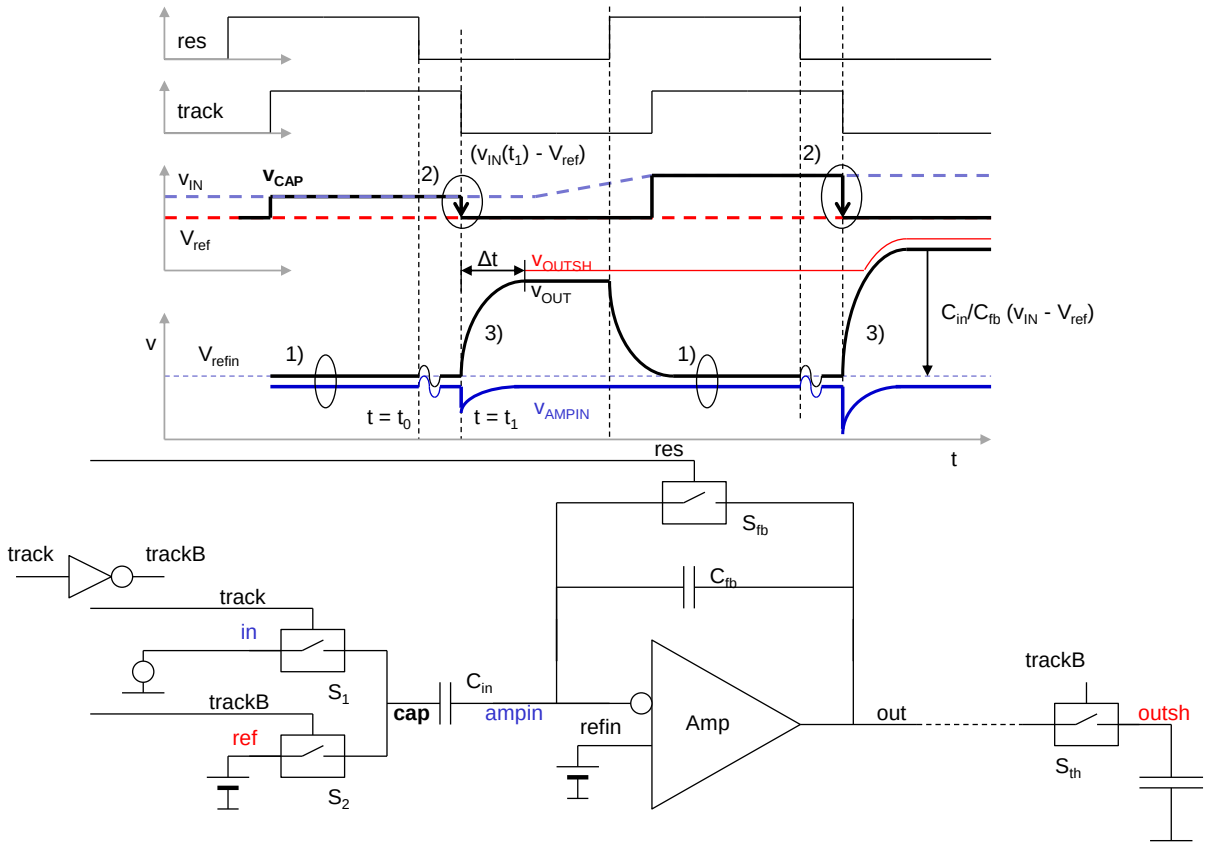


Figure 20: Schematic of the clocked voltage amplifier (bottom) and waveforms of important signals (top).

[1] In literature, a clocked amplifier is called a **switched-capacitor amplifier**.

The **reset signal** (res) is a digital signal. The amplifier is either in the **reset state** (res = 1) or in the **signal amplification state** (res = 0).

The components S_1, S_2, and S_{fb} are **switches**, implemented using **PMOS transistors, NMOS transistors, or transmission gates**.

The amplifier **Amp** (the active component) can be implemented either as:

- An **operational amplifier**, or
- A **single-ended amplifier with negative gain** (e.g., single-ended amplifier with folded cascode).

In the case of an **operational amplifier implementation**, the **positive input** of Amp is connected to a **constant reference voltage V_{refin}.**

1) Reset Phase

The role of S_{fb} is to **establish feedback** between the nodes **out** and **ampin**, in the same way that the resistor R_{fb} does in the continuous amplifier. This ensures that the amplifier is brought to the **correct operating point**.

The operating point is:

$$V_{ampin,dc} = V_{out,dc} = V_{refin}$$

We use the subscript **"dc"** to clarify that these are **DC voltages**, i.e., the operating points.

In the reset phase, the **instantaneous potentials** at nodes **out** and **ampin** are equal to the corresponding DC values:

$$v_{AMPIN} = V_{ampin,dc}$$

$$v_{OUT} = V_{out,dc}$$

2) Generation of the Voltage Step

The role of S_1 and S_2 is to **generate a voltage step** at the node **cap**. S_1 and S_2 form an **analog multiplexer**.

When the **track signal** goes from **logical 1 to 0** (t=t1), the potential v_{CAP} changes from $v_{IN}(t1)$ to V_{ref}.

3) Amplification

The amplifier **amplifies the voltage change** at node **cap**. The output potential changes from its DC value

$$V_{out,dc} = V_{refin}$$

to the value:

$$v_{OUT}(t_1 + \Delta t) = V_{out,dc} + \frac{C_{in}}{C_{fb}}(v_{IN}(t_1) - V_{ref}) = V_{refin} + \frac{C_{in}}{C_{fb}}(v_{IN}(t_1) - V_{ref}) \quad (19)$$

This means that the **output signals have an amplitude** of:

$$\frac{C_{in}}{C_{fb}}(v_{IN}(t_1 + NT) - V_{ref})$$

where T is the period of **res** and **track**, and N is an integer.

The **output potential** always jumps between the values:

Reset phase	V_{ref}
Amplification phase	$V_{refin} + \frac{C_{in}}{C_{fb}}(v_{IN}(t_1 + NT) - V_{ref})$

Thus, the output is **not continuously proportional to the input**, but repeatedly returns to the **reference level V_{refin}.**

This is **not a problem** if the clocked amplifier is connected to another clocked amplifier that can also amplify voltage changes.

It is also possible to connect a **track-and-hold circuit S_{th}** to the amplifier output. The node **outsh** then represents a **sample-and-hold output**.

Error Due to Charge Injection (Optional)

The **charge injection** of the switch S_{fb} affects the amplifier (Figure 21).

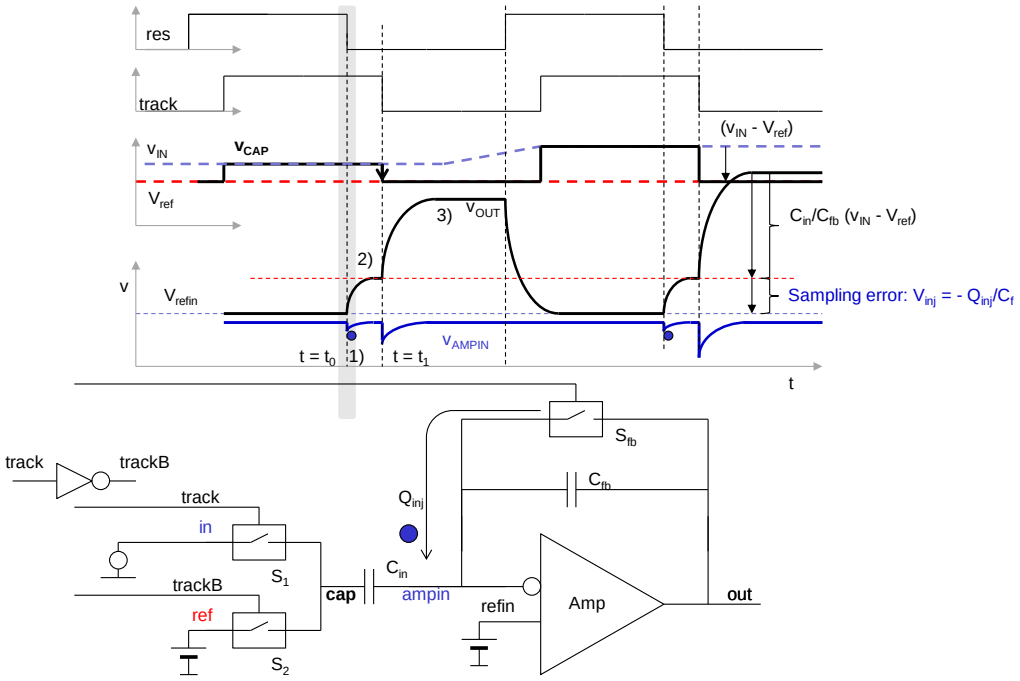


Figure 21: Schematic of the clocked voltage amplifier (bottom) and waveforms of important signals (top), including charge injection from switch S_{fb}.

1) **When S_{fb} opens**, the charge Q_{inj} flows onto the node **ampin**. In the case of an **NMOS switch S_{fb}**, Q_{inj} is **negative**, causing the potential v_{AMPIN} to **drop**.
2) The **feedback of the amplifier** tries to restore $v_{AMPIN} = V_{refin}$. This causes the **voltage at the node out** to increase by the **sampling error**:
   $V_{inj} = - Q_{inj}/C_f$
   After this adjustment, $v_{AMPIN}=V_{refin}$ again.
3) The signals at the output are therefore **shifted by $V_{inj} = -Q_{inj} / C_f$** higher than they would be without charge injection.

Note that the **left terminal of the switch S_{fb} (node ampin)** has a **constant, signal-independent potential**. Therefore, the **amount of injected charge is always the same**, independent of the signal level.

Conclusion: Charge injection introduces only a **constant offset**, which can be **reduced using a dummy switch**.

Fully differential Differential Amplifier (Optional)

It is also possible to implement the **clocked amplifier** as a **fully differential amplifier**.

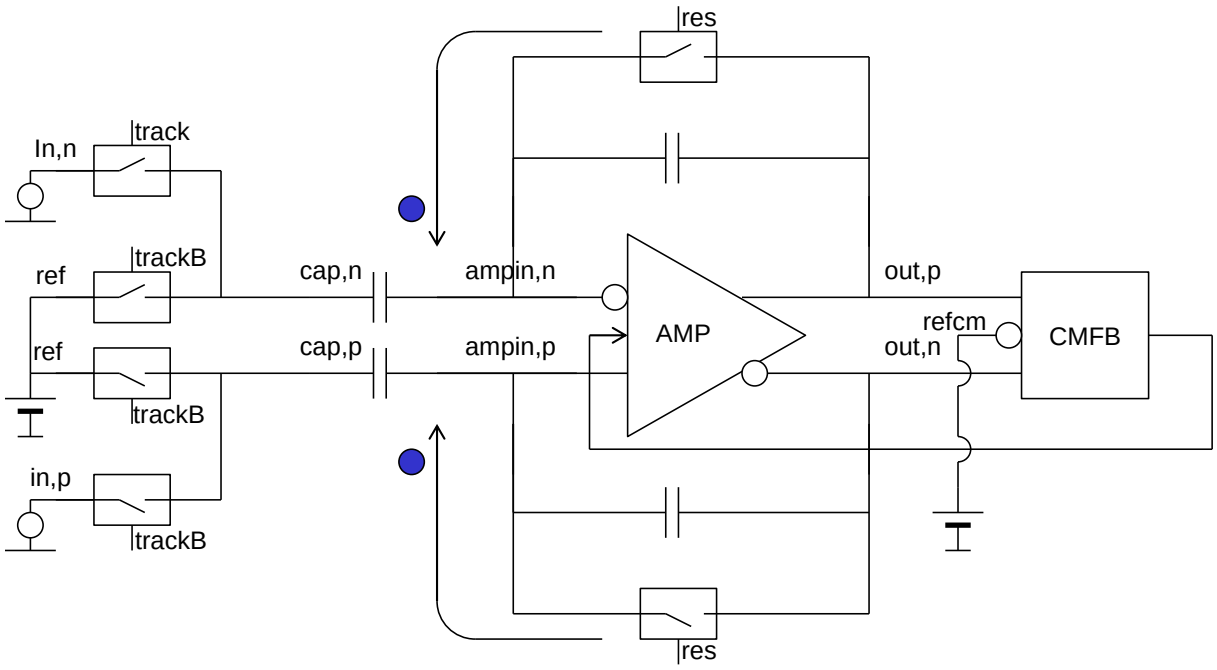


Figure 22: Switched fully differential amplifier.

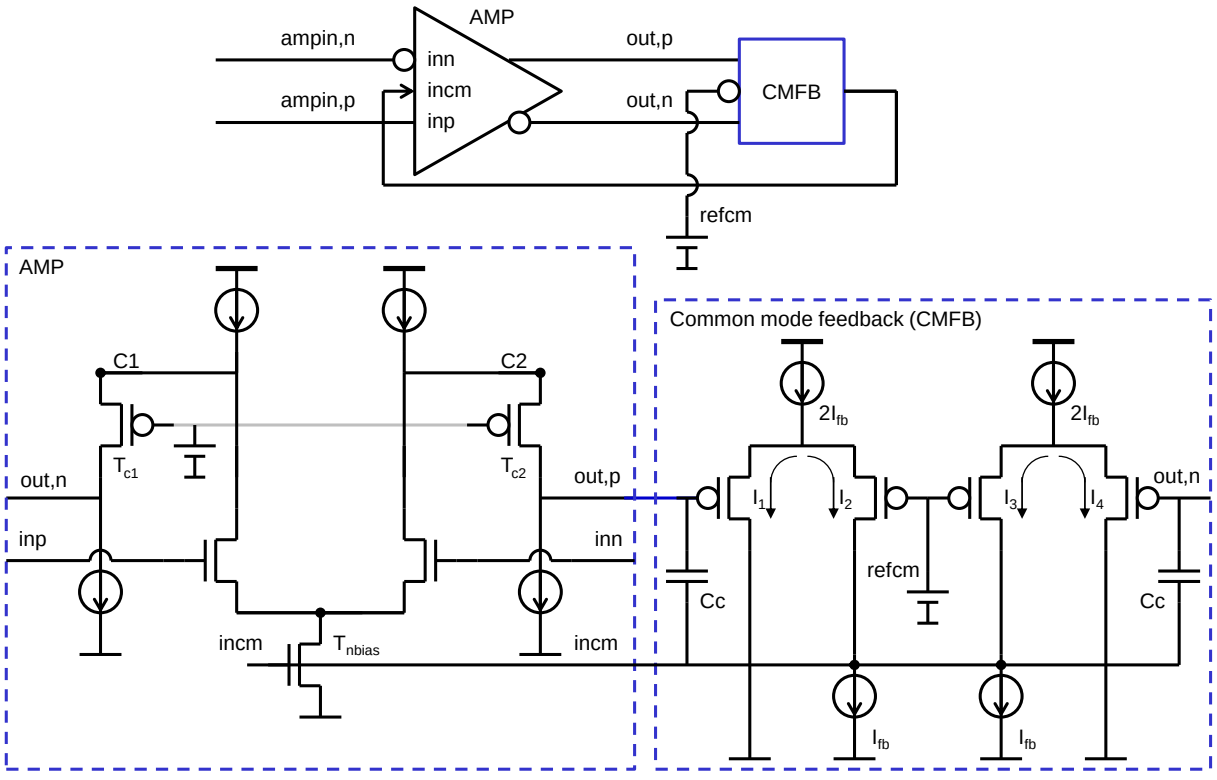


Figure 23: Transistor implementation of the differential amplifier AMPAMP and the common-mode feedback (CMFB).

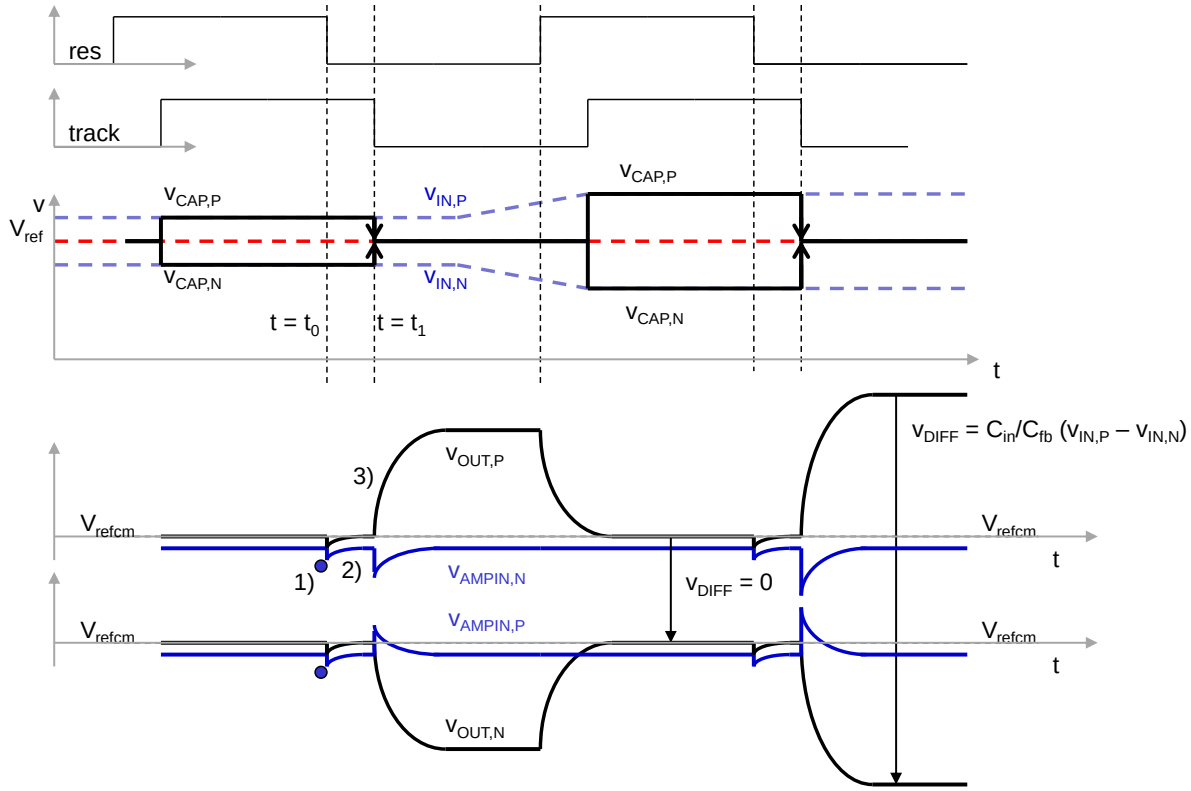


Figure 24: Waveforms of signals.

Figure 22 shows the **block diagram**. The active components, the amplifier **AMP** and the **common-mode feedback (CMFB)**, can be implemented as discussed in Lecture 9.

Figure 23 shows a slightly improved implementation of the CMFB. The CMFB ensures that the **average of the output potentials** equals V_{refcm}:

$$\frac{v_{out,p}+v_{out,n}}{2} = V_{refcm}$$

This is only the case when $I_2+I_3=I_{fb}$ (Figure 23), ensuring that the common-mode input potential V_{incm} neither rises nor falls.

The **capacitors C_c** ensure that for **small signals**:

$$\frac{v_{out,p}(t)+v_{out,n}(t)}{2} = 0$$

and that the **common-mode feedback remains stable**.

In the **reset phase** (Figure 24), all potentials are equal to V_{refcm}:

$$v_{AMPIN,N} = v_{AMPIN,P} = v_{OUT,P} = v_{OUT,N} = V_{refcm}$$

When **charge injection** occurs, both $v_{AMPIN,N}$ and $v_{AMPIN,P}$ **drop by the same amount** (Figure 24 – 1). Since this is a **common-mode signal**, it is **not amplified** by the amplifier AMP, thanks to its **high common-mode rejection ratio (CMRR)**.

The **common-mode feedback (CMFB)** quickly restores the original **DC values** (Figure 24 – 2).

The signals at **cap,n** and **cap,p** are in **opposite phase**. They are **amplified**, because the amplifier has a **high differential gain**, while the **average**

$$\frac{v_{OUT,P} + v_{OUT,N}}{2}$$

remains **constant** (Figure 24 – 3). The **differential output signal** is proportional to the **differential input signal**:

$$v_{OUT,P} - v_{OUT,N} = \frac{C_{in}}{C_{fb}}(v_{IN,P} - v_{IN,N})$$

The fully differential amplifier provides a very good signal-to-noise ratio.

Comparator

An **analog comparator** is a very important circuit. A comparator can be considered the **simplest analog-to-digital (A/D) converter**. Many real A/D converters use only **comparators, switches, and capacitors** as analog components.

A comparator can be implemented using an **operational amplifier without feedback**.

The output should be approximately at the **logical 1 level** when

$v_{IN}(t) > V_{th} + \Delta V$

and at the **logical 0 level** when

$v_{IN}(t) < V_{th} - \Delta V$

Here, ΔV is the **required voltage above or below the threshold** for the output to take a **definite logical level**.

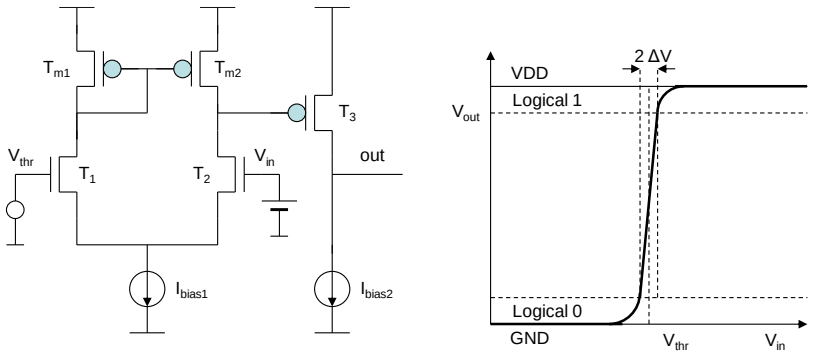


Figure 25: Comparator: left – schematic, right – DC transfer characteristic.

Implementation and DC Characteristic

Figure 25 shows a typical implementation of a comparator. By using **two amplification stages**, the **voltage gain** is very high. This ensures that ΔV is small and the output quickly reaches a **definite logical level**.

*The **right side of Figure 25** shows the **DC characteristic** of the comparator. Since the amplifier in Figure 25 operates **without feedback**, a **compensation capacitor for frequency stability** is not needed.*

When we implement a comparator using a **voltage amplifier**, we exploit the **nonlinearity of its transfer characteristic**. Most of the time, the circuit operates in regions where the output is **either GND or VDD**. The amplifier has an approximately **linear gain** only for small voltage range around V_{th}: $v_{IN}(t) \in (V_{th} - \Delta V, V_{th} + \Delta V)$.

Signal Delay

The **comparator's transfer characteristic** only allows us to determine the response of the circuit to **slow signals**. However, input signals are often **fast**, and an important property of a comparator is its **signal delay**.

The **signal delay** can be measured from the **response to voltage steps** at the input V_{in}, as shown in **Figure 26**. The delay is **smaller** when the voltage step has a **larger amplitude** (B).

Transistor T3 is **off** for $V_{in}<V_{th}$ (before the voltage step). Usually, the **turn-on time of T3** determines the delay. The **capacitance at node out1** must discharge from VDD to a value below $VDD-V_{th}$ (V_{th} is the threshold voltage of T3).

If the input signal is **just above the threshold**, and the difference $V_{in}-V_{thr}$ is small, the **output current of the first stage I_{out1}** is also small. It then takes a **relatively long time** to discharge the **parasitic capacitance at node out1**.

On the other hand, the current of **transistor T3** can become **relatively large**, so the capacitance at node **out** can be **charged relatively quickly**.

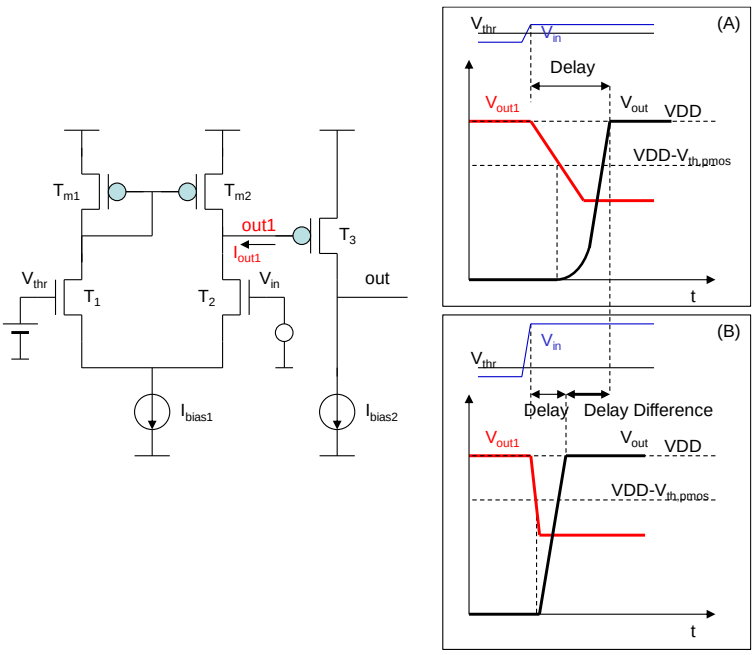


Figure 26: Comparator response to two voltage steps. Case A: input voltage step has small amplitude. Case B: input voltage step has large amplitude.

Input Range, PMOS and NMOS Implementation, Rail-to-Rail Input

We must always ensure that for $V_{in}\sim V_{th}$, the comparator has **sufficient gain** (to minimize ΔV) and that the **input transistors** and the **bias current source I_{bias1}** operate in **saturation**.

A comparator based on an **NMOS differential pair** (Figure 27, left) is suitable for **higher V_{th})**, while a comparator with a **PMOS differential pair** (Figure 27, right) is suitable for **lower V_{th})**.

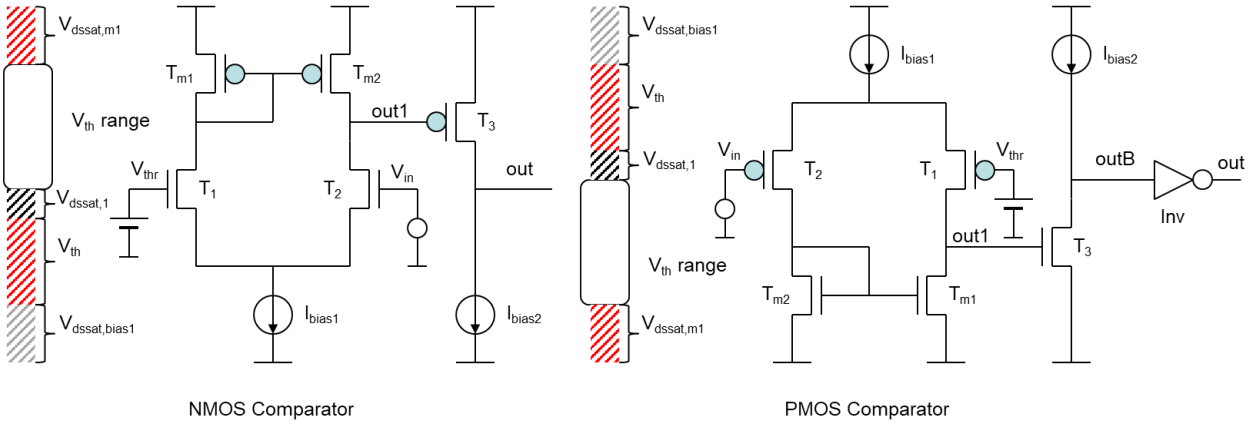


Figure 27: V_{th} must be within the correct voltage range so that the transistors operate in saturation when $V_{in} \sim V_{th}$.

Figure 27 shows the **allowed V_{th} voltage range**. When V_{th} is within this range, **transistors T_1 and I_{bias1}** operate in **saturation**.

Note that the **"PMOS comparator"** (Figure 27, right) produces a **logical 0** at the output outB when $V_{in} > V_{th}$. Therefore, a **CMOS inverter (Inv)** is used to **invert the signal**.

Also note that in both comparators, **T3 is off when $V_{in} < V_{th}$** . It is possible to swap V_{in} and V_{th} such that T3 is **on for $V_{in} < V_{th}$.** Both variants have **different signal delays** and **different output polarities**.

Transistor T3 can charge capacitances **faster** than the current source I_{bias2}, because the current of the current source is **limited to** I_{bias2}.

Normally, V_{th} is fixed, and we can choose either the **PMOS or NMOS comparator**.

If the comparator must operate over a **maximally wide V_{th} range**, a **rail-to-rail input comparator** is used, as shown in **Figure 28**.

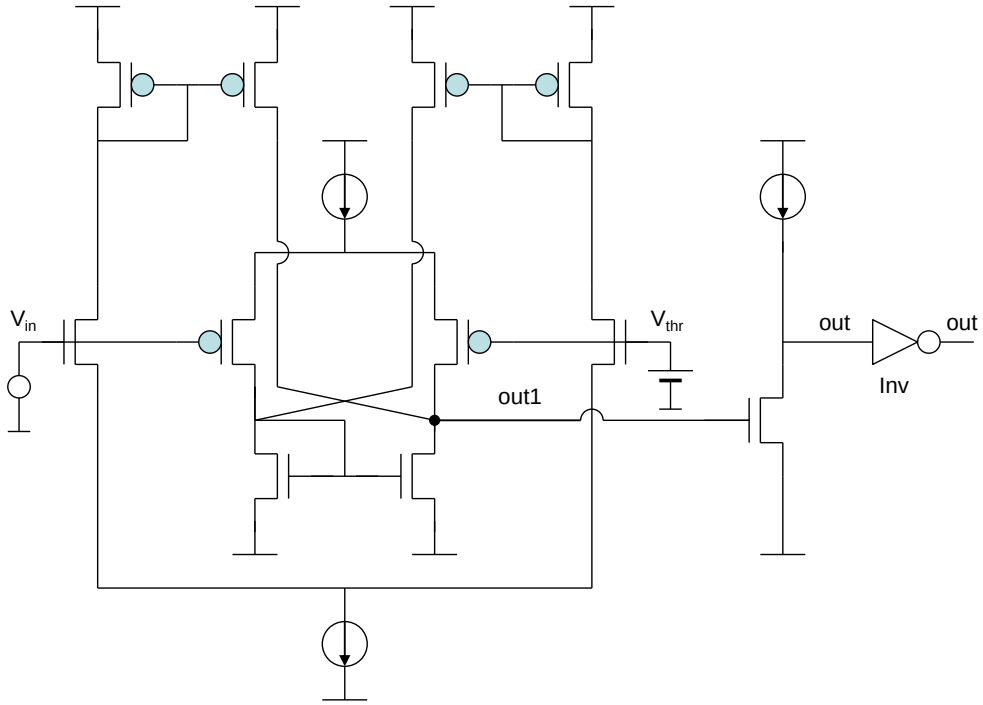


Figure 28: Comparator with rail-to-rail input.

The **rail-to-rail comparator** (Figure 28) has a **slightly longer signal delay** compared to the simple NMOS and PMOS comparators because the **capacitance at node out1 is larger**.

Offset

If the **input transistors T1 and T2** and the transistors in the **current mirror Tm1 and Tm2** have **unequal thresholds or transconductances**, an **offset** appears in the transfer characteristic (Figure 29).

Causes for unequal thresholds can be:

1. **Statistical variations**, e.g., variations in **oxide thickness, doping, or transistor dimensions W and L**.
2. **Asymmetry**, e.g., if one transistor has a different **orientation** than the other.

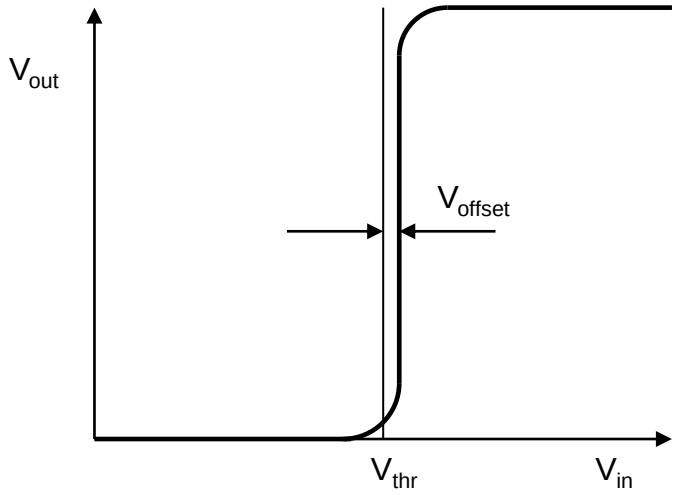


Figure 29: Offset

Different **drain voltages** of the input transistors can also contribute to the offset.

An **offset voltage V_{offset}** can be **modeled with a voltage source at the input** of the comparator, as shown in Figure 30 (bottom). This **shifts the effective threshold voltage**, which can cause an **incorrect output** from the comparator.

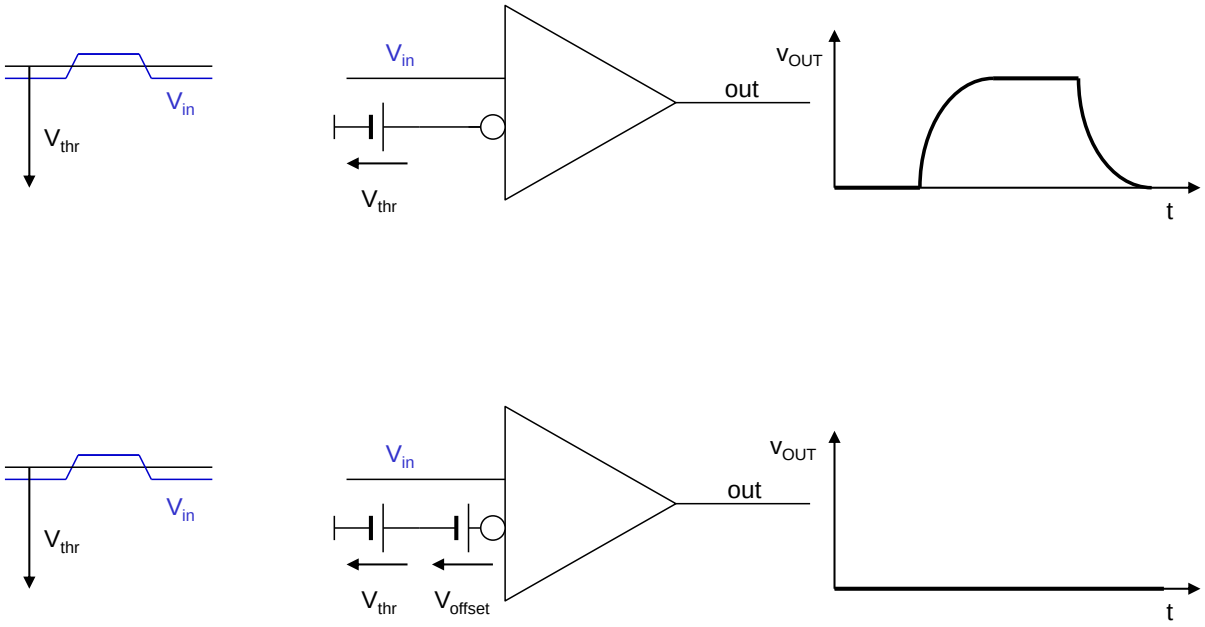


Figure 30: Top – ideal comparator. Bottom – comparator with offset.

Additional Topic (Optional)

Offset Compensation with a Clocked Comparator

This chapter is **not part of the exam**.

Comparators can also be implemented as **clocked amplifiers**.

Figure 31 shows the **clocked comparator in four clock phases**.

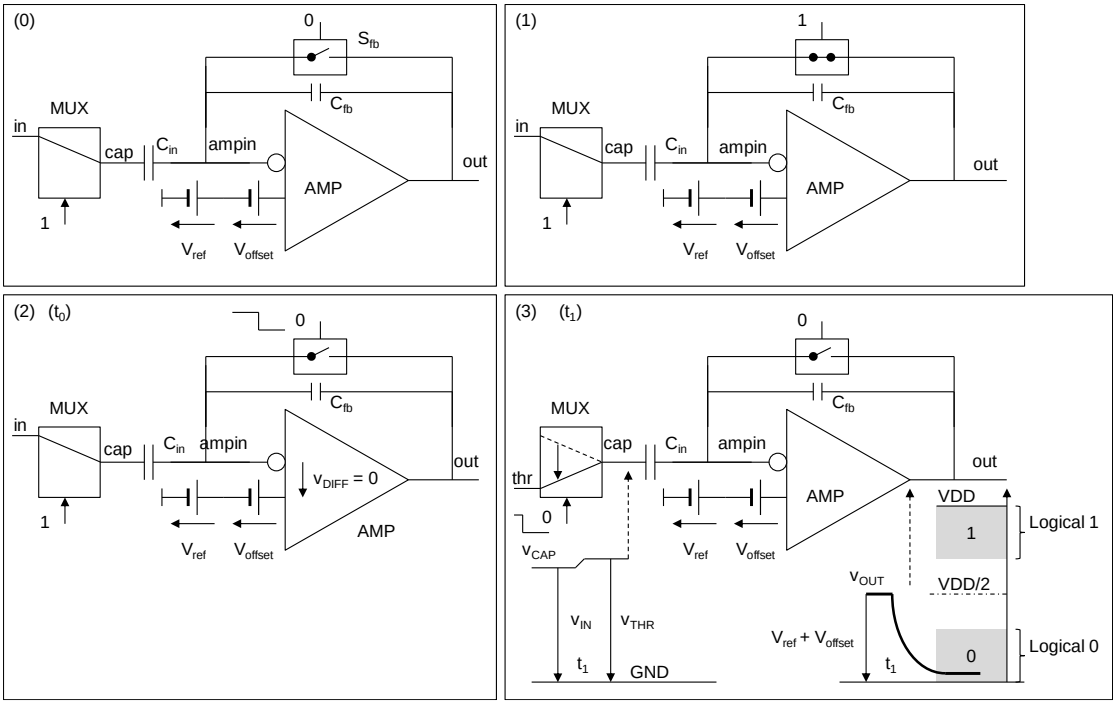


Figure 31: Clocked comparator with offset compensation.

The circuit has a **similar structure to the clocked voltage amplifier**, with the difference that C_{fb} is very small.

In the **reset state** (Figure 31 (1)), the switch S_{fb} is **closed**, and the feedback ensures:

$$v_{AMPIN} = v_{OUT} = V_{ampin,dc}$$

The **input voltage** can be determined from the **DC characteristic** of the comparator:

$$V_{ampin,dc} = V_{ref} + V_{offset}$$

After **opening S_{fb} (at $t=t_0$)** (Figure 31 (2)), the potentials v_{AMPIN} and v_{OUT} **remain unchanged**:

$$v_{OUT}(t_0) = V_{ref} + V_{offset} \qquad (20)$$

Note that the **voltage between the two inputs of the differential amplifier AMP is zero**, even though there is an offset. For this reason, this comparator is also called a **comparator with auto-zero capability**.

As in the case of the **voltage amplifier**, the **analog multiplexer (MUX)** generates a **voltage step** at the node **cap**. The potential v_{CAP} changes from $v_{IN}(t_1)$ to V_{thr} when, at $t=t_1$, **track** goes from 1 to 0 (Figure 31 (3)).

The **amplifier output** changes from:

$$v_{OUT}(t_0) = V_{ref} + V_{offset}$$

to

$$v_{OUT}(t_1 + \Delta t) = V_{out,dc} + \frac{C_{in}}{C_{fb}}(v_{IN}(t_1) - V_{thr})$$

In our example (Figure 31), we assume that $v_{IN}(t_1)$ is **slightly below the threshold V_{thr}**. In this case, the output voltage should be:

$$v_{OUT}(t_1 + \Delta t) = V_{ref} + V_{offset} + \frac{C_{in}}{C_{fb}}(v_{IN}(t_1) - V_{thr}) \qquad (21)$$

This will be interpreted as a **logical 0** by subsequent CMOS circuits (e.g., a CMOS inverter).

If the **gain $A = C_{in}/C_{fb}$** is large, the **offset voltage V_{offset}** has **little effect on the result**. The circuit amplifies the **signal difference** $(v_{IN}(t1) - V_{thr})$ by the factor A, while the offset V_{offset} is **not amplified**.

Influence of Charge Injection

The **charge injection** from the switch S_{fb} can affect the result. **Figure 34** illustrates this.

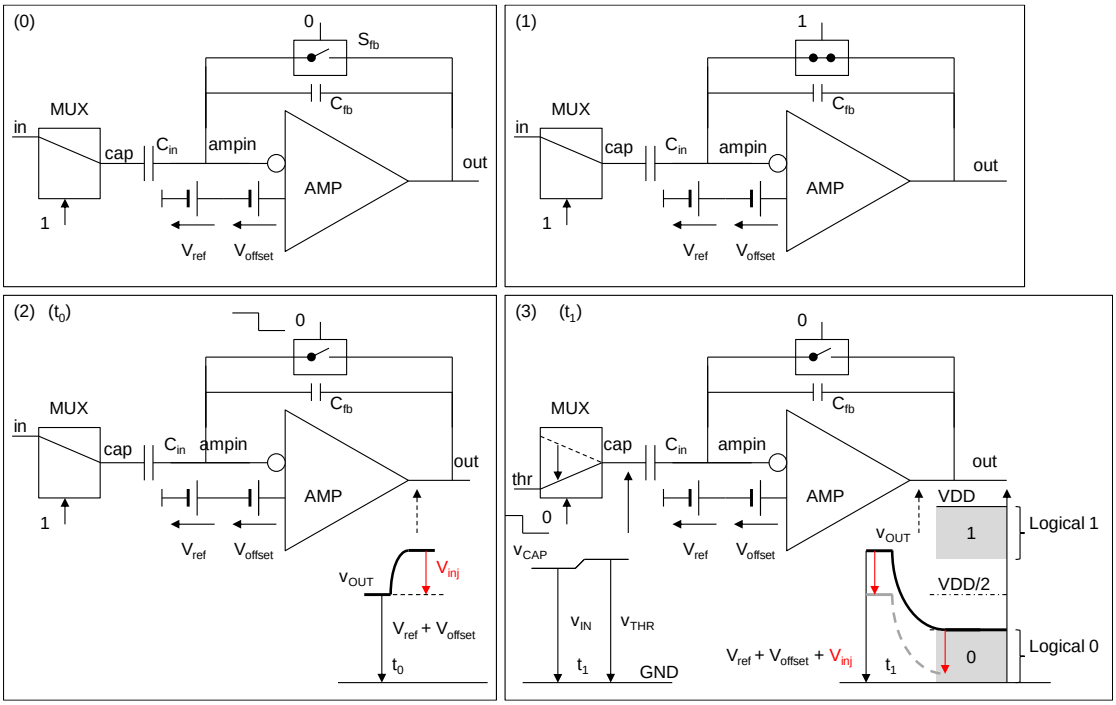


Figure 32: Clocked comparator – influence of charge injection

Due to charge injection, after **opening S_{fb} (at $t=t_0$)** (Figure 34 (2)), the output rises to:

$$v_{OUT}(t_0 + \Delta t) = V_{ref} + V_{offset} - \frac{Q_{inj}}{C_{fb}} = V_{ref} + V_{offset} + V_{inj} \qquad (22)$$

If an **NMOS switch** is used, Q_{inj} is **negative**, so V_{inj} is **positive**. The potential v_{OUT} is therefore **higher by V_{inj}** than without charge injection (compare to equation 20).

After **switching track from 1 to 0 (at $t=t_1$)** (Figure 34 (3)), the output voltage becomes:

$$v_{OUT}(t_1 + \Delta t) = v_{OUT}(t_0 + \Delta t) + \frac{C_{in}}{C_{fb}}(v_{IN}(t_1) - V_{thr}) = V_{ref} + V_{offset} + V_{inj} + \frac{C_{in}}{C_{fb}}(v_{IN}(t_1) - V_{th}) \qquad (23)$$

This output is also **higher by V_{inj}** than without charge injection (compare to equation 21).

As a result, it is possible that the **output no longer falls within the logical 0 range**.

Charge injection can be **reduced using a dummy switch**. An **alternative solution** is described in the next paragraph.

Compensation of Charge Injection with an Additional Amplifier

The effect of **charge injection** can be **reduced using an additional clocked amplifier AMP2**, as shown in **Figure 35**.

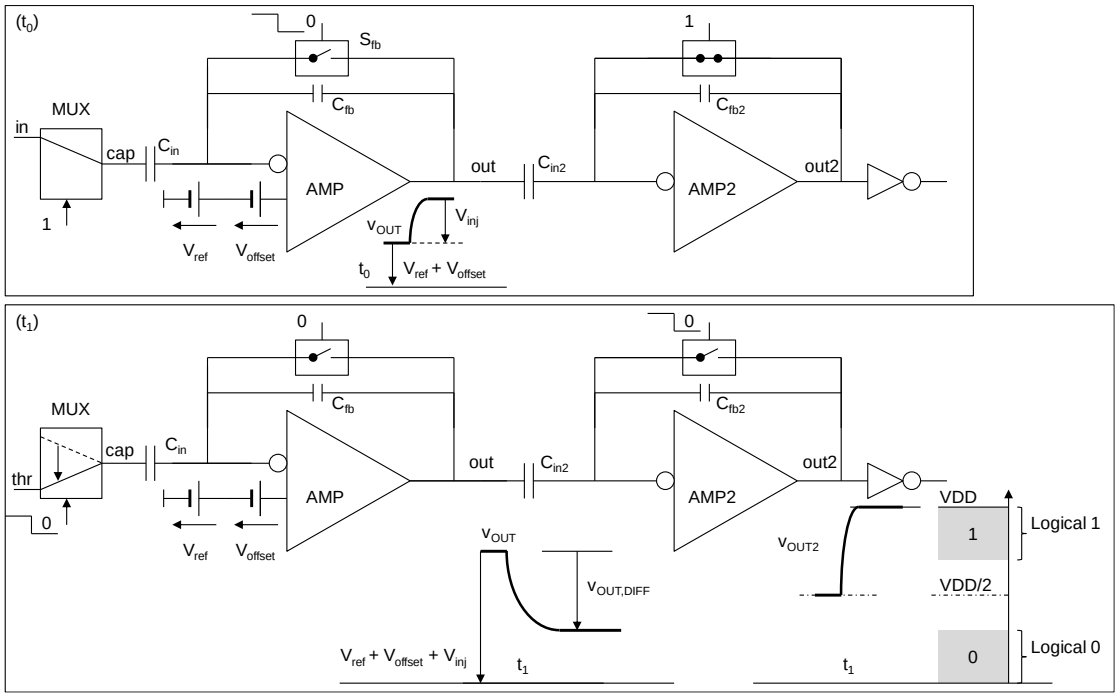


Figure 33: Compensation of charge injection.

The amplifier **AMP2** amplifies the **potential difference**:

$$v_{OUT,DIFF} \equiv v_{OUT}(t_1 + \Delta t) - v_{OUT}(t_0 + \Delta t) = \frac{C_{in}}{C_{fb}}(v_{IN}(t_1) - V_{thr})$$

Therefore, V_{inj} from the **first amplifier** does **not affect** the output of AMP2.

Due to the **additional gain** of the second amplifier, C_{in2}/C_{fb2}, the output out2 reaches a **clear logical level**, even in the presence of **charge injection in the second amplifier**.

The principle is the same as before: the **signal $(C_{in}/C_{fb})(V_{IN}-V_{thr})$** is **amplified by AMP2**, while the **errors of the first amplifier** (V_{offset}, V_{inj}) are **not amplified**.