Lecture 9

The theme of this lecture are differential amplifiers. We will describe:

Applications

Classification

Differential and common mode gain, CMRR

Fully differential amplifier

Common mode feedback

Operational amplifier

Variant with R_{load}

Variant with current mirror

Differential amplifiers

In the previous lectures we had the amplifiers with one input and an output, precisely single ended input and single ended output. These amplifiers are called single-ended amplifiers.

The topic of this lecture is the difference amplifier. As the name suggests, they amplify the difference between two input signals. An equally important feature is that a differential amplifier should not amplify instantaneous signals. So if the two input signals increase by the same contribution, the output should remain unchanged.

The first application of differential amplifiers is the measurement of two signals relative to each other, i.e. measurements of signals not related to ground.

We have an electrical circuit, a resistance network and want to measure the currents flowing through the resistance. So we were only interested in the voltage between the resistance electrodes and not the absolute potentials related to ground. We apply the differential amplifier.

Fig 1 shows the symbol of the single ended amplifier with its small signal model. We assume the implementation with a transistor. Therefore the amplifier has the input voltages v_g (gate voltage) and v_s (source voltage). V_s is also the reference potential. Therefore the single ended amplifier shown in Fig has two input contacts. The contact vs is also connected to the source at the output.

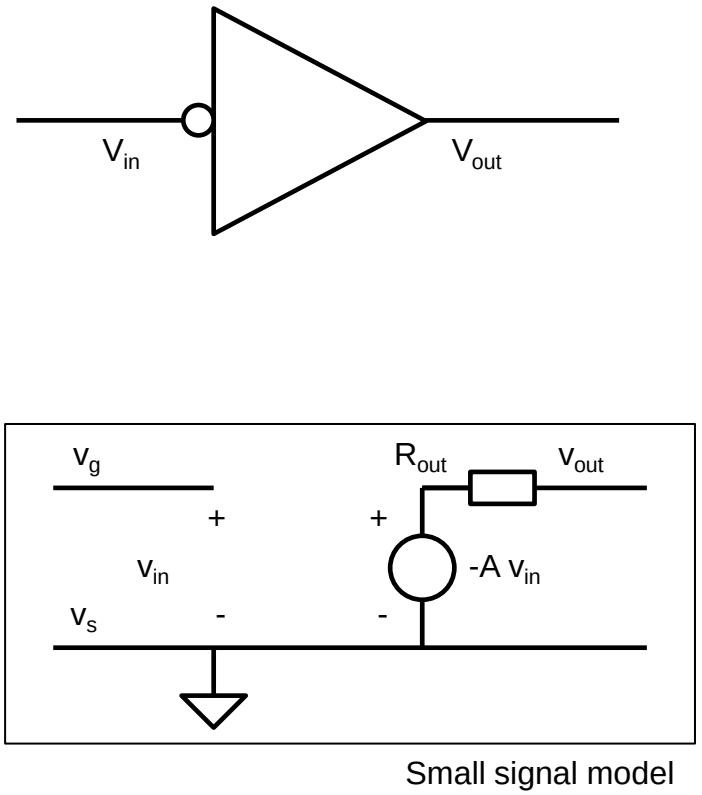


Fig 1: Single ended amplifier

The topic of this lecture is the differential amplifier. As the name suggests, they amplify the difference between two input potentials. It holds:

$$V_{out} = A\,(V_{inp} - V_{inn})$$

If the two input potentials increase by the same value, the output voltage should remain unchanged.

Fig 2 shows a differential amplifier with its small signal model.

The small signal circuits of single ended amplifier from Fig 1 and the differential amplifier from Fig 2 have following differences:

In the case of the single ended amplifier the negative input (potential v_s) is connected to the output source. In the case of the differential amplifier, the output source is disconnected from the input.

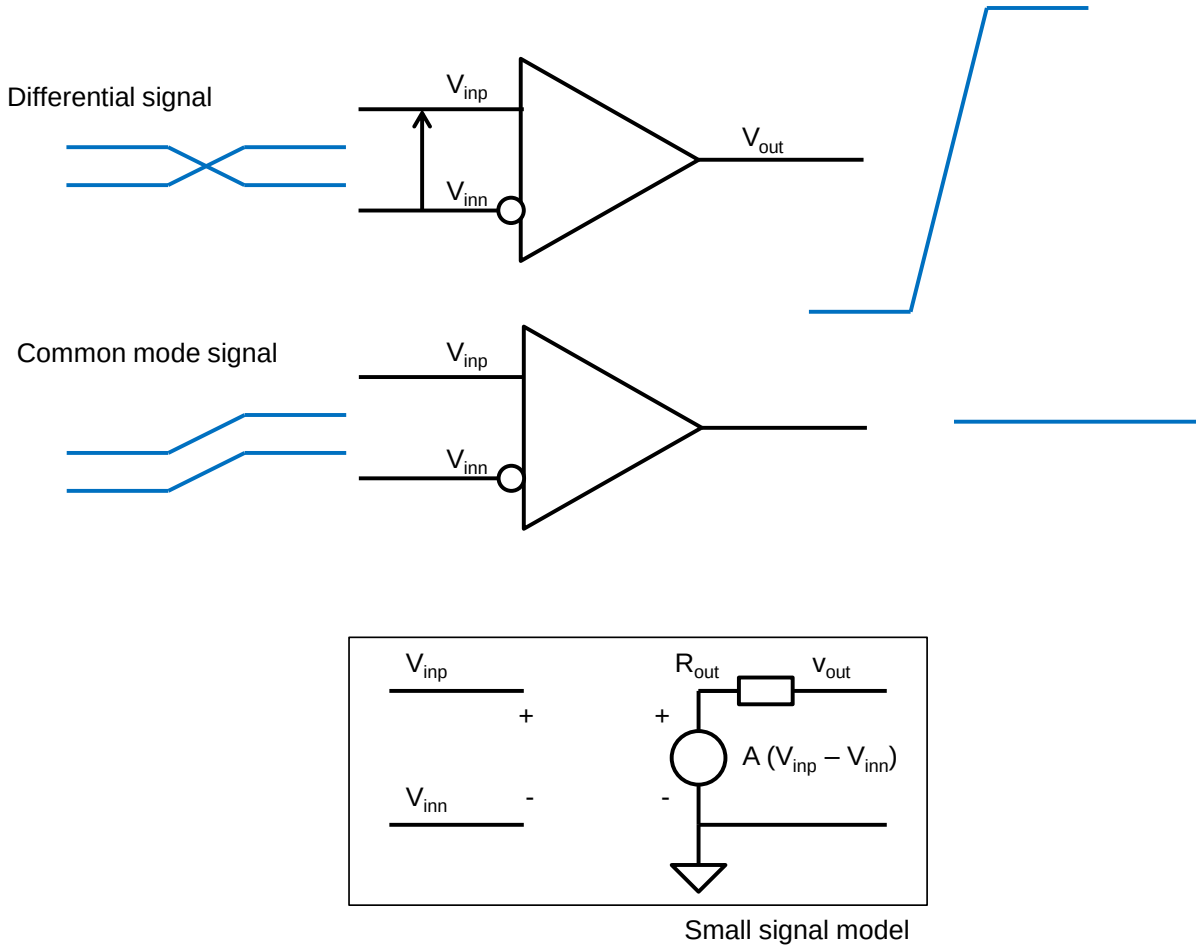


Fig 2: Differential amplifier

Applications of the differential amplifier

The first application of differential amplifiers is the measurement of two signals relative to each other.

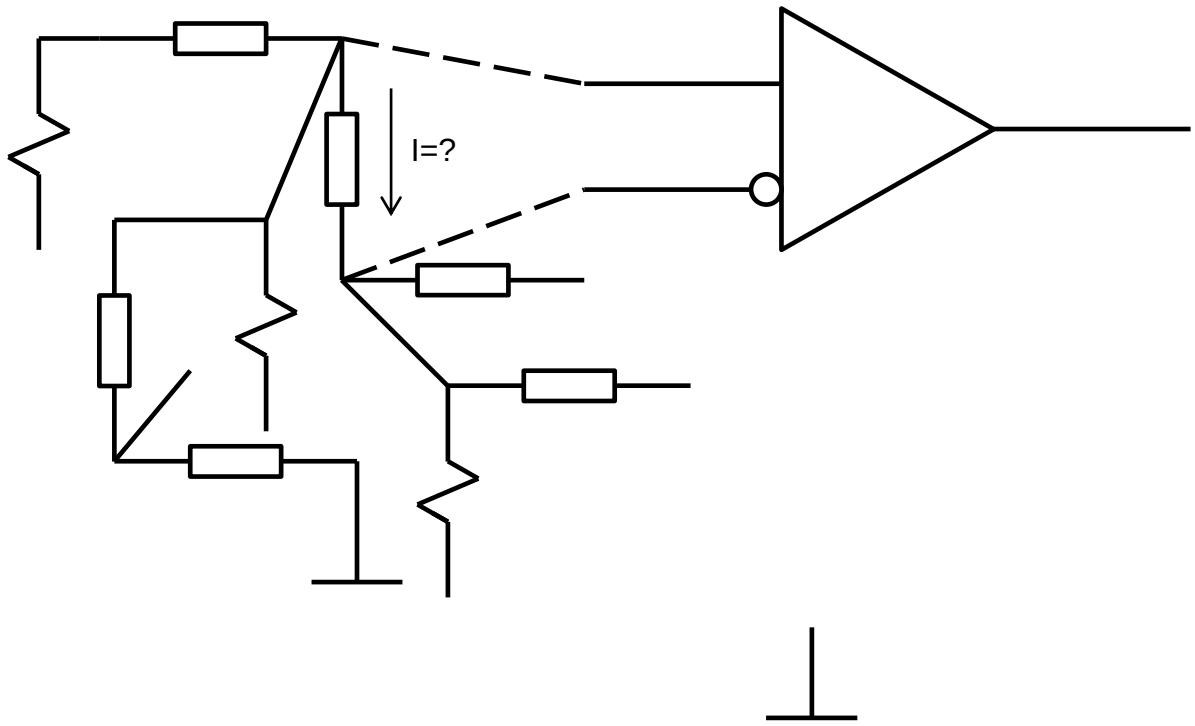


Fig 3: Applications: measurements of voltage differences

Assume that we develop an amplifier that measures the currents flowing through resistors (Fig 3). The device should only measure the voltages across resistances and not the potentials with respect to ground. We use differential amplifier for this purpose.

Another application of the differential amplifiers is the differential signal processing. The idea is here that a signal is not transmitted as a voltage related to ground by means of a single line then as potential difference between two symmetrical lines. Ideally, the two voltages of the line pair have a constant sum, i.e. a phase difference of 180 degree. This is illsutrated in Fig 4.

In the case of single ended signal transmission, one needs also two lines, the signal line and the ground line. The ground line is usually wide and it is used by many circuits. The ground is often conencted to earth potential. The ground line has a different shape than the signal line. In the case of differential signal transmission, the two lines are similar. One example is twisted pair.

Such signal transmission has some advantages:

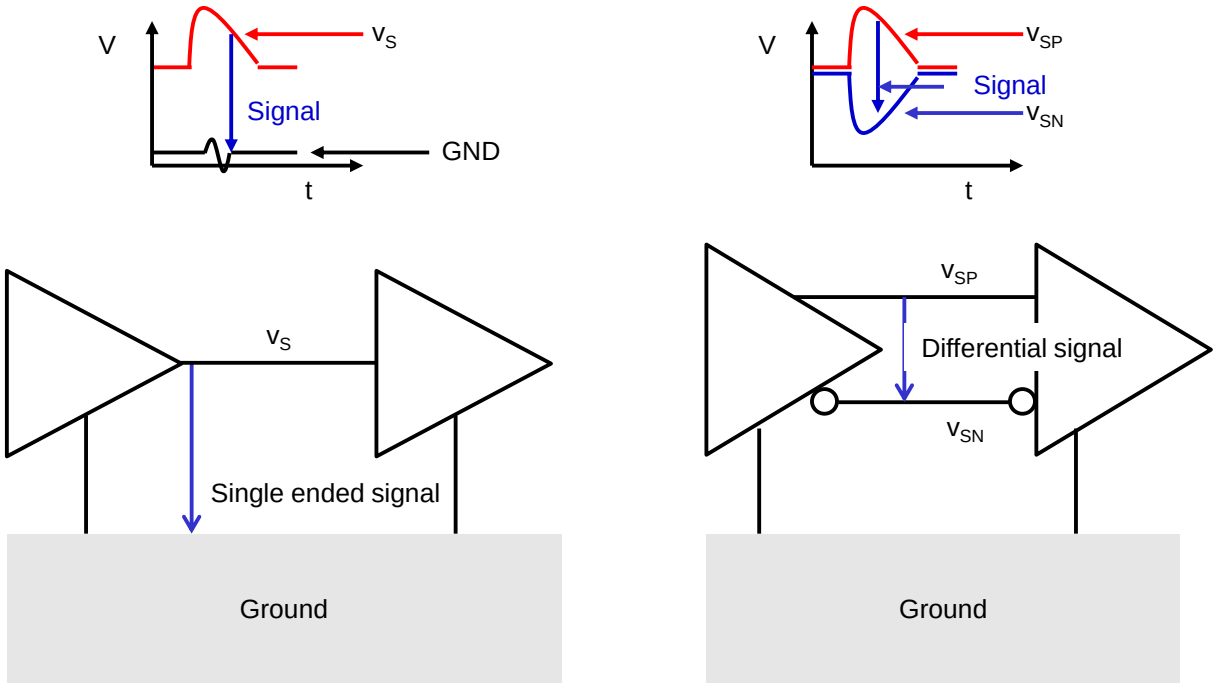


Fig 4: Single ended and differential signal

The amplitude of the differential signal is two times larger than the amplitude of each voltage when individually considered (Fig 5). A large amplitude also means a large signal noise ratio.

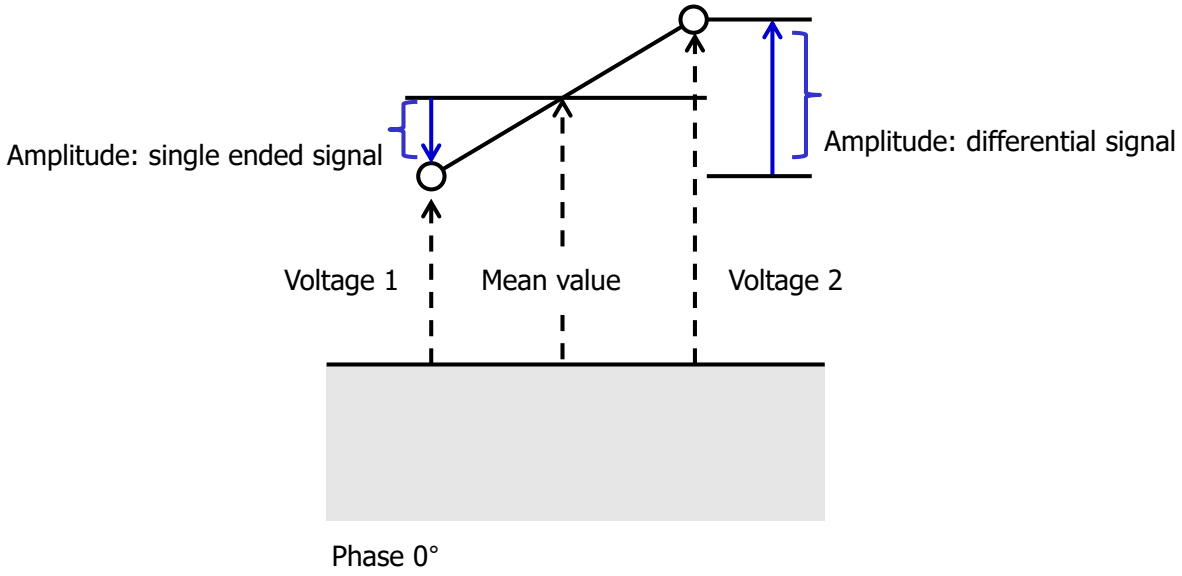


Fig 5: The amplitude of the differential signal is two times larger than the amplitude of each voltage when individually considered

Suppose we design a circuit in a modern chip technology. The supply voltage is only about 1.0 V. A single-ended signal can therefore have a maximal peak to peak amplitude of 1 V. A differential signal on the other hand has a maximum peak to peak amplitude of 2 V. For the same signal to noise ratio, we can accept two times larger noise in the case of differential signals. Fig 6 illustrates this.

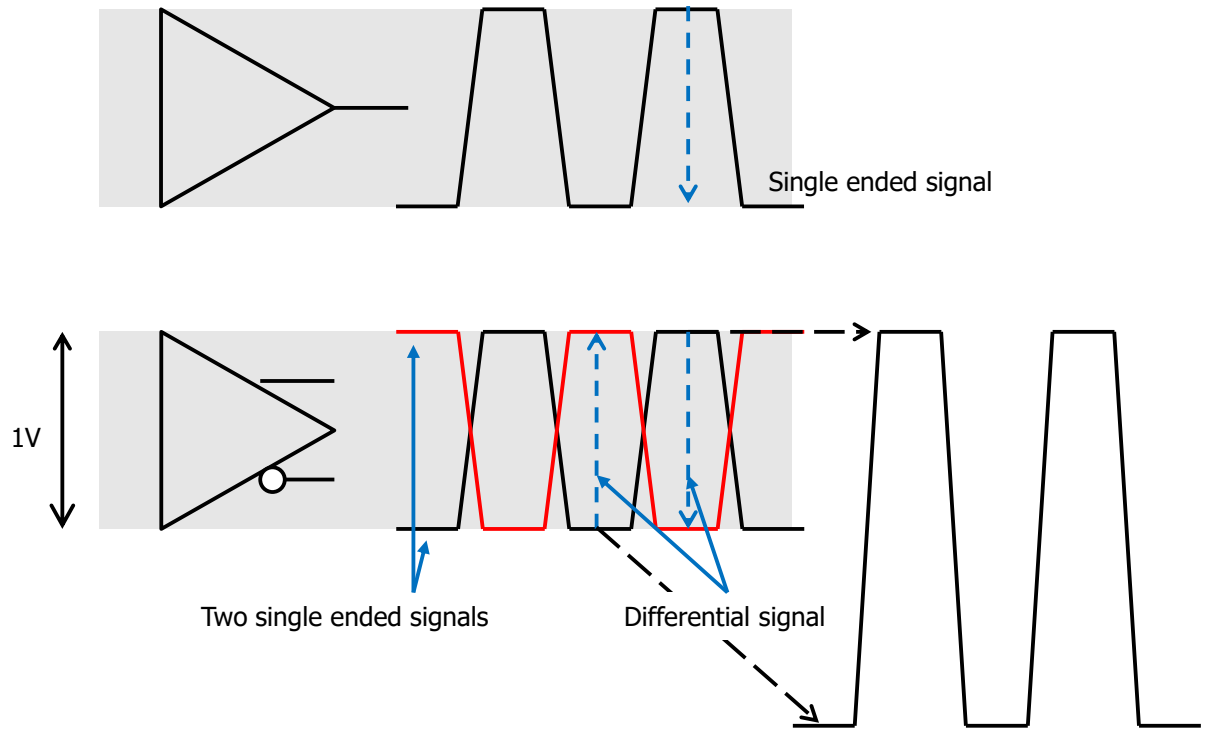


Fig 6: The amplitude of the differential signal is two times larger than the amplitude of each voltage when individually considered

If the two voltages of a differential pair have a constant sum, they almost do not cause electromagnetic intereference at a distance.

Capacitive or inductive crosstalk from externals has a small influence to a differential signal. This is illustrated in Fig 7. Imagine that a single ended signal line (CMOS line) is routed over a differential pair of lines. Both signals (voltages) of the differential pair are slightly disturbed by capacitive crosstalk from the CMOS line. The disturbances are in phase. If the receiver only amplifies the difference of voltages, such disturbance does not affect the signal reception, it is not amplified.

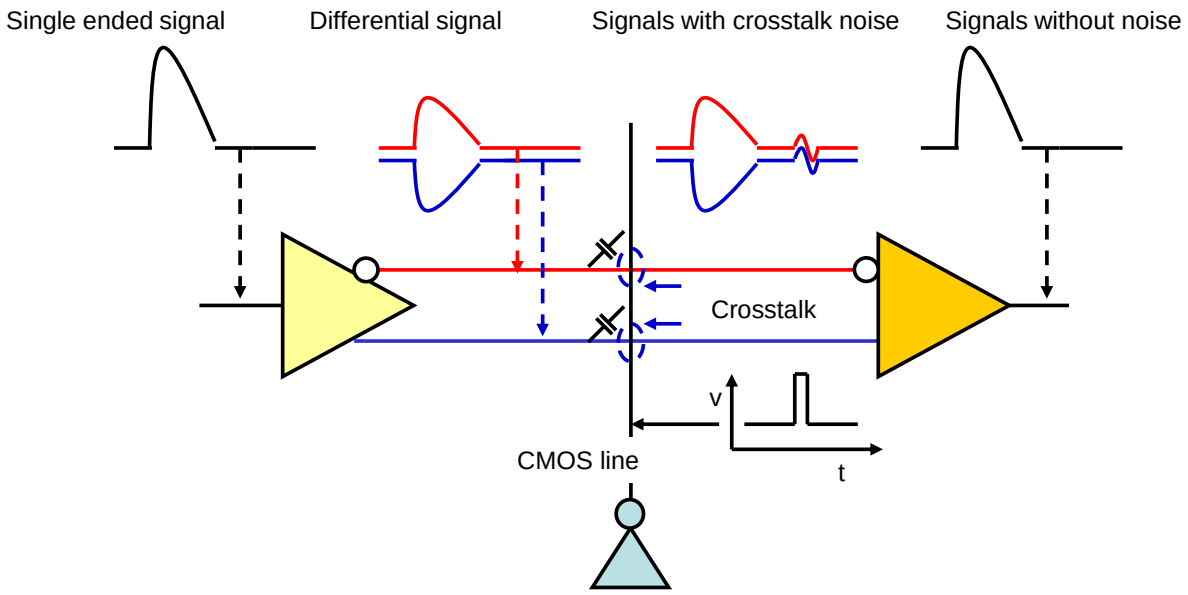


Fig 7: Capacitive or inductive crosstalk from externals has a small influence to a differential signal

The differential amplifier is used as a basic electronic component, the operational amplifier. Various circuits can be realized using the operational amplifier, such as the feedback amplifiers, filters, oscillators and different mathematical operations (integrator, differentiator). Hence the name operational amplifier.

Fig 8 shows the inverting and the non-inverting amplifier.

Notice that we can also implement an inverting amplifier with a single ended amplifier, while a non-inverting amplifier requires a differential amplifier.

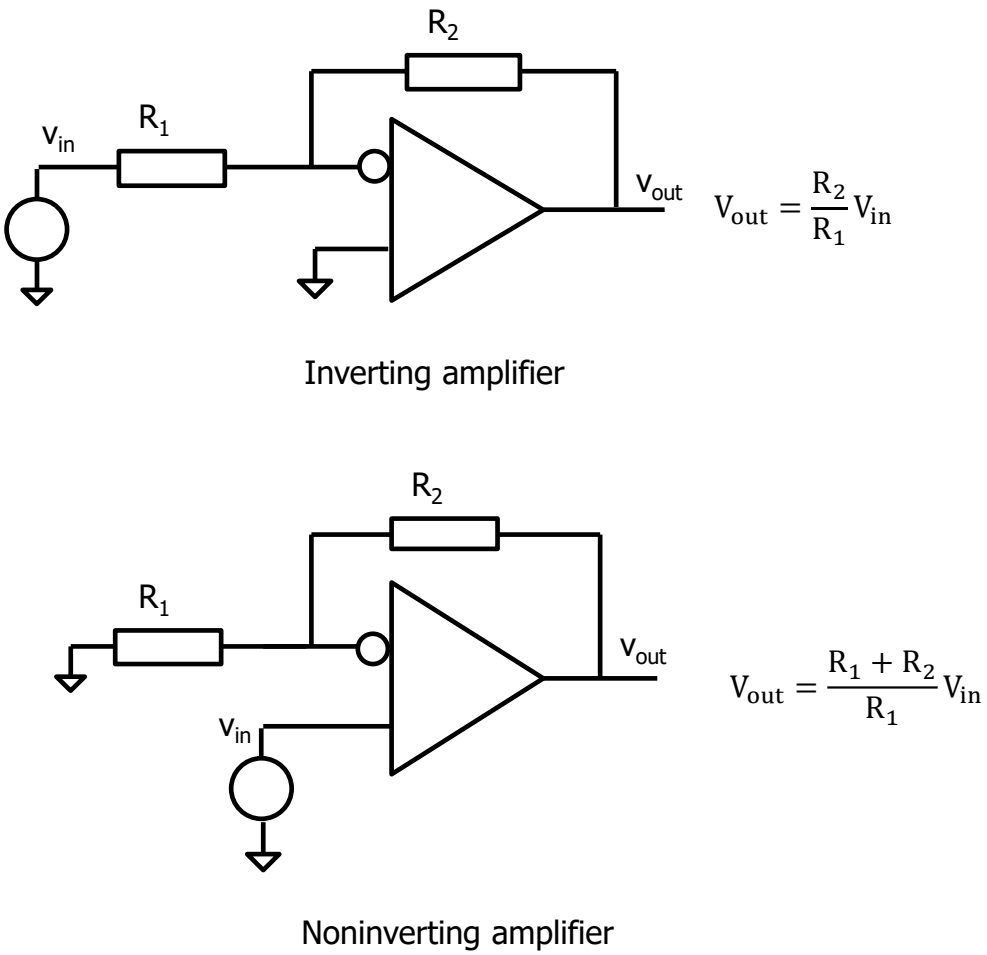


Fig 8: Inverting and noninverting amplifier

Another application is the comparator. Fig 9 shows an analogue comparator and its input and output signals. The output signal changes between VDD and GND, depending whether V_{inp} is larger or smaller than V_{inn}.

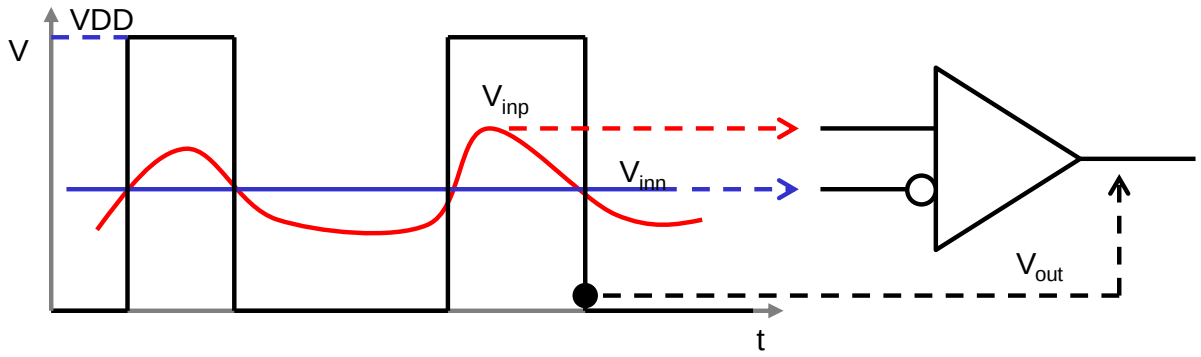


Fig 9: Differential amplifier as comparator

The differential amplifier can be also used in digital circuits. Examples are the receivers and drivers for differential data transmission (Fig 10). The advantage of this transmission is that the amplitude of the differential signal is two times larger than the amplitude of each voltage of the line pair when individually considered. Therefore, logical levels (bits) can be reliably transmitted with less amplitude/line. Low Voltage Differential Signaling (LVDS) works on this principle.

Logical components such as gates or flip-flops can also be realized based on differential amplifiers. Such logic always consumes a constant current. Therefore, it does not cause voltage changes on supply lines if they have significant resistance. Fig 11 shows a SR-latch, a D-latch and an ring oszillator.

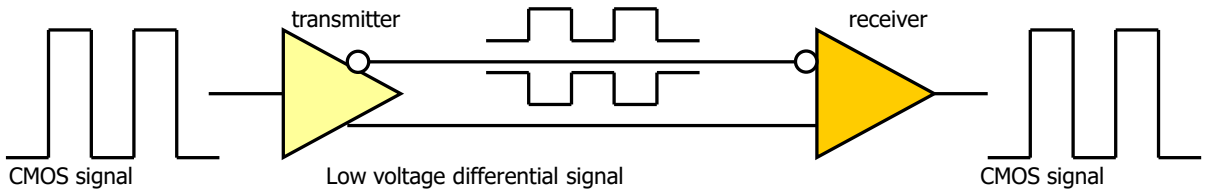


Fig 10: Low voltage differential signalling

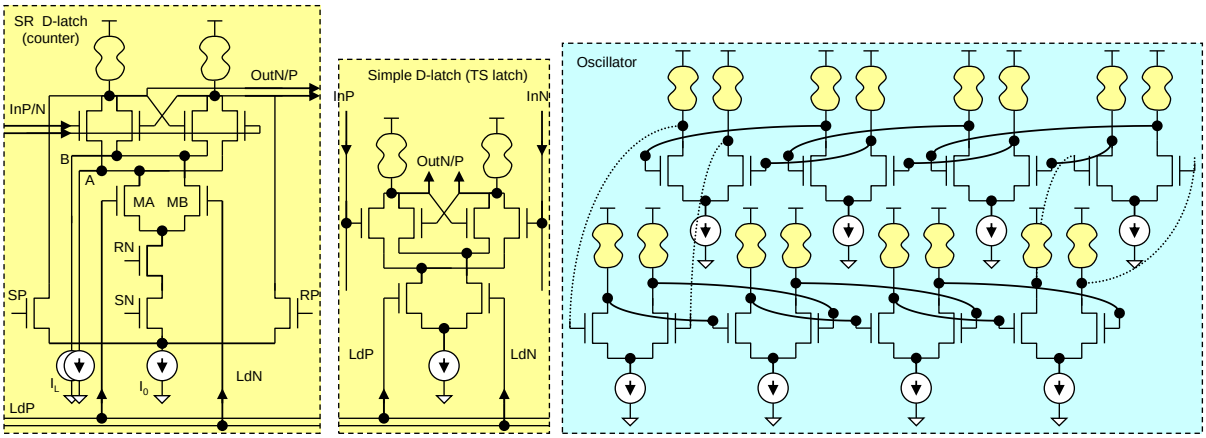


Fig 11: Differential logic gates

Classes of differential amplifiers

We can classify the differential amplifiers according to the input/output type (Single Eneded, Differential), Fig 12.

An operational amplifier has e.g. the differential input (two pins) and a signal ended output. The output signal is related to ground.

There are also differential amplifiers with the differential output. The two voltages of the differential outputs have opposite phases and their sum is constant. These amplifiers are called fully differential amplifiers.

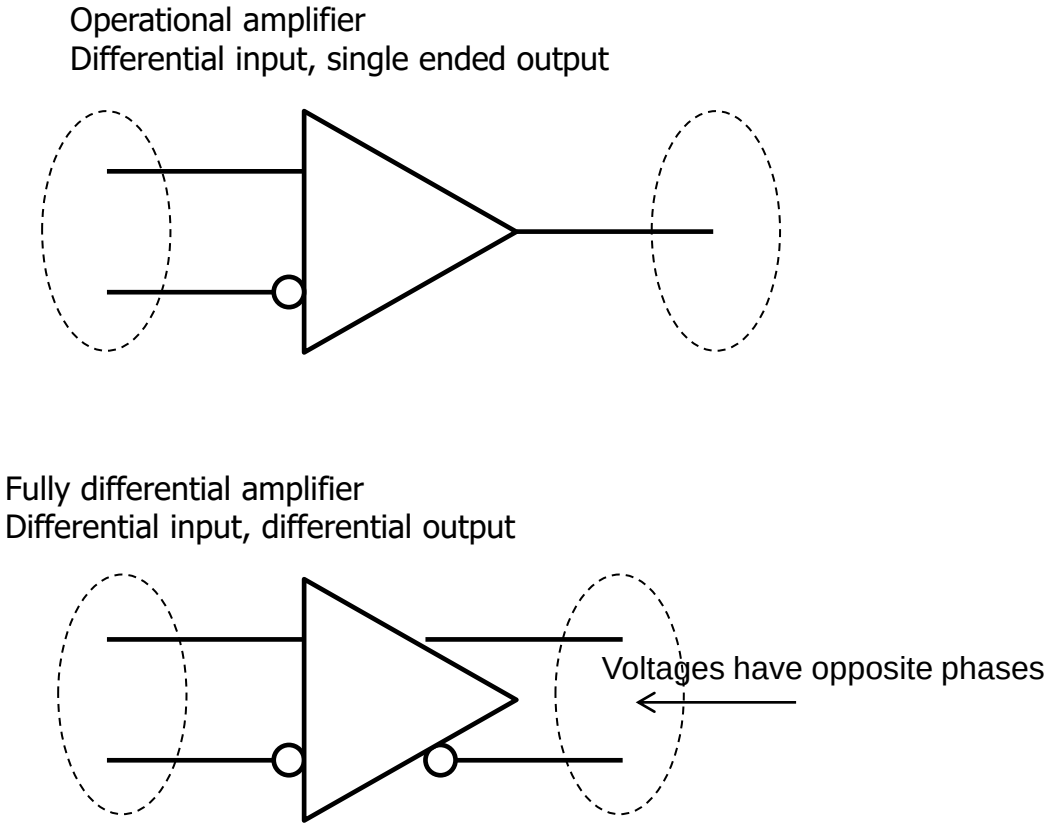


Fig 12: Different types of differential amplifiers

The main application of these fully differential amplifiers is the precise analogue signal processing. For example, such amplifiers are used in the switcherd capacitor amplifiers (Fig 13).

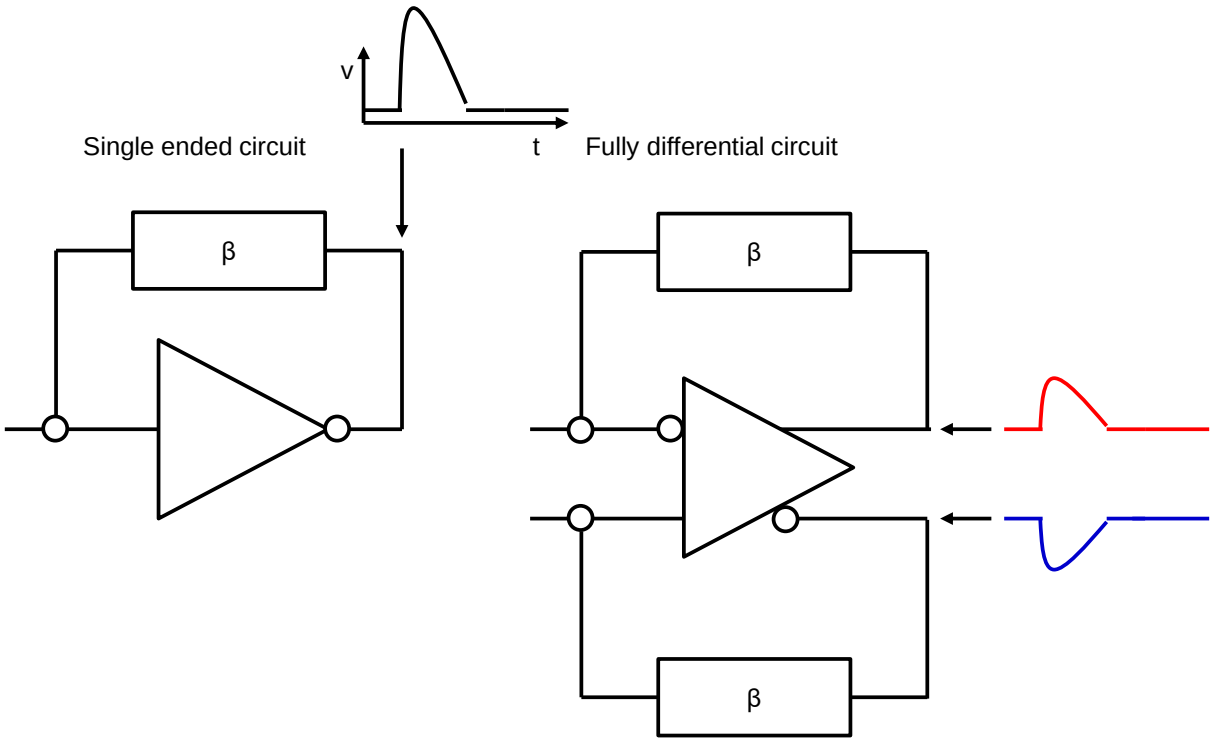


Fig 13: Single ended- and differential analogue signal processing

Transistor implementation

The basic component of a differential amplifier is the differential pair.

The pair consists of identical transistors T_{in1} and T_{in2} that share one bias current (Fig 14). The bias currennt is either generated with a current source Ibias or with a large resistor Rbias. The source electrodes of T_{in1} and T_{in2} are usually connected. The current increase in one transistor of the pair leads to the equal current decrease in the other transistor. It holds:

$$I_{ds1} + I_{ds2} = I_{bias}$$

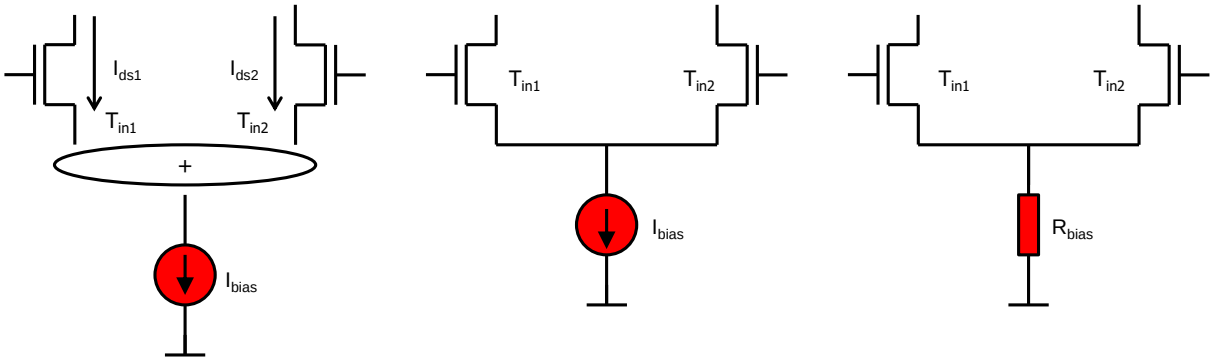
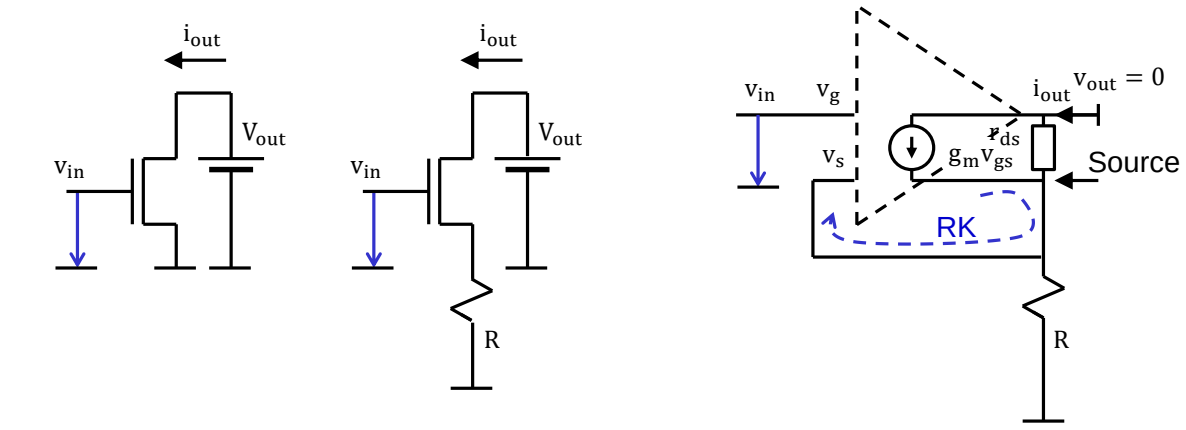


Fig 14: Differential pair

V-I Converter

To explain the operation of the differential pair, we would like to first introduce a simpler building block. It is the V-I converter based on a transistor with a resistance between the source electrode and the ground. The drain of the transistor is the current output and it is connected to the constant voltage V_{out}, which assures that the transistor works in saturation.

The source resistance R creates a negative feedback. The feedback can be recognized more clearly in the small signal schematics Fig 15 right. Since the source contact (v_s) is not connected to gound, there is a signal transmission from the current source of the transistor to the input which causes feedback. Notice that the current output (drain) is at 0V in the small signal circuit (ground symbol).



Simple V-I converter | V-I converter with source resistor | V-I converter with source resistor (small signal circuit)

Fig 15: V-I Convertor

How does the feedback affect the V-I converter?

Firstly, it reduces the amplification.

Secondly, it increases the output resistance.

We will apply the Mason's gain formula to calculate the current gain of the circuit

:

$$G = \frac{A_{IN}A_{OL}}{1-\beta A} \quad (1)$$

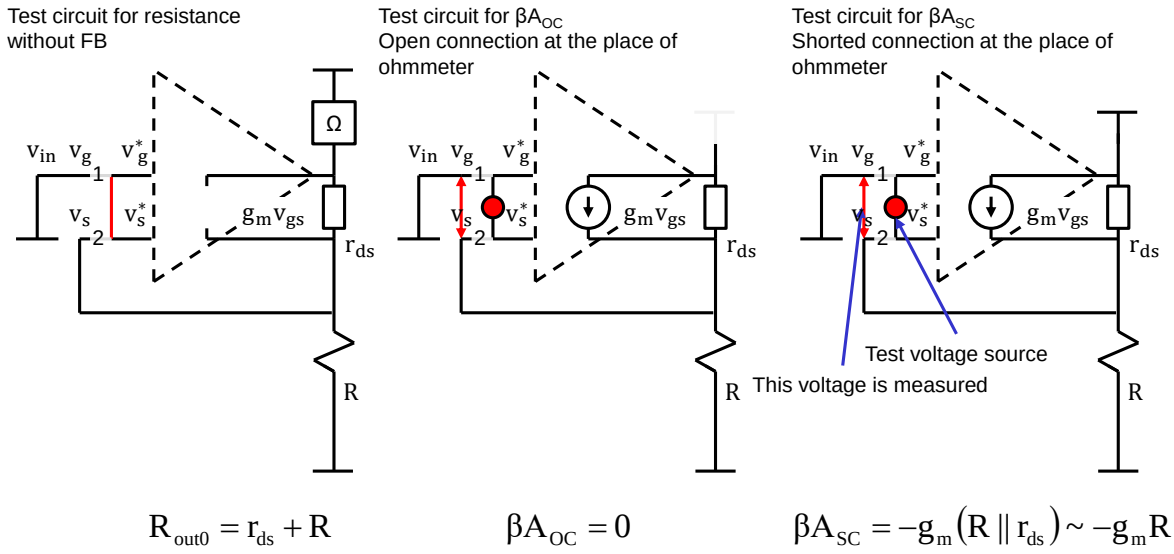
And the Blackman's formula to calculate the output resistance with feedback:

$$R_{out} = R_{out0}\frac{1-\beta A_{SC}}{1-\beta A_{OC}} \quad (2)$$

Fig 16 shows the test circuits for the calculation of the factors in Mason's formula: A_{IN}, A_{OL} and βA. Fig 17 shows the circuits for the factors of Blackman's formula: R_{OUT0}, βA_{OC} and βA_{SC}.

The approach for the calculation is similar as in the case of the inverting amplifier that analysed in lecture 5. There are a few small differences. The output variable is current in the case of V-I converter. For this reason the output node (transistor drain) must *not* be open circuit when we calculate A_{OL} and βA (the drain must be connected to something). The drain is set to 0 V in the corresponding test circuits. Generally, when we calculate A_{IN}, the output variable (either current or voltage) must be forced to be 0 (A or V). In the case of inverted amplifier, we set the output to 0 V. In the case of V-I converter we leave the output node unconnected (open circuit) since it holds $i_{out} = 0$ in this case. This is shown in Fig 16.

Remind, that we need to cut the feedback in front of the amplifier when we calculate the gain factors. In the case of inverting amplifier, it was enough to cut one input line of the transistor model (v_g). The other input line v_s was grounded and it was not necessary to cut it. In the case of V-I converter, the input variable is the voltage difference $v_g - v_s$. Voltage that is fed back acts on v_s and the input signal on v_g. For this reason, we have cut both the gate and the source line in points 1 and 2.



$$R_{out0} = r_{ds} + R \qquad \beta A_{OC} = 0 \qquad \beta A_{SC} = -g_m\left(R \parallel r_{ds}\right) \sim -g_m R$$

Fig 16: Test circuits for the calculation of current gain with the Mason's gain formula

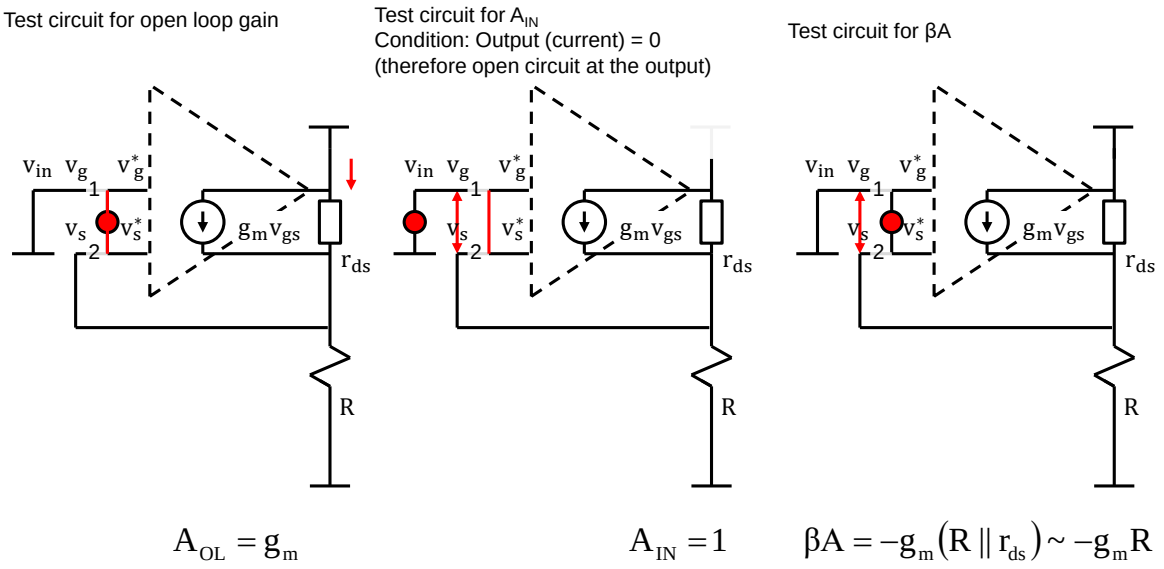


Fig 17: Test circuits for the calculation of output resistance with the Blackmans formula

Notice that the loop gain with opened output is equal to zero: $\beta A_{OC} = 0$ (Fig 17, middle). This is caused by the opened line at the output. (The imaginary ohmmeter is replaced with open line.) The current through resistor R is for this reason 0. It follows: $v_s = 0$, $v_{gs} = 0$ and $\beta A_{OC} = v_{gs} / v_{test} = 0$.

If we replace the gain factors from Fig 16 and Fig 17 in equations (1) and (2), we obtain the formula for the current gain of the V-I converter:

$$G = \frac{i_{out}}{v_{in}} = \frac{g_m}{1+g_m R} \qquad (3)$$

And the formula for output resistance:

$$R_{out} = (R + r_{ds})[1 + g_m(R||r_{ds})] = (1 + Rg_m)r_{ds} \qquad (4)$$

The gain with feedback G is equal to the gain without feedback g_m divided by the factor $1 - \beta A$, i.e. $1 + g_m R$. The output resistance with feedback is equal to the output resistance without feedback $r_{ds} + R$ multiplied by the factor $1 - \beta A_{SC}$, i.e. $1 + g_m R$.

Fully differential amplifier

We can obtain a fully differential amplifier by taking two single-ended amplifiers (in simples case two common source amplifiers), by connecting the sources of two input transistors and by biasing of such common source (node S in Fig 18) using a resistor R_{bias} or a current source.

The output variable is defined as $\Delta V_{out} = V_{out1} - V_{out2}$.

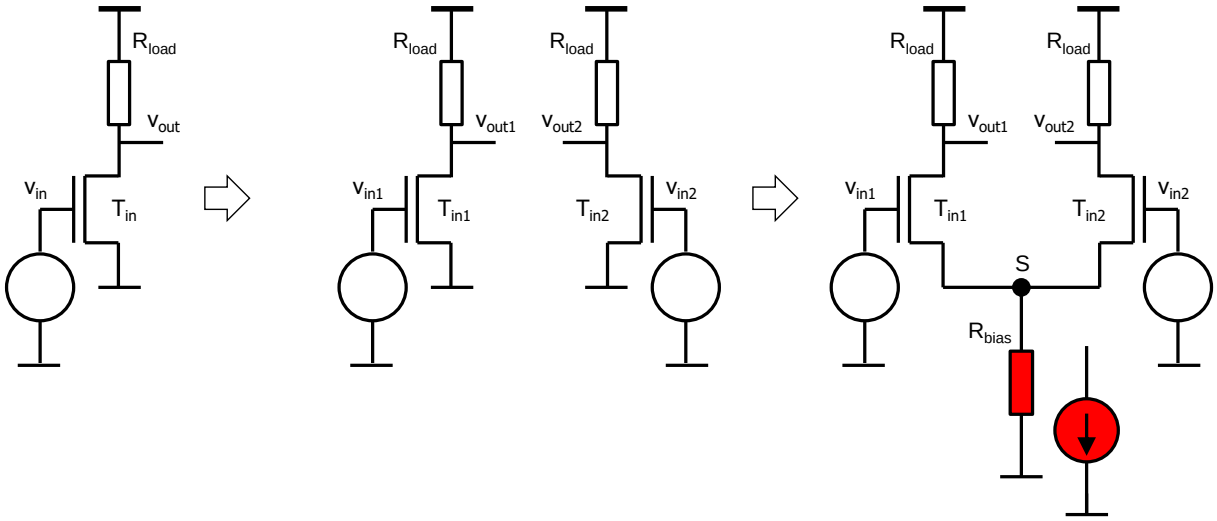


Fig 18: Fully differential amplifier

Let us calculate the voltage gain.

Since we have two output voltages (V_{out1} and V_{out2}) we can for each of them define amplifications.

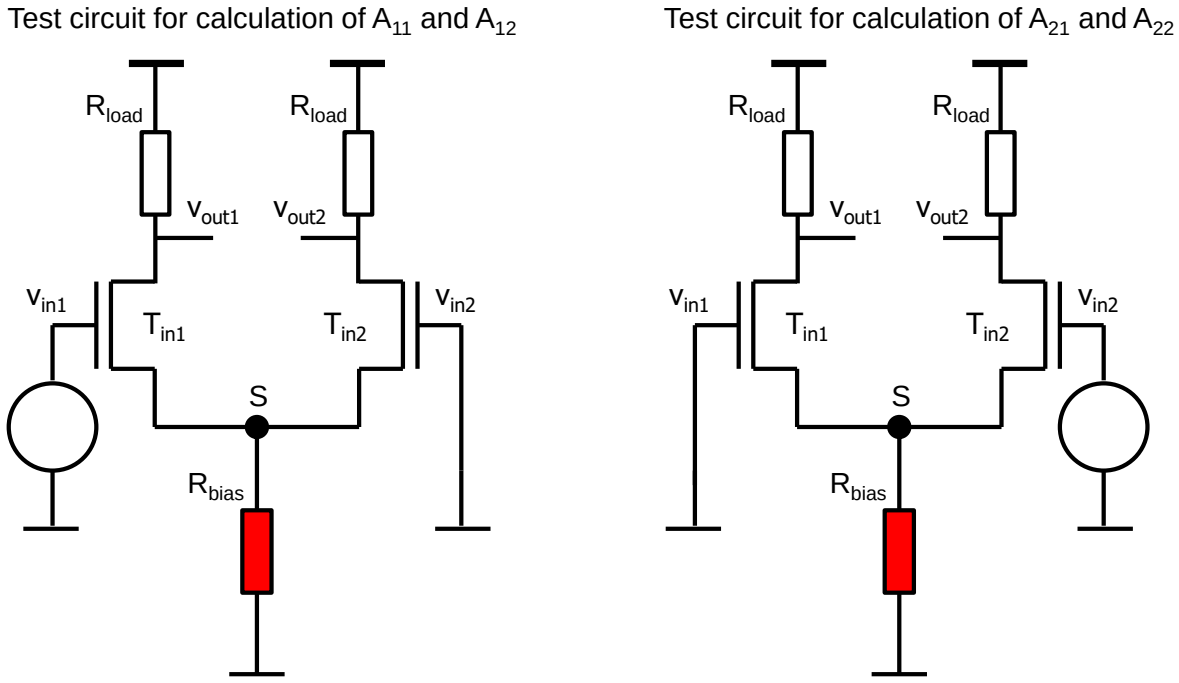


Fig 19: Fully differential amplifier: Test circuits for the calculation of different gains

We could further apply the principle of superposition and consider the two input voltage sources individually. We switch off source V_{in2} by replacing it with a short circuit to ground and calculate the outputs as a function of V_{in1}. In this way we obtain the gains: $A_{11} = V_{out1}/V_{in1}$ and $A_{12} = \Delta V_{out2}/V_{in1}$ (Fig 19, left).

Then we repeat the calculation for the second source and calculate A_{21} und A_{22} (Fig 19, right).

We will calculate the gain in a bit different way:

It is possible to express two input voltages as a sum of its mean value (referred to as the common mode voltage) and the difference voltage (Fig 20).

We define the difference voltage as:

$$v_{diff} = v_1 - v_2$$

The common mode voltage is defined as:

$$v_{cm} = \frac{v_1 + v_2}{2}$$

It holds:

$$v_1 = v_{cm} + \frac{v_{diff}}{2}$$

$$v_2 = v_{cm} - \frac{v_{diff}}{2}$$

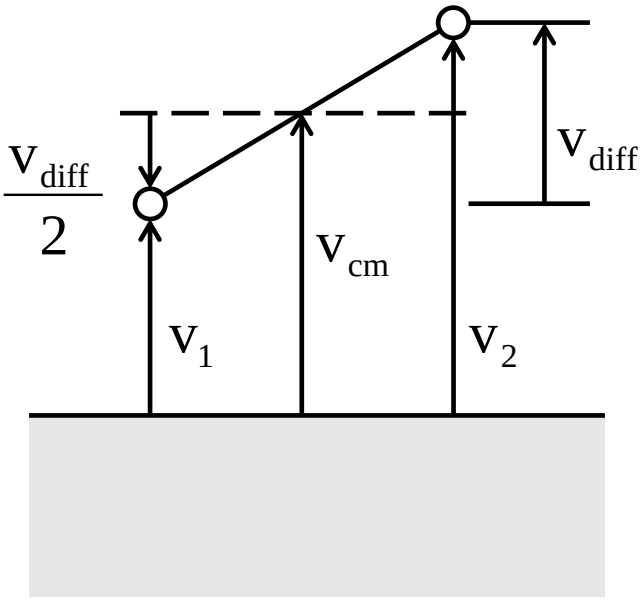


Fig 20: Representation of two voltages v_1 and v_2 as sum of voltage difference v_{diff} and common mode voltage v_{cm}

Therefore we can replace the voltage sources v_{in1} and v_{in2} with voltage sources v_{cm} and v_{diff} (Fig 19).

$$v_{diff} = v_{in1} - v_{in2} \qquad (5)$$

$$v_{cm} = \frac{v_{in1} + v_{in2}}{2} \qquad (6)$$

We define the differential gain as:

$$A_{diff} = \frac{v_{out,diff}}{v_{diff}} \qquad (7)$$

And the common mode gain as:

$$A_{cm} = \frac{v_{out,diff}}{v_{cm}} \qquad (8)$$

Why did we replace v_{in1} and v_{in2} with v_{diff} and v_{cm}?

Firstly, the test circuits for the calculation of A_{diff} and A_{cm} (Fig 21) are more symmetrical than the circuits for calculation of $A_{11} - A_{22}$ (Fig 19). We can make use of this symmetry to simplify the circuits. Secondly, it holds often $A_{cm} \sim 0$ and we need to calculate only one gain A_{diff}.

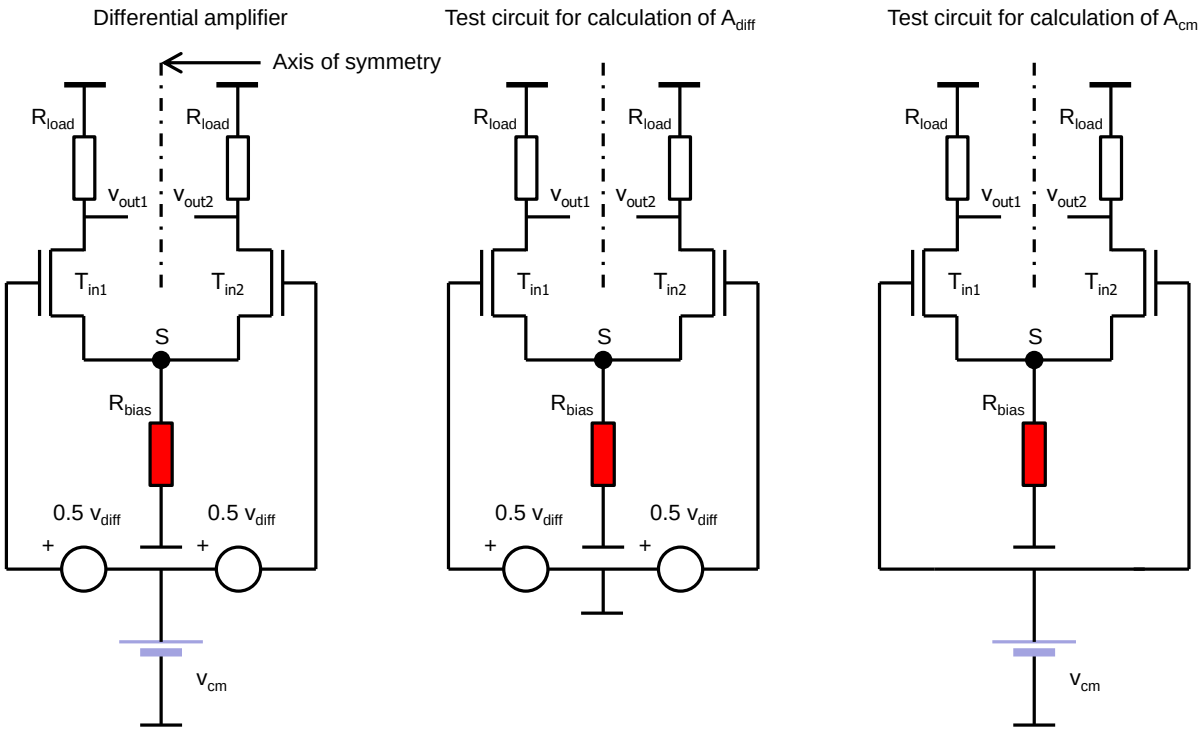


Fig 21: Symmetrical differential amplifier with differential and common mode voltage at the input. Middle figure: test circuit for A_{diff}. Right figure: test circuit for A_{cm}.

Differential gain

Let us first calculate the output voltages as function of v_{dff} and the differential gain A_{diff}.

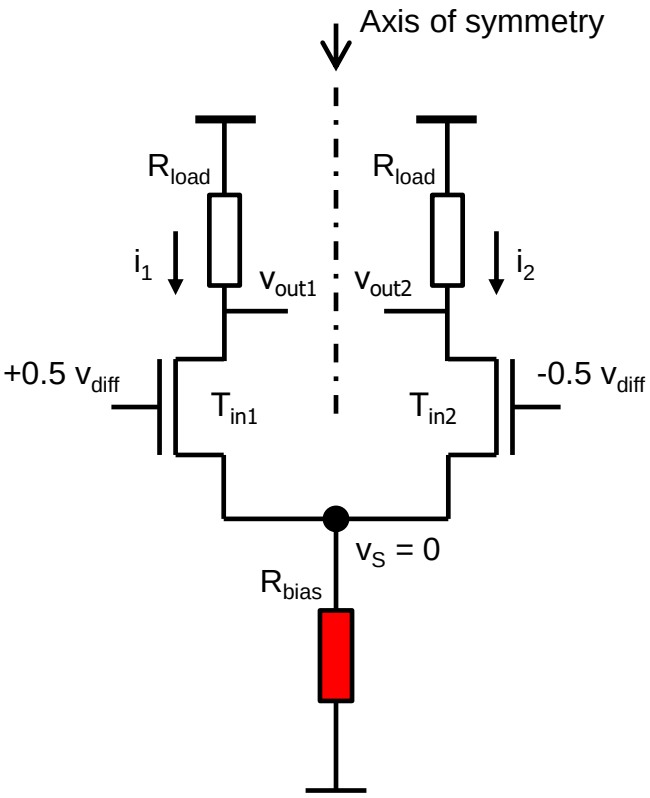


Fig 22: Test circuit for the calculation of the differential voltage gain

Since we perform AC-analysis we set v_{cm} and all DC voltage sources to zero (Fig 22).

The circuit is symmetrical in the way that we obtain the same form when we rotate the circuit by 180° around the symmetry axis. Since this rotation changes only the sign of the input voltages (the absolute value stays equal), the voltages of other nodes also only change their signs. The potentials of the nodes at the symmetry axis are zero. Zero is the only number for which holds a = -a. (Notice that we do AC analysis. In the case of large signals the potentials at the symmetry axis are constant, but not necessarily 0.) Therefore it holds $v_s = 0$. We obtain:

$$i_1 = g_m \frac{v_{diff}}{2}$$

$$i_2 = -g_m \frac{v_{diff}}{2}$$

g_m is the transconductance of T_{in1} and T_{in2}.

The voltages v_{out1} and v_{out2} are:

$$v_{out1} = -g_m R_{load} \frac{v_{diff}}{2} \qquad (9)$$

$$v_{out2} = g_m R_{load} \frac{v_{diff}}{2}$$

The differential gain is:

$$A_{diff} = \frac{v_{out1} - v_{out2}}{v_{diff}} = -g_m R_{load} \qquad (10)$$

Common mode gain

Let us now calculate the output voltage as function of v_{cm} and the common mode gain A_{cm}.

We set v_{diff} to zero and keep v_{cm}, as shown in Fig 23.

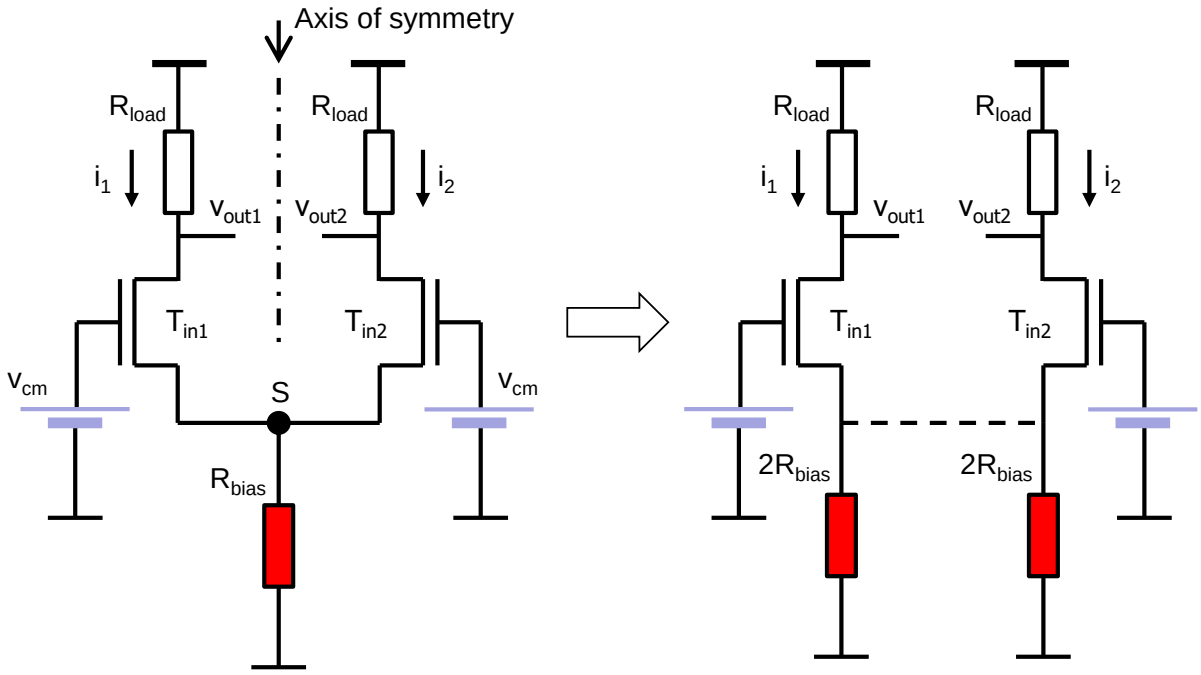


Fig 23: Test circuit for the calculation of the common mode gain

The circuit is symmetrical when it is rotated by 180° around the symmetry axis. When we rotate the circuit, the voltages at the input do not change as well as all other voltages. Since the potentials left and right from the symmetry axis are equal, there is no current through the lines that intersect the symmetry axis. This allows us the split the circuit into two halves (Fig 23, right). The resistances $2R_{bias}$ introduce in each half of the circuit feedback in the same way as in V-I converter, and the drain currents are reduced.

It holds:

$$i_1 = i_2 = v_{cm} \frac{g_m}{1 + 2 g_m R_{bias}}$$

It holds for the voltages at the output:

$$v_{out1} = v_{out2} = -v_{cm} \frac{g_m R_{load}}{1 + 2 g_m R_{bias}} \qquad (11)$$

Let us now calculate the common mode gain.

$$A_{cm} = \frac{v_{out1} - v_{out2}}{v_{cm}} = 0 \qquad (12)$$

We define a common mode rejection ratio (CMRR) as A_{diff}/A_{cm}. CMRR is in our case very large:

$$\mathrm{CMRR} = \frac{A_{diff}}{A_{cm}} = \infty \quad (13)$$

Fully differential amplifier based on folded cascade amplifiers

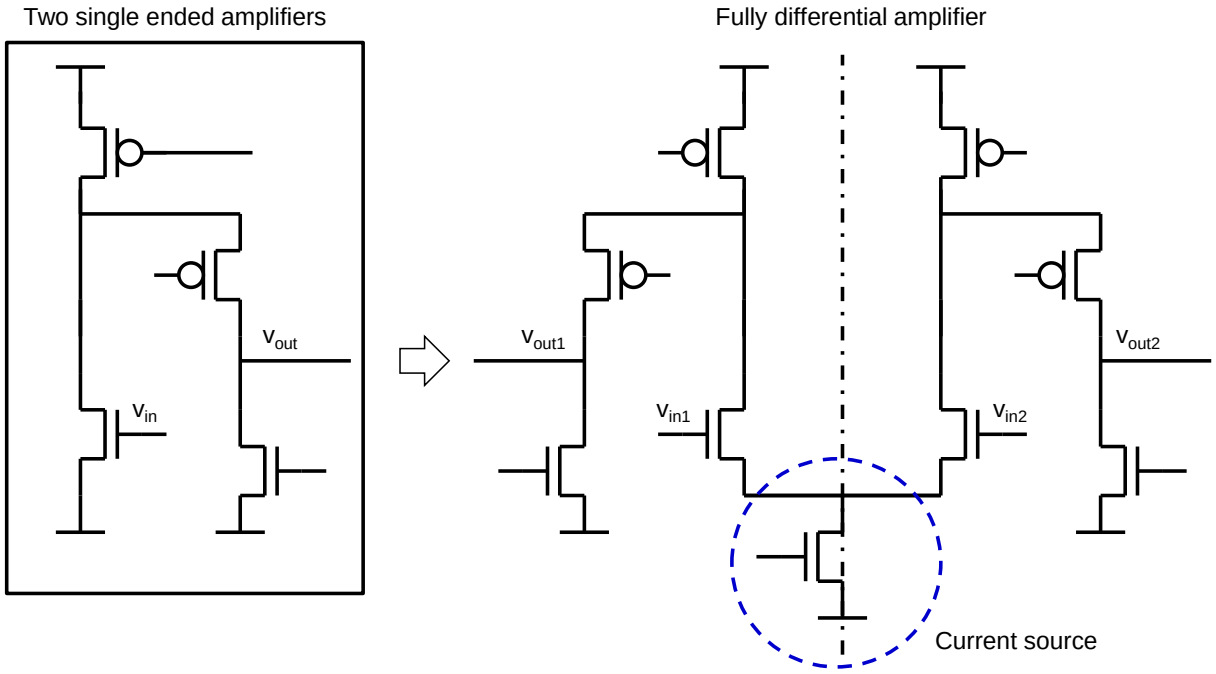


Fig 24: Fully differential amplifier based on two amplifiers with folded cascode

In the first example (Fig 18) we built a fully differential amplifier from two simplest single-ended amplifiers (two common source amplifiers). We could have used more complex single-ended amplifiers, such as the amplifiers with folded cascade, to buld a differential amplifier. Fig 24 shows a fully differential amplifier based on amplifiers with folded cascode. Fig 25 shows the complete cirrcuit with bias elements.

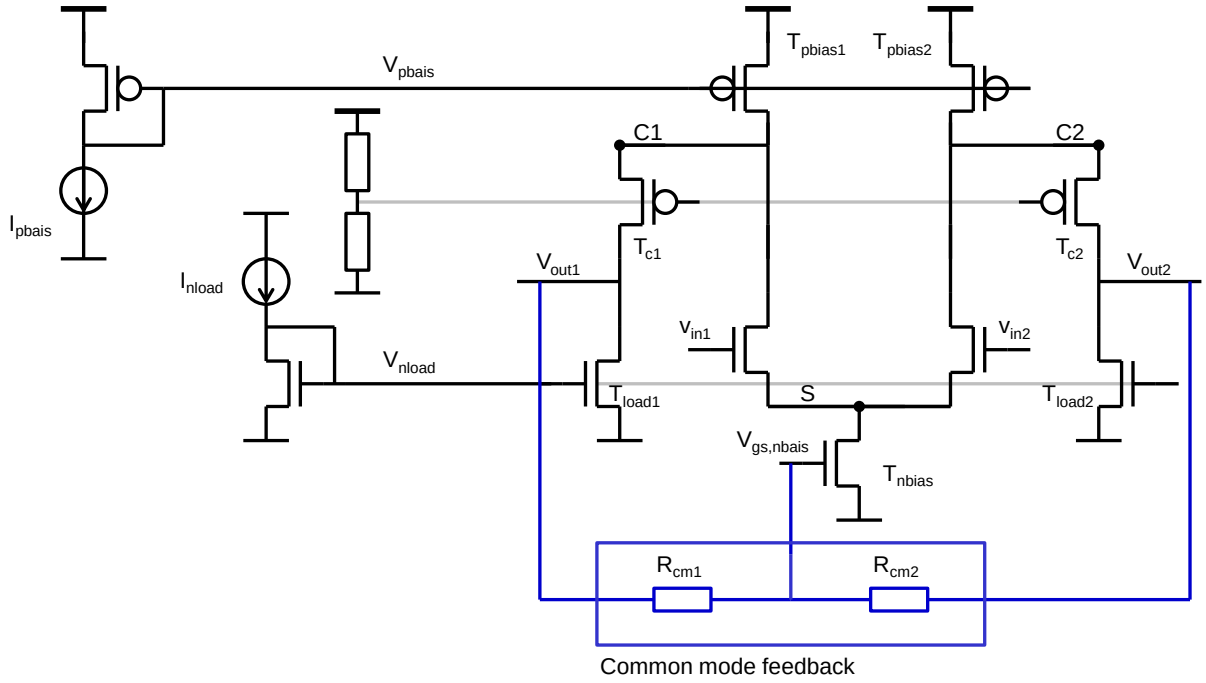


Fig 25: Fully differential amplifier with common mode feedback

Common mode feedback

A fully differential amplifier often requited a common mode feedback. We will discuss it briefly here:

If the amplifier from Fig 25 wouldn't have a common mode feedback, we would have the following problem. If the sum of bias currents through T_{pbias1} and T_{pbias2} (sum of all currents through VDD) is different then the sum of bias currents through T_{load1}, T_{load2} and T_{nbias}, (sum of all currents to GND), the potentials of nodes C1, C2, Out1, Out2 and S will increase/decrease towards VDD or GND until T_{pbias1} and T_{pbias2} or T_{load1}, T_{load2} and T_{nbias} enter the triode region. This cause the DC values of Out1 and Out2 to become too high or low and therefore a small gain.

To prevent this, an active regulation for the gate voltage of T_{nbias} (V_{nbias}) is introduced. It should ensure that DC voltages in the Out1 and Out2 nodes are approximately ½ VDD. We call this regulation the common mode feedback. The easiest way to design it is using two resistors R_{cm1} and R_{cm2} as shown in Fig 25.

Working principle

Suppose the currents through T_{pbias1} and T_{pbias2} are too large. It flows then more current into nodes C1 and C2 through T_{pbias1} and T_{pbias2} from VDD than through T_{nbias}, T_{load1} and T_{load1} to GND. Therefore, the potentials of nodes C1 and C2 increase. This increases the $|v_{gs}|$ of transistors T_{c1} and T_{c2}, and finally Out1 and Out2 potentials.

The resistors $R_{cm1/2}$ cause that:

$V_{gs,nbias} = \frac{V_{out1}+V_{out2}}{2}$.

The increase of V_{out1} + V_{out2} cause increase of $V_{gs,nbias}$. In this way the equilibrium state is achieved:

$I_{ds,pbias1} + I_{ds,pbias2} = I_{ds,nbias} + I_{ds,nload1} + I_{ds,nload2}$

And the potentials V_{out1}, V_{out2} do not increase any more.

If an input signal is amplified, voltages v_{OUT1} und v_{OUT2} change in the way that the sum v_{OUT1} + v_{OUT2} stays constant. (The result of small gains v_{out1}/v_{cm} and v_{out2}/v_{cm} (11) is, that the small signals v_{out1} und v_{out2} have opposite signs and equal absolute values) The voltage $v_{GS,NBIAS}$ and the current $i_{DS,NBIAS}$ stay constant.

Operational amplifier

We will now introduce the differential amplifier with the single ended output, i.e. an operational amplifier.

Simple operational amplifier

The simplest possibility to make an operational amplifier would be to take the fully differential amplifier from Fig 18 and use V_{out1} as output. This is shown in Fig 26.

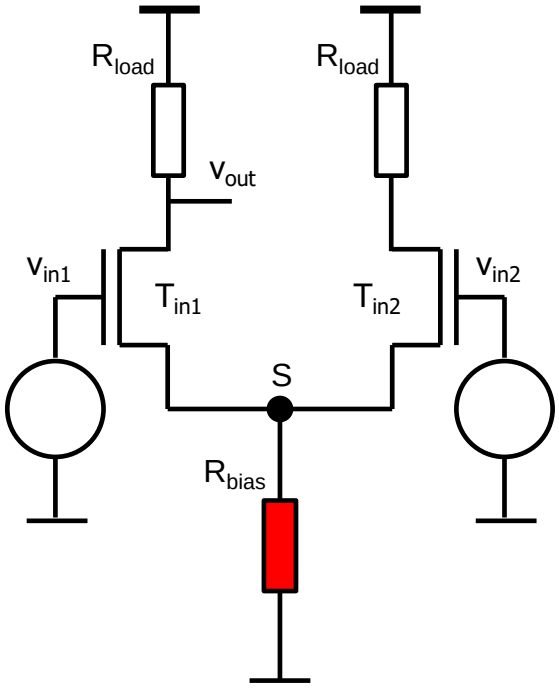


Fig 26: Simple differential amplifier with single ended output (operational amplifier)

The differential and common mode gain is: (it follows from (9) and (11)):

$$A_{diff} = \frac{V_{out1}}{v_{diff}} = -\frac{1}{2} g_m R_{load} \quad (14)$$

$$A_{cm} = \frac{V_{out1}}{v_{cm}} = -\frac{g_m R_{load}}{1+2g_m R_{bias}} \quad (15)$$

The CMRR is:

$$\mathrm{CMRR} = \frac{A_{diff}}{A_{cm}} = \frac{1+2g_m R_{bias}}{2} \quad (16)$$

CMRR (16) relatively large, however not as large as in the case of the fully differential amplifier (13). The differential gain (14) is one half of the gain of the fully differential amplifier (10).

Operational amplifier with current mirror

If we extend the circuit from Fig 26 with an active current mirror (Fig 27), we achieve similarly good properties like in the case of the fully differential amplifier. We will explain this briefly:

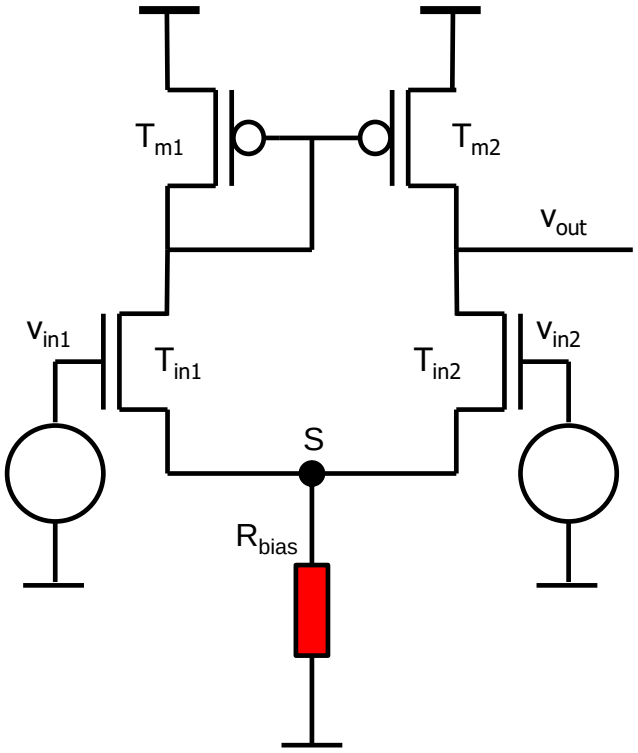


Fig 27: Operational amplifier with current mirror

The new circuit consists of a differential pair (T_{in1} and T_{in2}), a bias resistance R_{bias} or a current source and a current mirror (T_{m1} und T_{m2}).

Differential current gain

Let us now calculate the differential gain. Fig 28 shows the test circuit.

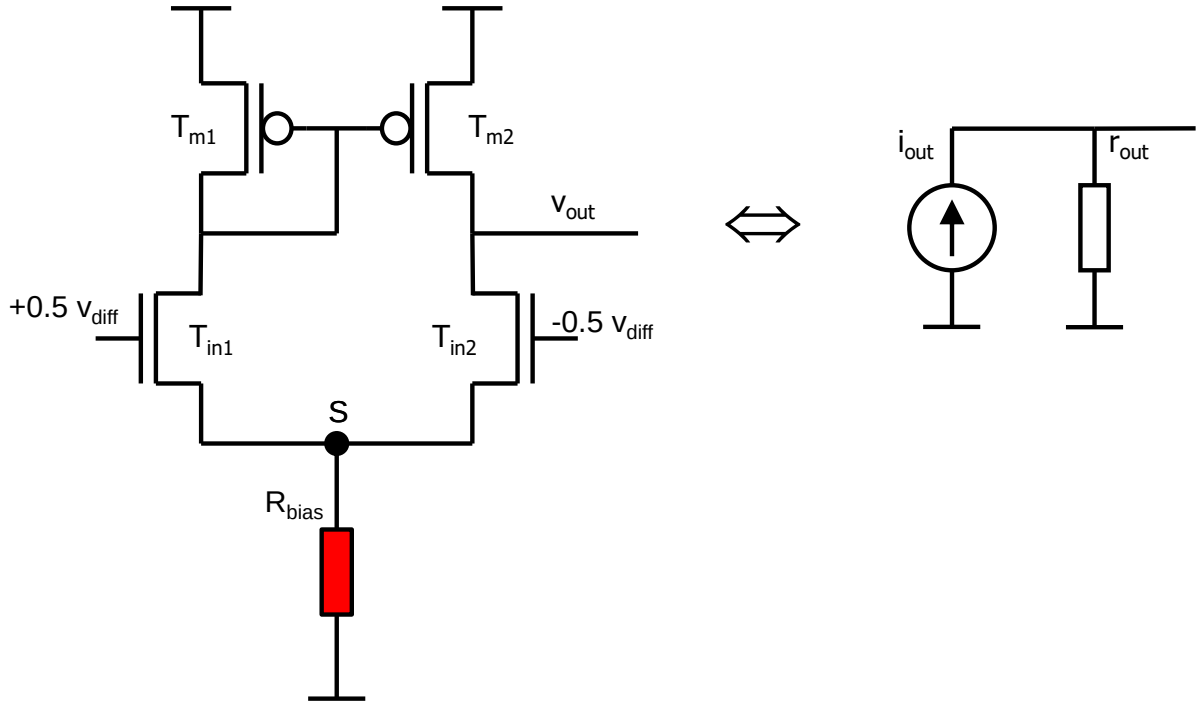


Fig 28: Small signal test circuit for the calculation of the differential gain. The amplifier can be represented as a current source.

We will proceed in the following way. We will not calculate the voltage gain directly then we will represent the differential amplifier as real current source – the Norton's current source. We will as first calculate the parameters of this current source: the short circuit current i_{out} and the internal resistance r_{out}. After this, we will calculate the voltage gain.

Let us first calculate i_{out} as function of v_{diff}. Fig 29 shows the test circuit.

If we let v_{out} open, no current can flow. Therefore we have to set v_{out} to 0 V for AC signals. This is illustrated with ground symbol in Fig 29. Only in this case the current that flows out of the circuit i^*_{out} is equal to the short circuit current of the Norton's current source i_{out}.

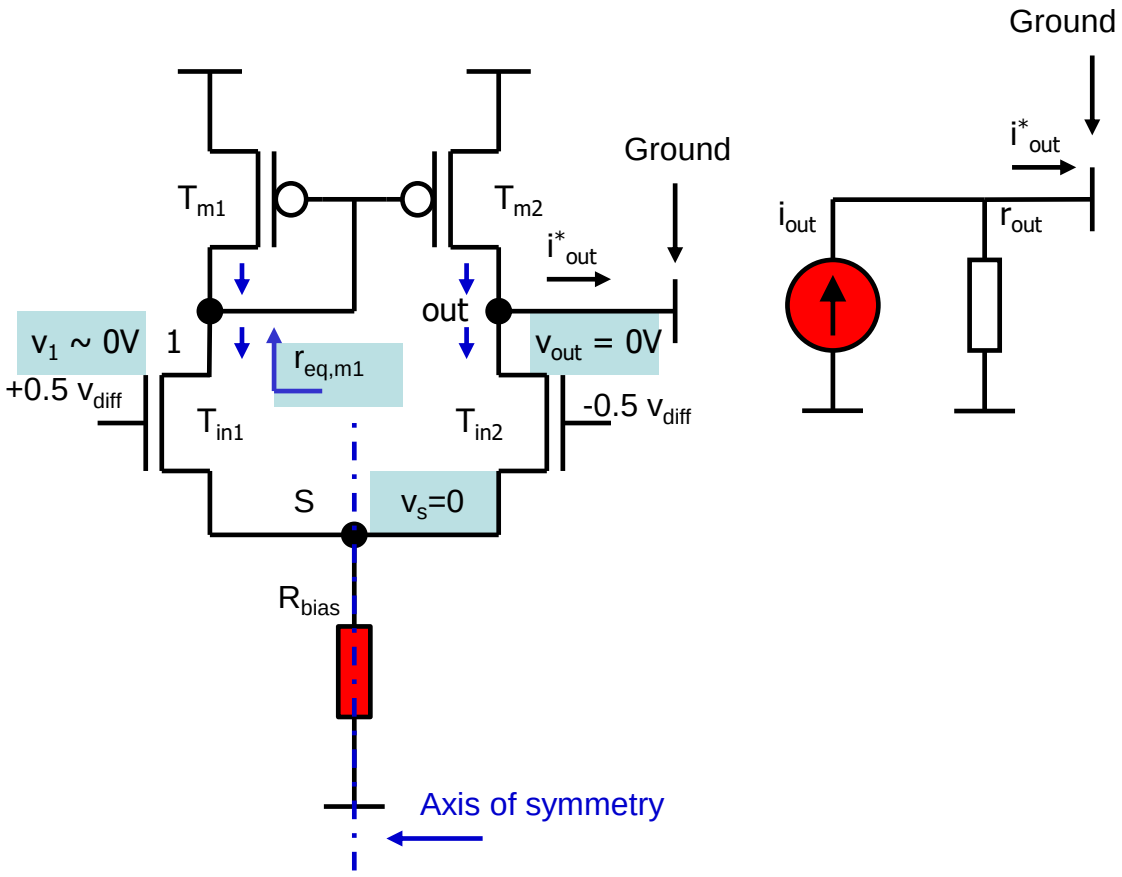


Fig 29: Small signal test circuit for the calculation of the short circuit current i_{out} as function of v_{diff}

The node out is now grounded, its potential v_{out} is equal to 0. The potential of the node 1 varies only a little, since the resistance of this node towards T_{m1} drain is small:

$$r_{eqm1} = \frac{1}{g_{m,m1}}$$

Transistor T_{in1} has a large drain resistance – a small voltage change at its drain does not influence its current. For this reason, when we can assume that the drain potential of T_{in1} is v_1 = 0 V. Since it is also v_{out} = 0, the both transistors T_{in1} and T_{in2} hate equal drain voltages. The lower half of the circuit is symmetrical (Fig 29) and the small signal voltages at the gates of T_{in1} and T_{in2} have equal absolute values and different signs. Therefore it holds for the voltage at the symmetry axis: v_s = 0. The currents are given by the following equations:

$$i_{ds,in1} = g_m v_{gs,in1} = g_m \frac{v_{diff}}{2} \qquad (10b)$$

$$i_{ds,in2} = g_m v_{gs,in2} = -g_m \frac{v_{diff}}{2} \qquad (10c)$$

Symbol g_m is the transconductance of T_{in1} und T_{in2}.

The current mirror copies the current: $i_{ds,m1} = i_{ds,in1}$.

The output current is:

$$i^*_{out} = i_{ds,m2} - i_{ds,in2} = i_{ds,in1} - i_{ds,in2} \qquad (10d)$$

When we substitute (10b) and (10c) in (10d), we obtain:

$$i^*_{out} = g_m \, v_{diff}$$

The short circuit current of the Norton's current source is:

$$i_{out} = i^*_{out} = g_m \, v_{diff} \qquad (17)$$

We define the differential current gain as follows:

$$G_{diff} = \frac{i_{out}}{v_{diff}} \qquad (17b)$$

with

$$G_{diff} = g_m \qquad (17c)$$

Common mode current gain

Fig 30 shows the test circuit for the calculation of i_{out} as function of v_{cm}.

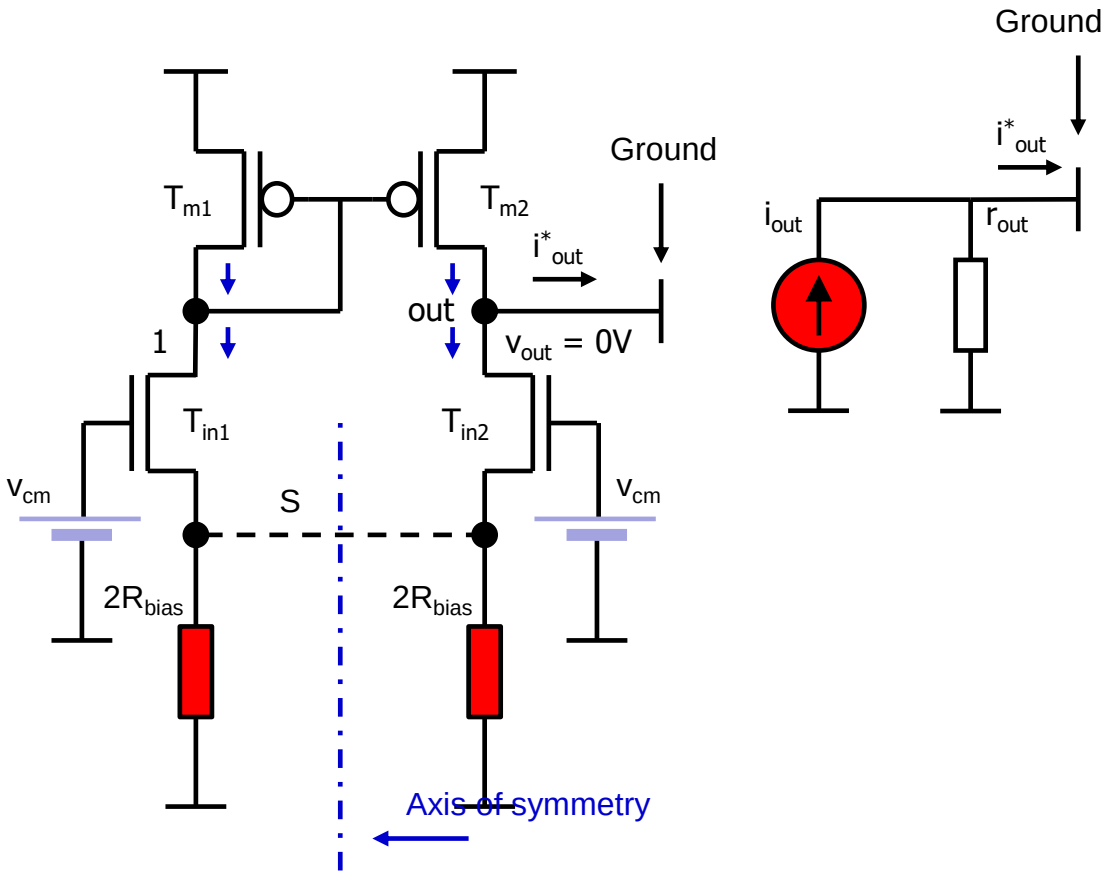


Fig 30: Small signal test circuit for the calculation of the short circuit current i_{out} as function of v_{cm}

Due to symmetry, the currents $i_{ds,in1}$ and $i_{ds,in2}$ are nearly equal. Because of (10d), it holds:

$$i^*_{out} = i_{out} = i_{ds,m2} - i_{ds,in2} \sim 0$$

The common mode current gain is:

$$G_{cm} = \frac{i_{out}}{v_{cm}} \sim 0 \qquad (17b)$$

Output resistance

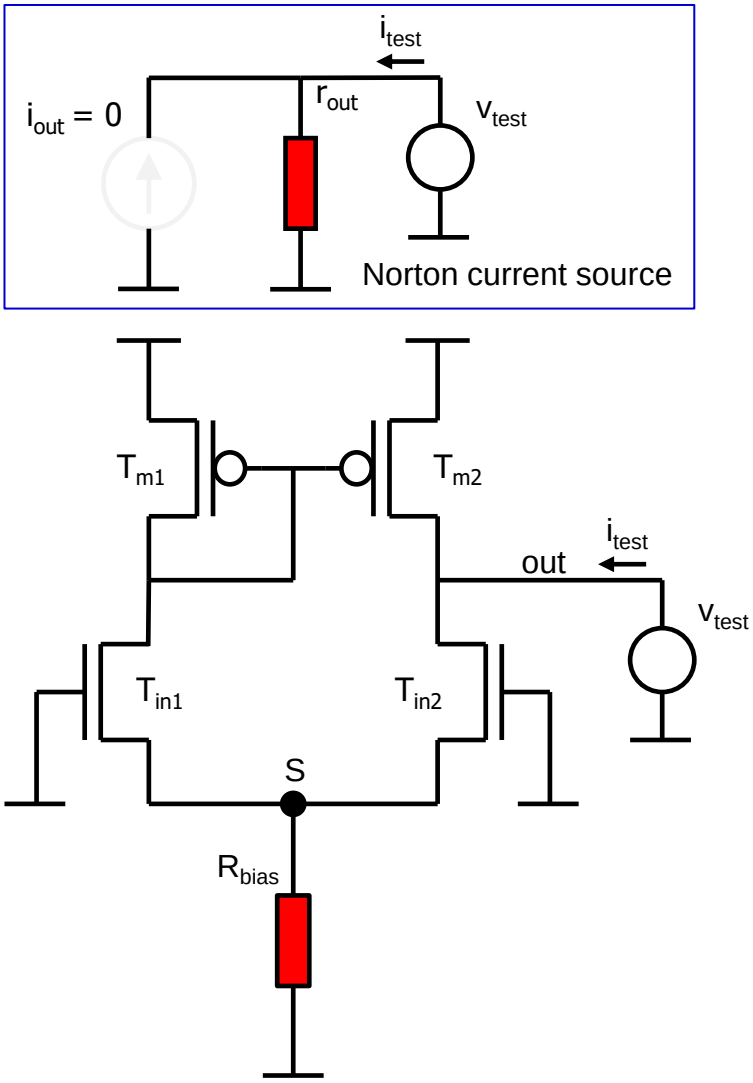


Fig 31: Small signal test circuit for the calculation of output resistance

Let us now calculate the output resistance. Fig 31 shows the test circuit. The voltage sources at the inputs of the amplifier are off ($i_{out} = 0$). The output resistance is calculated by assuming a test voltage source:

$$r_{out} = \frac{v_{test}}{i_{test}} \quad (18)$$

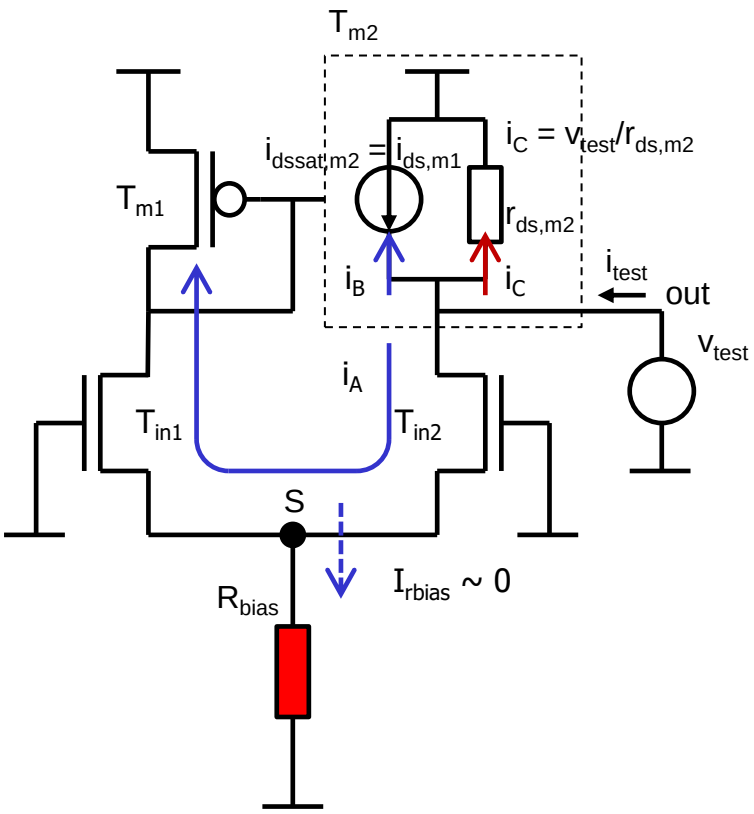


Fig 32: Small signal test circuit for the calculation of output resistance, T_{m2} is replaced with its small signal model

Fig 32 shows a more detailed schematics, where transistor T_{m2} is replaced by its small signal model. The transistor model consists of the current source $i_{dsssat,m2} = g_{m,m2}\, v_{gs,m2}$ and the resistance $r_{ds,m2}$. Since T_{m1} and T_{m2} make a current mirror, it holds:

$$i_{dssat,m2} \sim i_{ds,m1} \qquad (19)$$

The current i_{test} gets split into three currents $i_A = i_{ds,in2}$, $i_B = -\, i_{ds,m1}$ and i_C (Fig 32).

$$i_{test} = i_A + i_B + i_C \qquad (19b)$$

Let us as first calculate i_A. Transistor T_{in2} sees the following resistance at its source:

$$r_s = \frac{1}{g_{m,in1}} || R_{bias} \sim \frac{1}{g_{m,in1}} \qquad (20)$$

The circuit can be further simplified as is Fig 33.

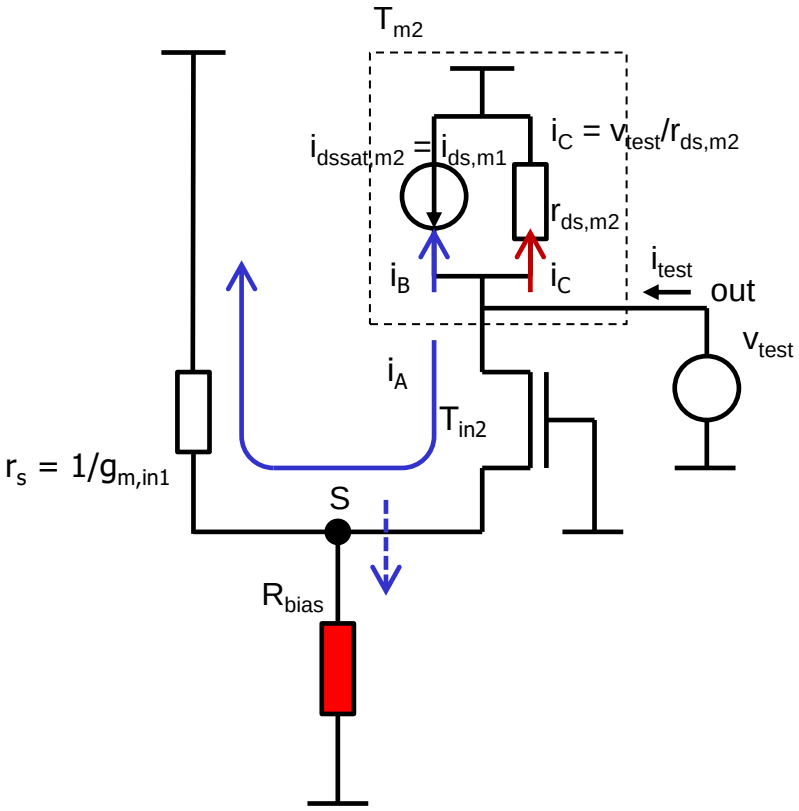


Fig 33: Simplified test circuit for the calculation of the output resistance

T_{in2} and r_s make the same circuit as V-I converter as in Fig 15. The output resistance of the V-I converter is given by (4). The resistance at the drain of T_{in2} is:

$$r_d = (1 + g_{m,in2}\, r_s) r_{ds,in2} = 2r_{ds,in2} \qquad (21)$$

We assumed $g_{min1} = g_{min2} = g_m$. The current i_A is:

$$i_A = \frac{v_{test}}{2r_{ds,in2}} \qquad (22)$$

Notice that the current i_A splits in the node S into current through T_{in1} (r_s) and the current through R_{bias}. Since $R_{bias} >> r_s$, we can neglect the current through R_{bias}.

The current i_A is copied by the current mirror. It holds:

$$i_B \sim i_A \qquad (23)$$

The current i_C is:

$$i_C = \frac{v_{test}}{r_{ds,m2}} \qquad (24)$$

We obtain the total current when we substitute (24), (22) and (23) in (19b):

$$i_{test} = \frac{v_{test}}{r_{ds,in2}} + \frac{v_{test}}{r_{ds,m2}} \quad (26)$$

The output resistance (i.e. the internal resistance of the Norton's current source) is (Fig 34):

$$r_{out} = \frac{v_{test}}{i_{test}} = \frac{1}{\left(\frac{1}{r_{ds,in2}} + \frac{1}{r_{ds,m2}}\right)} = r_{ds,in2} \,||\, r_{ds,m2} \quad (27)$$

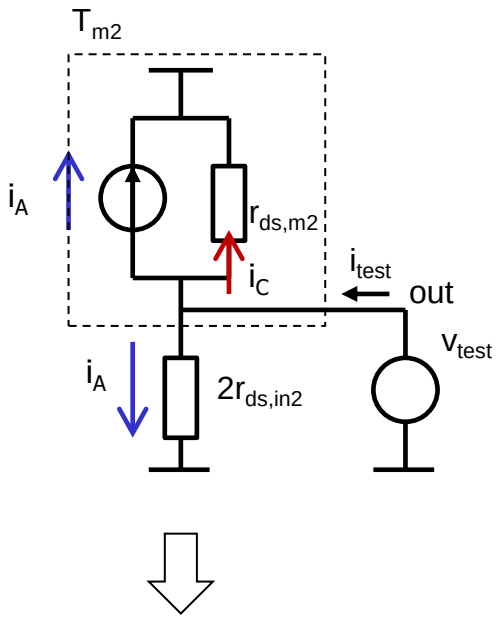


Fig 34: Simplified test circuit for the calculation of the output resistance

When we leave the output of the Norton current source open, the following voltage is generated:

$v_{out} = i_{out}\, r_{out}$. The differential voltage gain is:

$$A_{diff} = \frac{v_{out}}{v_{diff}} = r_{out}\frac{i_{out}}{v_{diff}} = r_{out} G_{diff} \quad (28)$$

Because of (17c) it holds

$$A_{diff} = g_m\, r_{out} \quad (29)$$

Because of (17b) we obtain

$$A_{cm} \sim 0 \quad (30)$$

It holds:

$$CMRR = \frac{A_{diff}}{A_{cm}} \sim \infty \quad (31)$$

The differential amplifier with current mirror has a good CMRR. It is much better that the CMRR of the simple operational amplifier (16). Also the voltage gain (29) is assuming the same r_{out} better than (14).

The operational amplifier with current mirror is often used. It has the same voltage gain as the common source single ended amplifier. The operational amplifier is more flexible in applications since either positive or negative gain can be achieved by swapping the input pins and since the input pines are disconnected from the output. The small signal models of the operational amplifier with current mirror are shown in Fig 35. We assumed $A_{cm} = 0$ – the output current (and voltage) depend only on the difference between input voltages.

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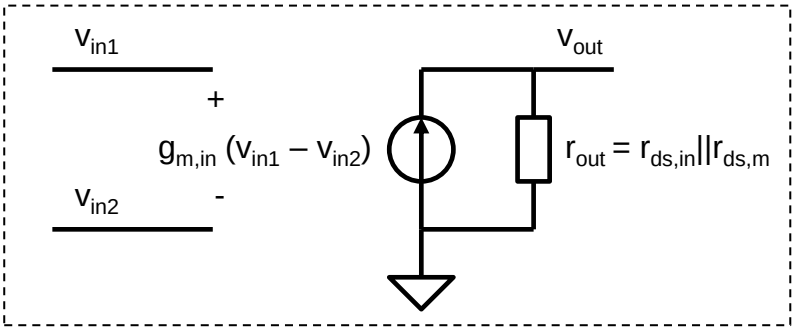
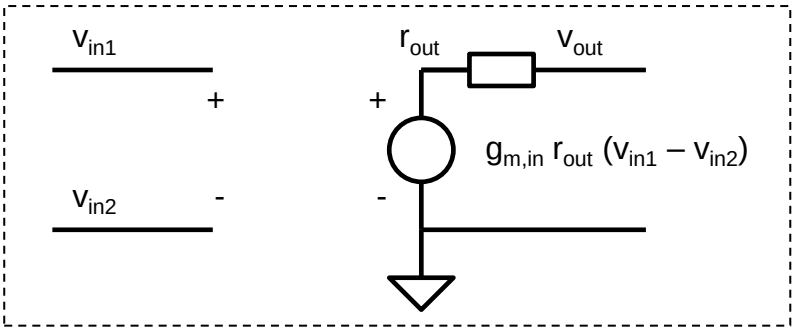


Small signal model as current source



Small signal model as voltage source

Fig 35: Small signal model of the operational amplifier