Lecture 8

Cascode and common source amplifier

The themes of this lecture are cascode and common source amplifier.

Cascode

Cascode is a circuit consisting of a MOSFET (the cascode transistor T_{casc}) having a constant voltage at its gate and an input current source I_{in} connected to the source of T_{casc}, as shown in Fig 1.

The word *cascode* is abbreviation from "cascaded anode". The anode is the positive electrode of the electron tube, which plays similar role as drain of a MOSFET. We will normally refer to the entire circuits made of the current source and the transistor T_{casc} as the cascode. However, sometimes we will call T_{casc} alone the cascode. For instance we may say that Fig 1 shows a current source with a cascode.

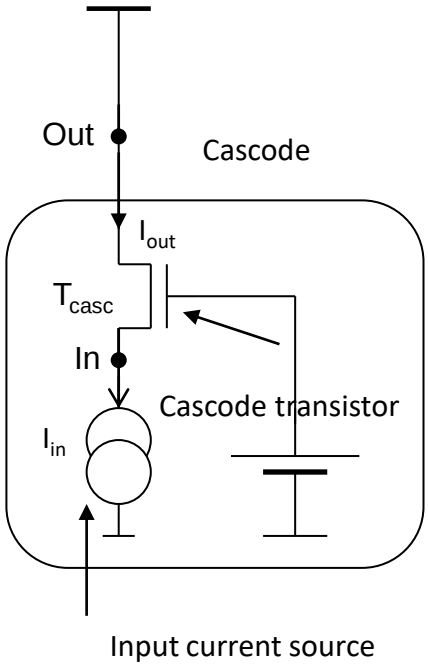


Fig 1: Cascode

The cascode transistor works like an impedance converter. It conducts the input current (the signal current) ($I_{out} = I_{in}$).

The AC resistance of the source of T_{casc}, that we also call the input resistance (r_{in}) of the cascode, is small. The resistance at the drain of T_{casc} (the output resistance r_{out}) is large.

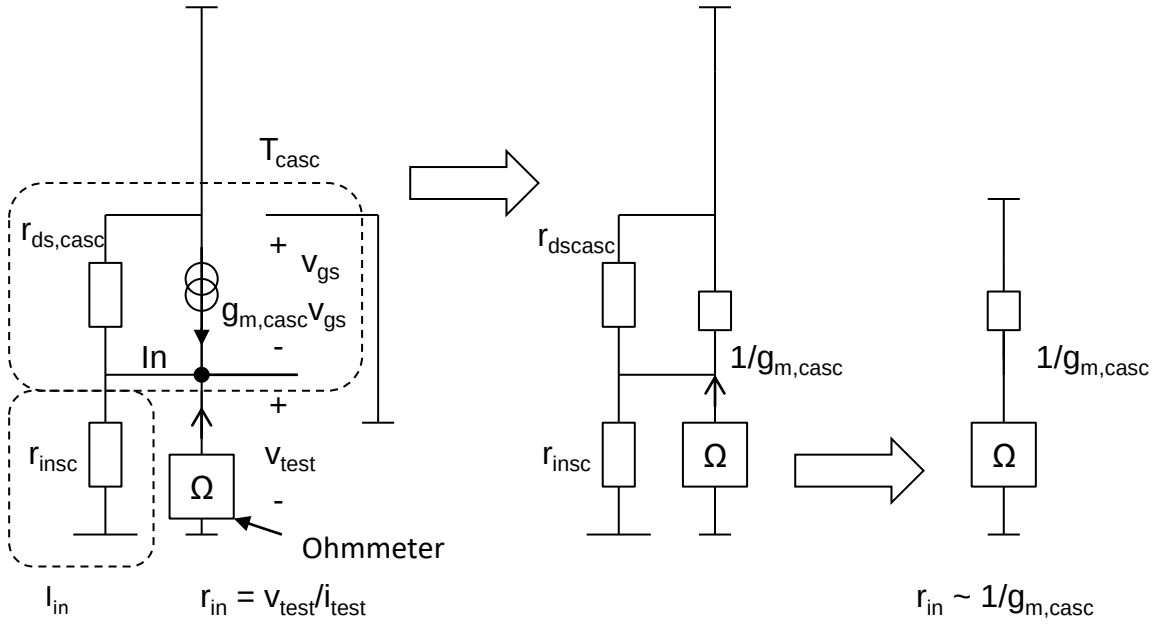


Fig 2: Input resistance of the cascode transistor

Input resistance of the cascode transistor

Fig 2 shows a test circuit for the calculation of r_{in}.

Let us beforehand write the result:

$R_{in} \sim 1/g_{m,casc}$, where $g_{m,casc}$ is the transconductance of the transistor T_{casc}.

In order to calculate this, let us imagine an ohmmeter connected to the source of T_{casc} (node In) that generates a small voltage v_{test} and measures the current i_{test}. Voltage v_{test} generates the following gate source voltage for T_{casc}:

$v_{gs} = - v_{test}$.

For this reason T_{casc} (the current source of its model) conducts the current $i = g_{m,casc} \times v_{test}$.

This corresponds to the resistance:

$v_{test}/i_{test} = 1/g_{m,casc}$ (1)

The ohmmeter "sees" also the parallel connection of $r_{ds,casc}$ (r_{ds} of T_{casc}) and the (r_{insc}), however these resistances are larger than $1/g_{m,casc}$ and they can be neglected.

$1/g_{m,casc}$ is relatively small (*relatively* means of the order of 1 kΩ or smaller). This means that the voltage change at the source of T_{casc} is relatively small (relatively in comparison with the voltage change at the drain of T_{casc})..

Output resistance of the cascode transistor

How large is the AC resistance r_{out} at the drain of the T_{casc} (at the node Out)?

Let us also here write the result beforehand:

R_{out} is much larger than both $r_{ds,casc}$ and r_{insc}.

R_{insc} is the small signal resistance of the current source.

Exact derivation yields to the result:

$$r_{out} = g_{m,casc}\, r_{ds,casc}\, r_{insc} \quad (2)$$

The test circuit with an ohmmeter is shown in Fig 3.

The increase in resistance is the result of the negative feedback. This can be explained as follows.

Circuit B in Fig 3 is obtained from circuit A when T_{casc} is replaced with the small signal model. In circuit B we can easier recognise a feedback. When the ohmmeter is "switched on" and a voltage v_{test} is generated, a current i_{test0} first flows through $r_{ds,casc}$ and r_{insc}. This increases the potential of the v_S. Thus, a negative v_{gs} is created and the current source in the transistor generates an AC current i_{ds} that flow against the direction of the original current. The Ohmmeter measures a smaller current and therefore a larger resistance.

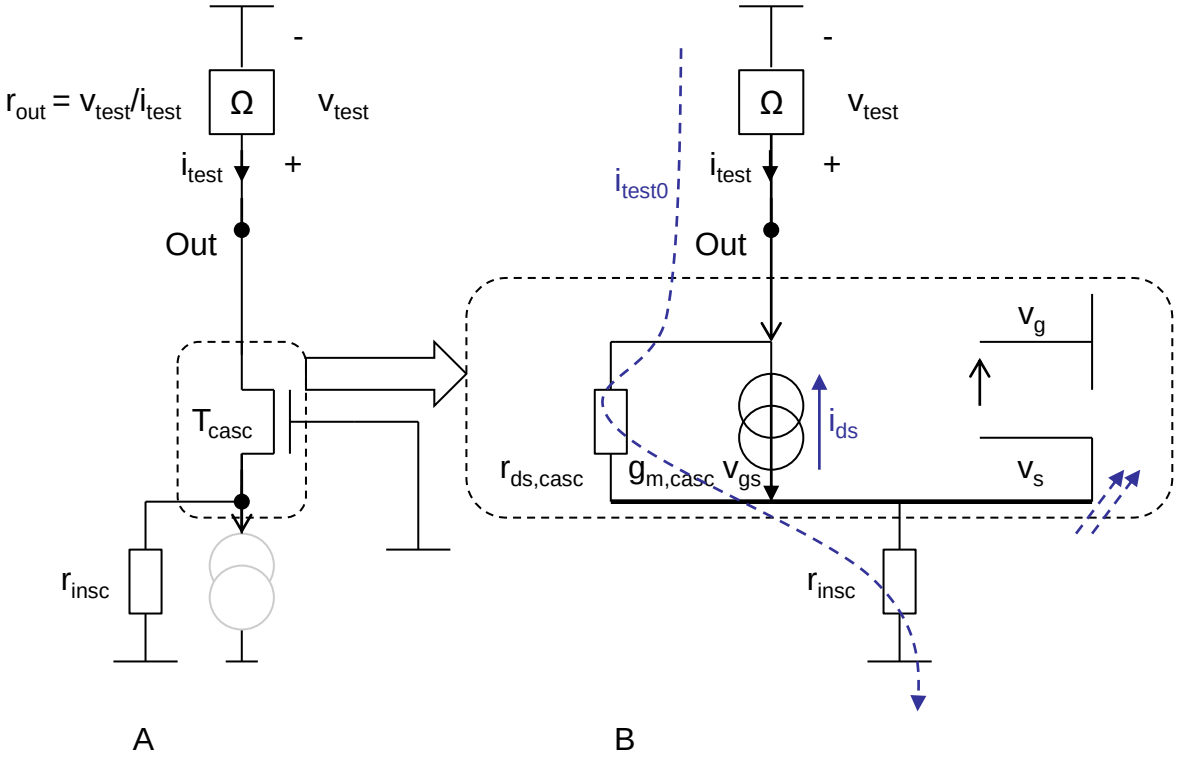


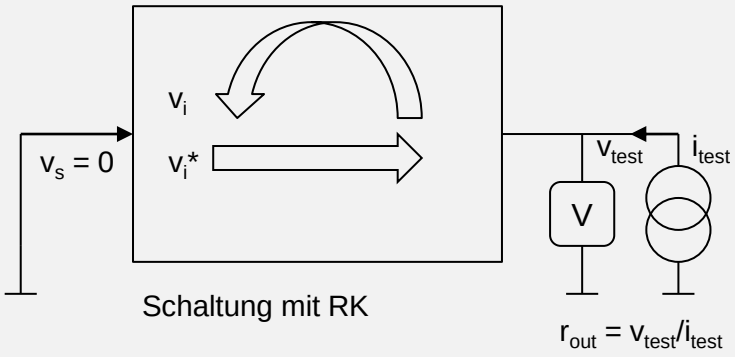
Fig 3: Test circuit for calculation of output resistance of T_{casc}

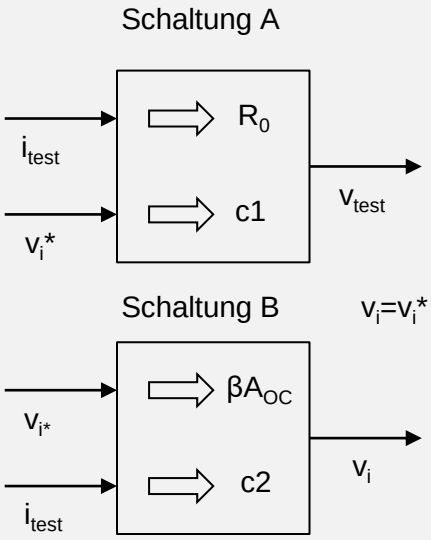
Let us now calculate r_{out} precisely.

As we explained, the feedback influences the resistance.

Blackman's formula

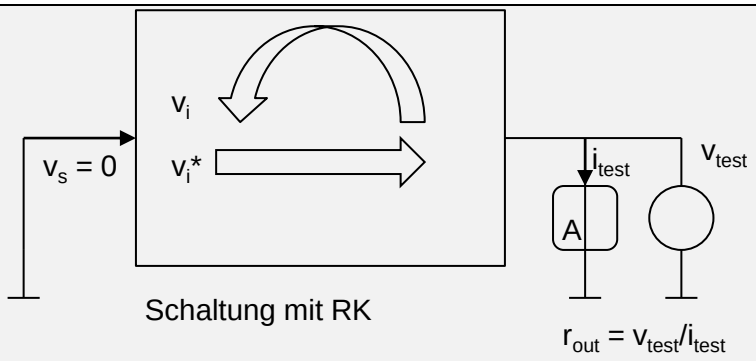
Fig 4 and Fig 5 show two test circuits for the calculation of the output resistance of the circuit with feedback R_{FB}. The first circuit uses one voltage source v_{test}. Current i_{test} is measured (calculated) in order to calculate R_{FB}. The second circuit uses a current source i_{test} while the voltage is measured. In both cases it is $R_{FB} = v_{test} / i_{test.}$ Both circuits must lead to the same R_{FB} result. When the original circuit is split into circuits A and B and when the condition $v_i = v_i^*$ is taken into account, formulas A1 and A2 can be derived (Fig 4 and Fig 5). From (A1) and (A2) follows the formula A3 (Fig 5), known as Blackman's formula.



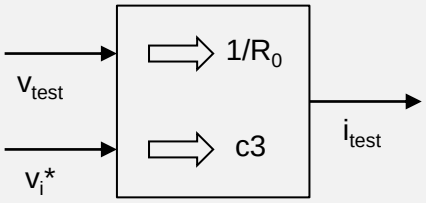


$$v_i = v_i^* \Rightarrow R_{FB} \equiv \frac{v_{test}}{i_{test}} = R_0 \frac{f}{1-\beta A_{OC}} \quad (A1)$$

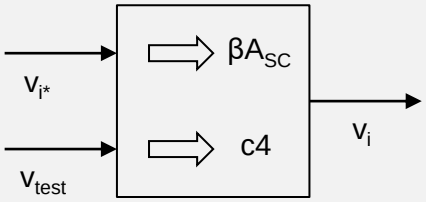
Fig 4: First test circuit for the derivation of R_{FB}. The resistance is "measured" with a current source



Schaltung A



Schaltung B



$$v_i = v_i^* \Rightarrow R_{FB} \equiv \frac{v_{test}}{i_{test}} = R_0 \frac{1-\beta A_{SC}}{g} \quad (A2)$$

$$(A1), (A2) \Rightarrow R_{FB} \equiv \frac{v_{test}}{i_{test}} = R_0 \frac{1-\beta A_{SC}}{1-\beta A_{OC}} \quad (A3)$$

Fig 5: First test circuit for the derivation of R_{FB}. The resistance is "measured" with a voltage source

The resistance in a circuit with feedback can be calculated using the Blackman's formula that was introduced in lecture 6:

$$r_{outFB} = r_{out0} \frac{1-\beta A_{SC}}{1-\beta A_{OC}} \qquad (4)$$

r_{out0} is the resistance that we had if we switched off the feedback. (By setting the input voltage of the amplifier to 0.)

βA_{SC} is the loop gain, calculated from a test circuit where the nodes are short circuited, the ohmmeter was placed between.

βA_{OC} is the loop gain, calculated from a test circuit where the nodes are opened, the ohmmeter was placed between.

The test circuit is show in Fig 6. The feedback is cut.

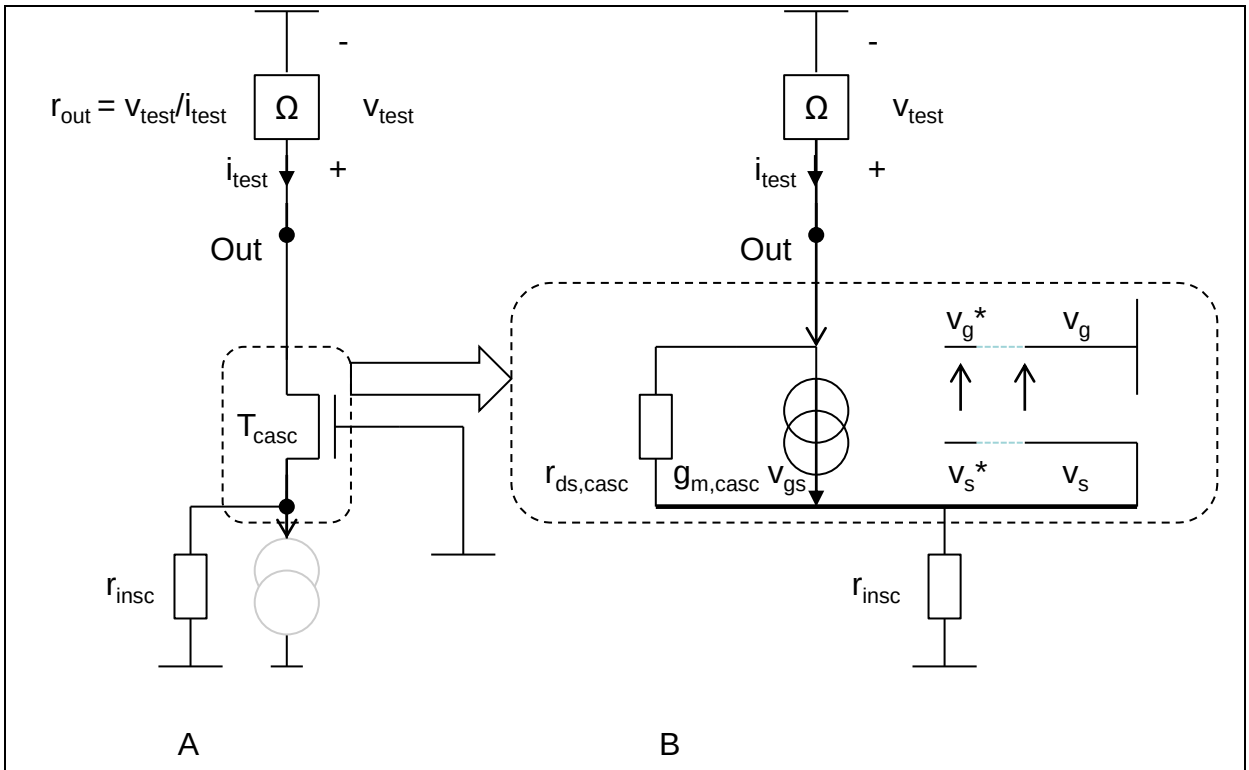


Fig 6: Test circuit for calculation of output resistance of T_{casc}

Let us calculate as first the resistance without feedback r_{out0}.

Fig 7 shows the test circuit.

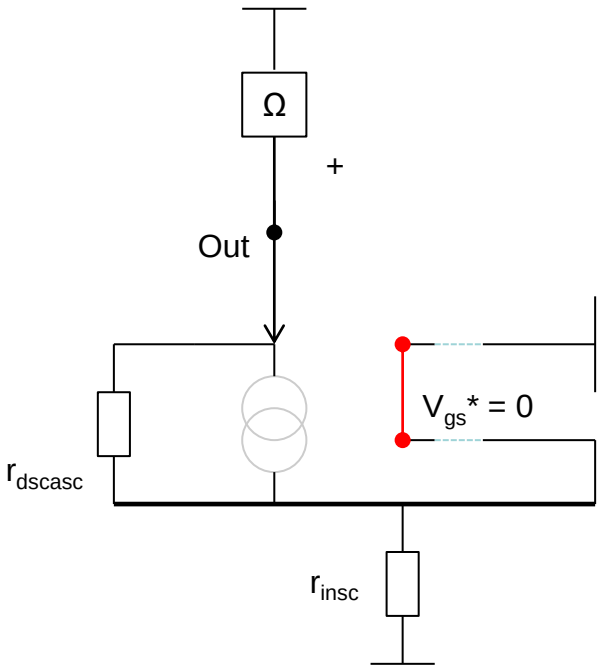


Fig 7: Test circuit for calculation of r_{out0}

The feedback is switched off by shorting v_g* and v_s*. In this way the current source in the transistor model is switched off. The ohmmeter sees only the series of $r_{ds,casc}$ und r_{sig}:

$r_{out0} = r_{ds,casc} + r_{sig}$

Fig 8 shows the test circuit for βA_{OC}. The line where the ohmmeter was connected is now open. A_{OC} is defined as follows:

$\beta A_{OC} = (v_g - v_s)/v_{test}$

Note that the current flowing into the encircled network (i_{in}) is zero. Therefore, the current flowing from the network to the resistance must also be zero ($_{iout}$). Therefore: $v_s = 0$. Since v_g is also zero, it holds $v_g - v_s = 0$ and

$\beta A_{OC} = 0$.

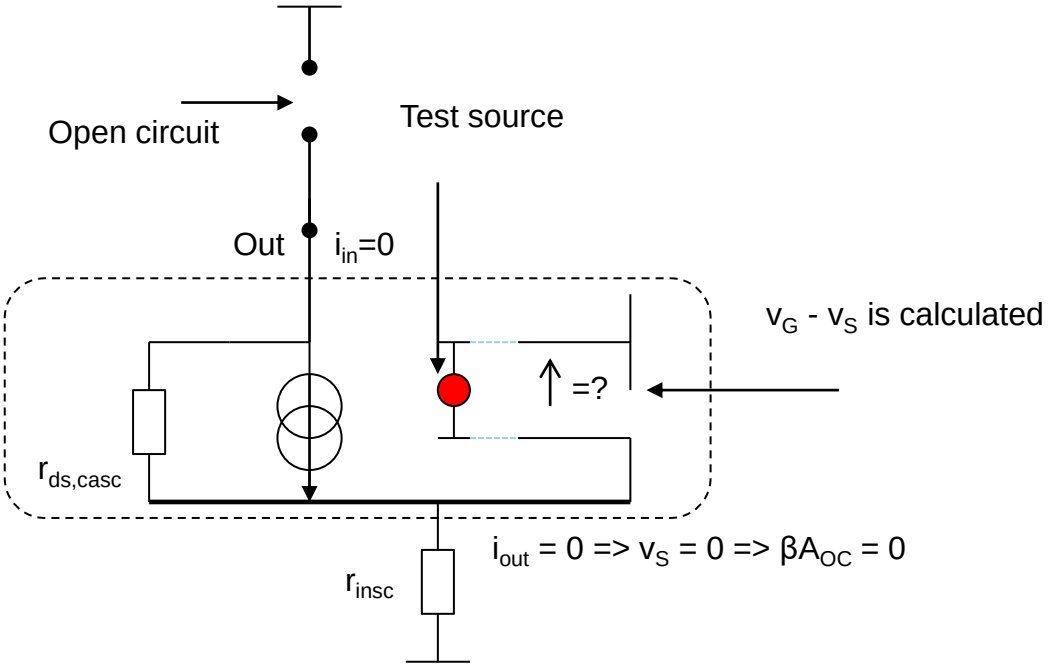


Fig 8: Test circuit for calculation of βA_{OC}

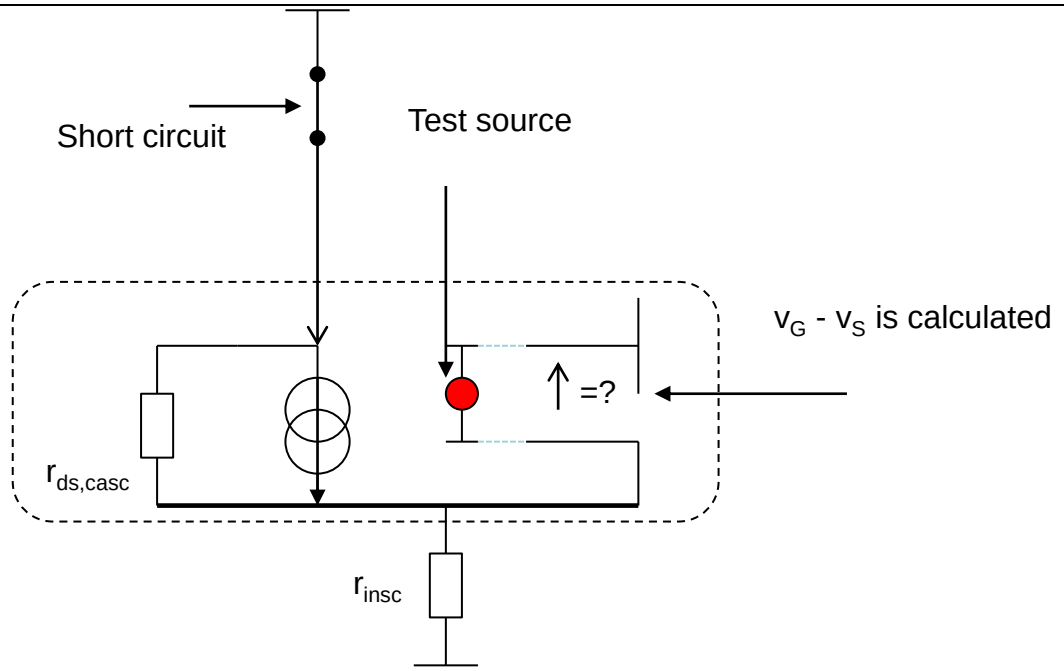


Fig 9: Test circuit for calculation of βA_{SC}

Fig 9 shows the test circuit for the calculation of βA_{SC}. It can be easily derived:

$$\beta A_{SC} = -\frac{r_{insc}\, r_{ds,casc}}{r_{insc} + r_{ds,casc}} g_{m,casc}$$

When we substitute the results for r_{out0}, βA_{OC} and βA_{OC} in the Blackman's formula (4), we obtain:

$$r_{out} = (r_{insc} + r_{ds,casc})\left(1 + \frac{r_{insc}\, r_{ds,casc}}{r_{insc}+r_{ds,casc}}\, g_{m,casc}\right) \sim r_{insc}\, r_{ds,casc}\, g_{m,casc} \gg r_{insc} \quad (5)$$

The product $g_m\, r_{ds}$ is in the case of the circuit from the exercises ~ 40.

The cascode transistor has a similar function like a current mirror connect to a signal source: there is a current input, a current output, r_{in} is small, r_{out} is large.

The main difference is that a cascode transistor change the current direction and a current mirror does not change, as shown in Fig 10.

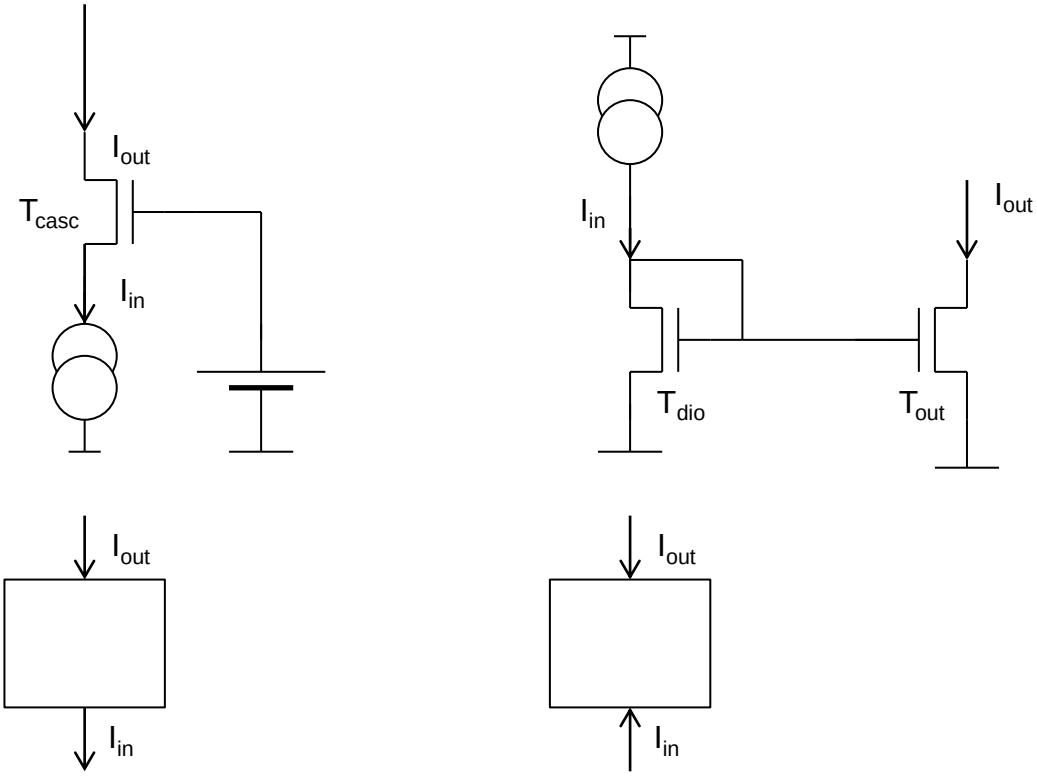


Fig 10: Cascode transistor vs current mirror

Common source amplifier

We will discuss one of the most important basic circuit: the common source voltage amplifier.

The name indicates that the source of the input transistor is connected to a constant voltage or ground in the small signal model.

The easiest way to design a common source amplifier is to attach a load resistor R_{load} to an input transistor T_{in} working as a current source, as shown in Fig 11. The resistance fulfils two tasks: first to bias the input transistor T_{in} and to create a proper DC work point, second to convert the output current into a voltage.

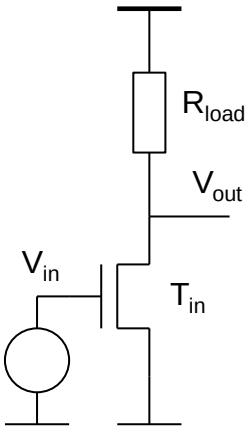


Fig 11: Common source amplifier

As we shown in lecture 5, we can perform the DC analysis graphically (using U-I characteristics).

On the same plot we draw the I_{ds} - V_{ds} characteristic of the transistor and the corresponding characteristic of the resistor, as shown in Fig 12. We determine the output voltage as the intersection point of the transistor and the resistor characteristics. If the input voltage increases, the transistor characteristics move upwards and the output voltage moves from the positive supply VDD to the left.

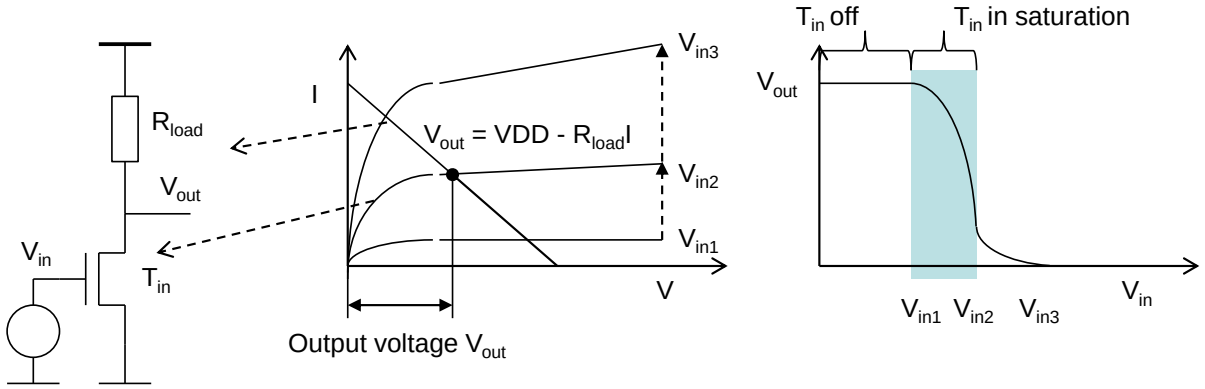


Fig 12: Graphical DC analysis

For the working region where T_{in} is in saturation (condition $V_{out} > V_{dssat} = V_{in} - V_{th}$), we can derive the small signal model. The voltage gain can be calculated from the small signal circuit shown in Fig 13:

$$A = \frac{v_{out}}{v_{in}} = -g_m(r_{ds}||R_{load}) \equiv -g_m r_{out} \quad (6)$$

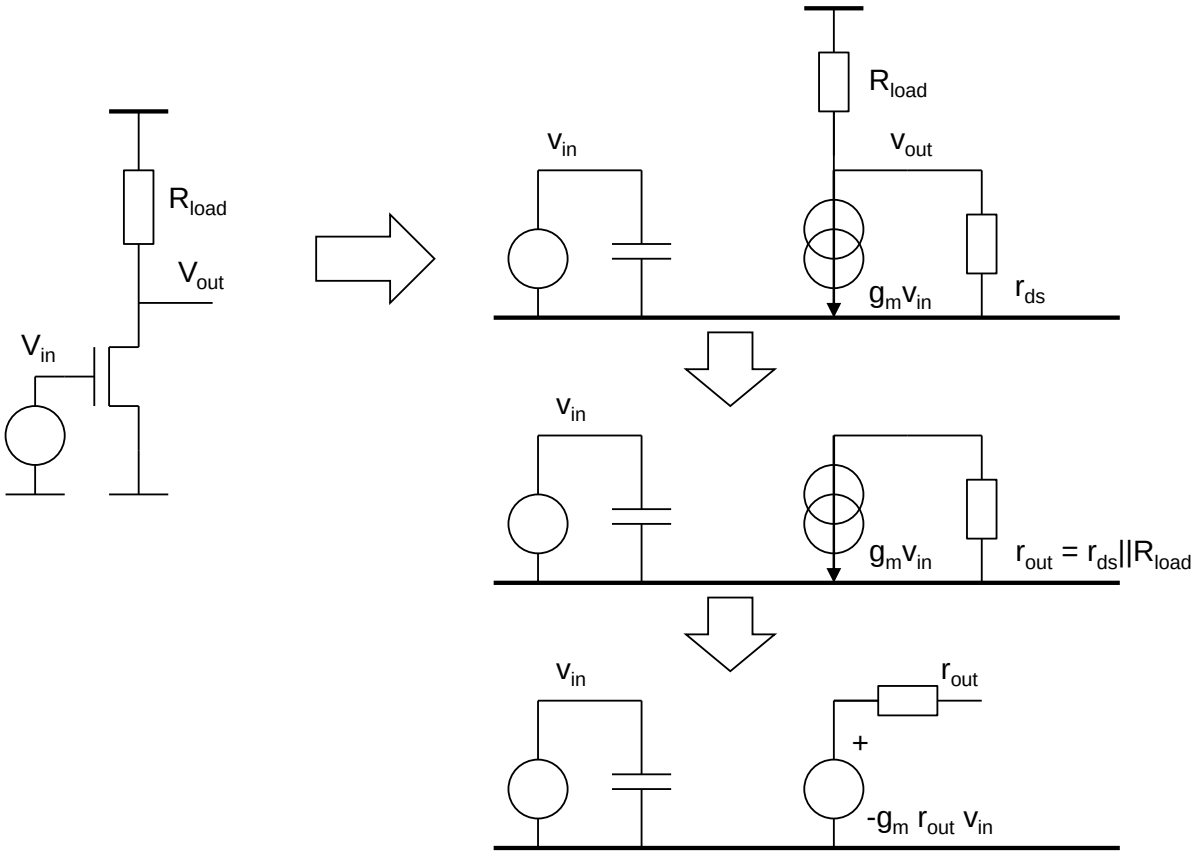


Fig 13: Common source amplifier – small signal circuit

Common source amplifier with active load

Motivation

In order to maximize the voltage gain we need large values for g_m and r_{out}.

Resistance $r_{out} > 50\ k\Omega$ is considered to be large. A transconductance $g_m > 1\ mS$ is also considered as large.

The disadvantage of the amplifier with a linear resistance is that it is not possible to maximize both g_m and R_{load}. If the resistance R_{load} is large, its characteristic is close to the x-axis. The transistor current is small. A small current leads to a small transconductance. This is illustrated in Fig 14.

If the resistance R_{load} is small, the transistor current is higher, as well as the transconductance. However, because of the small R_{load}, the amplification is small.

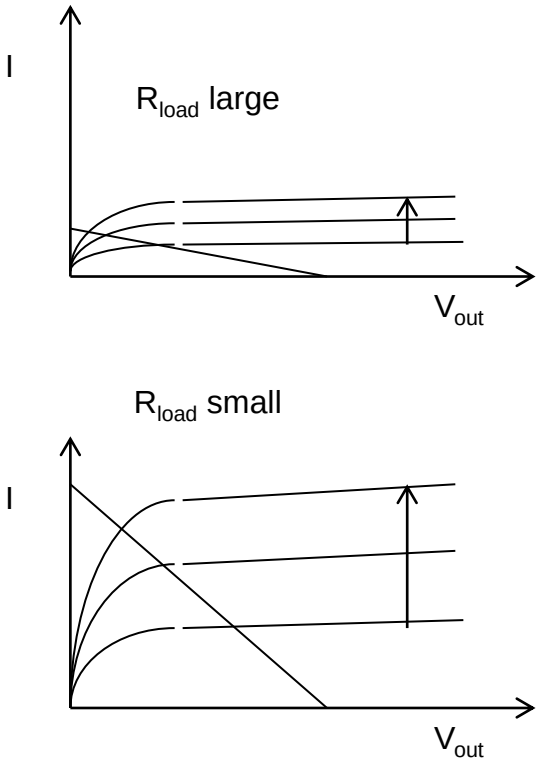


Fig 14: I-V characteristics for small and large R_{load}

A characteristic that rises relatively quickly and then moves horizontally across a large V_{out} region (as shown in Fig 15) would be better than the characteristics of a linear resistor.

A PMOS transistor (a PMOS current source) with source connected to VDD (positive voltage supply) and with a constant gate potential has almost ideal characteristics, as shown in Fig 16.

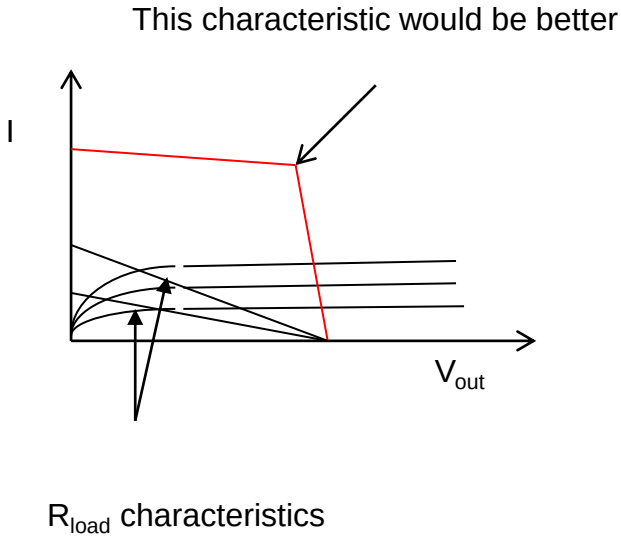


Fig 15: I-V characteristics of the ideal load element

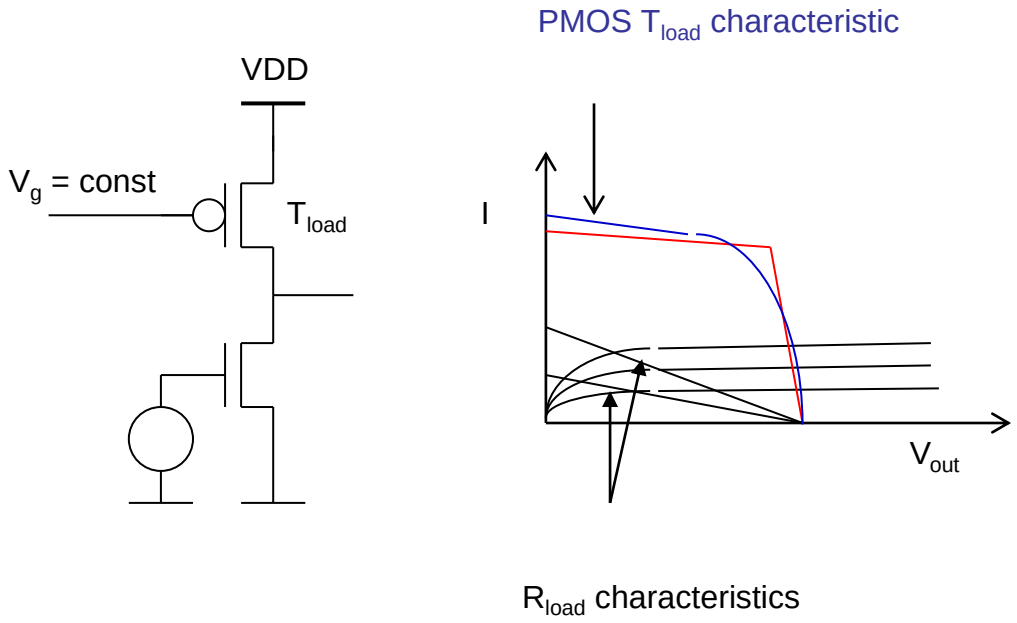


Fig 16: I-V characteristics of the ideal load element and PMOS current source characteristics

Therefore we can improve the voltage amplifier by replacing the resistance R_{load} with a PMOS current source, as shown in Fig 17. The figure also shows the bias circuit for the current source in the form of a MOSFET diode T_{dio} and a reference current source I_{bias}. The reference current can be implemented in different ways, the simplest is using a resistor R_{bias}. We refer to the load element implemented with a transistor as the *active load*. We call the circuit from Fig 17 the common source amplifier with active load.

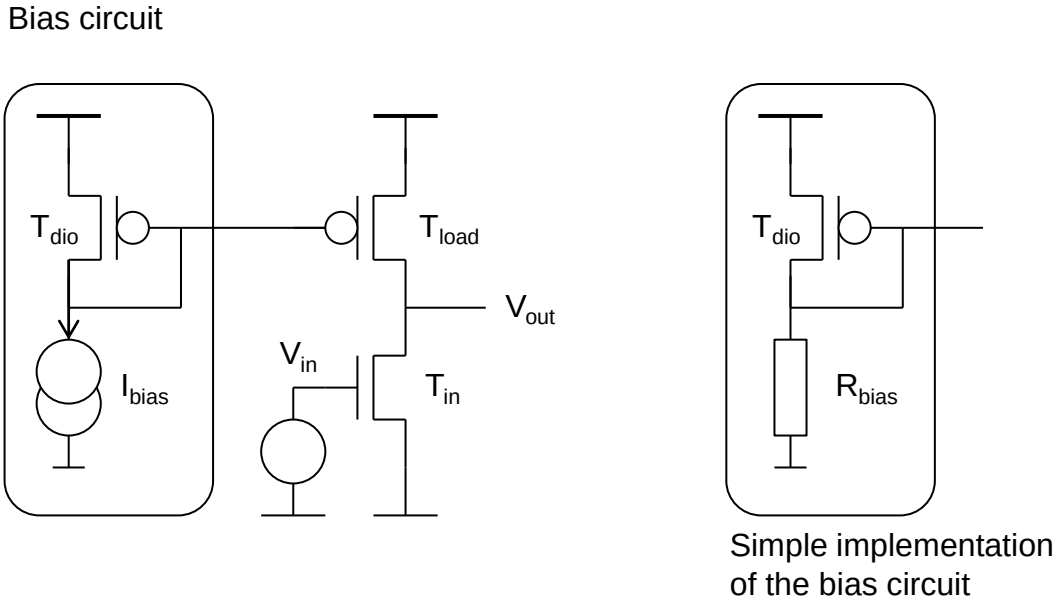


Fig 17: Common source amplifier with active load

From the characteristics of T_{in} and T_{load} we can graphically derive a V_{out} =f(V_{in}) characteristic (Fig 18). The amplification is high only in the region where both transistors T_{in} and T_{out} are in

saturation. We see that DC current is relatively high in this area, so we can expect a high transconductance.

The condition for saturation of T_{in} is $V_{out} > V_{in} - V_{th}$. The condition for saturation for T_{load} is $V_{out} < VDD - V_{dssat,load}$ where $|V_{dssat}| = |V_{gs}| - |V_{th}|$.

The region where both transistors are in saturation is marked with grey in Fig 18 (bottom figure).

We see from the upper graph in Fig 18 that the DC current is large in the region with large gain. We can therefore expect a large transconductance g_m.

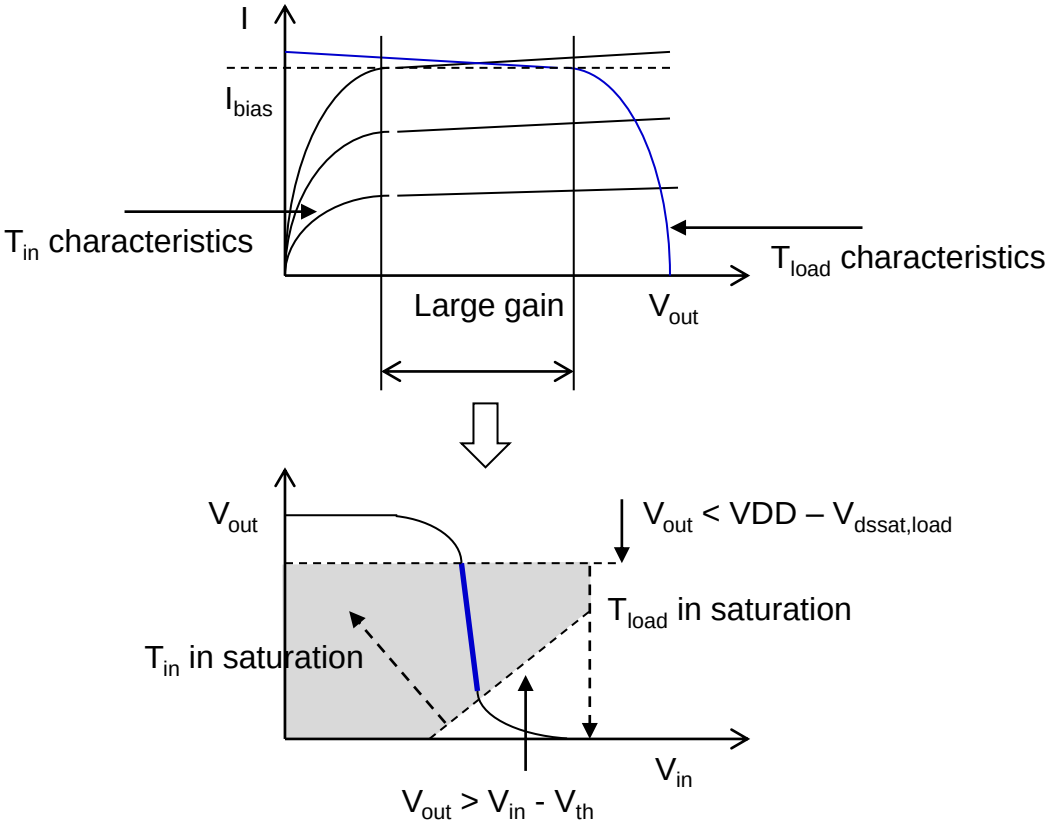


Fig 18: Input-output characteristic of the voltage amplifier with active load

The small signal model of the circuit, when both transistors are in saturation is shown in Fig 19.

The voltage amplification is:

$$A = -g_{m,in}(r_{ds,in} || r_{ds,load}) \equiv -g_{m,in} r_{out}$$

$G_{m,in}$ and $r_{ds,in}$ are the transconductance and the drain-source resistance of the input transistor Tin. $r_{ds,load}$ is the drain-source resistance of the load transistor T_{load}.

An amplifier is a two port circuit. This circuit can be described with its amplification and the input and the output impedances. The input impedance of the amplifier arises from the gate source capacitance of T_{in}. The output resistance is:

:

$$r_{out} = r_{ds,in} || r_{ds,load}$$

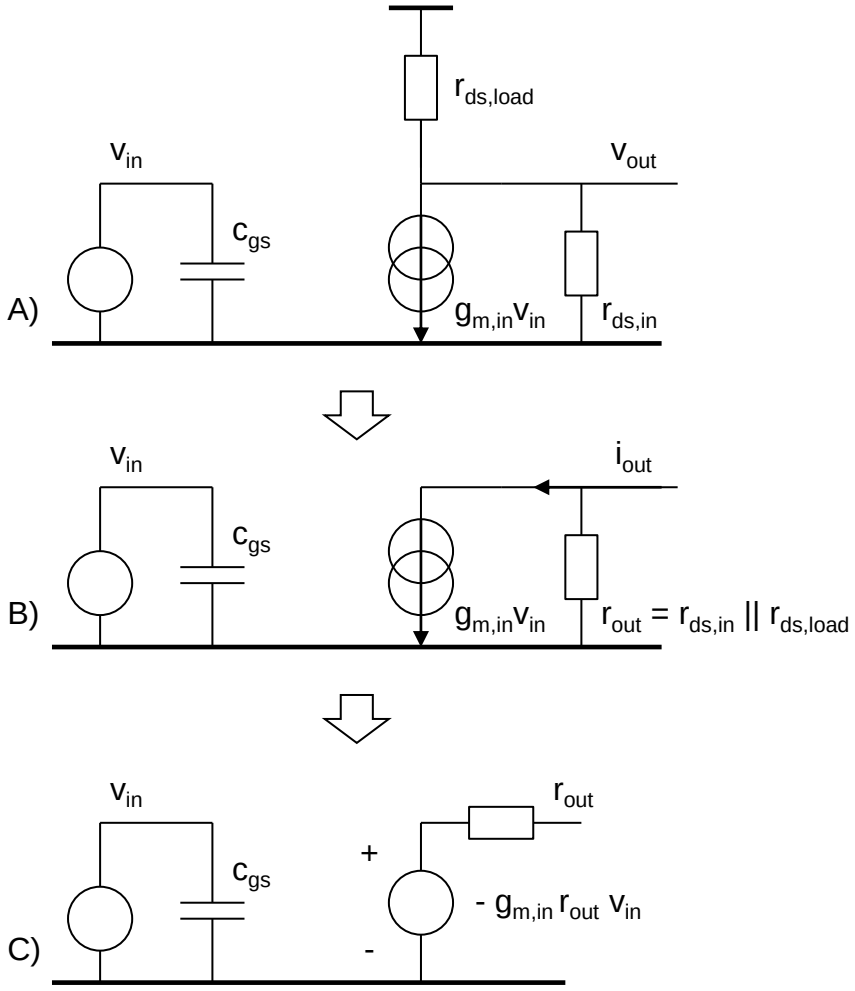


Fig 19: Small signal model of the common source amplifier with active load

The amplifier can therefore be represented as a voltage controlled current source with the current $i_{out} = g_{m,in}\, v_{in}$ and the output resistance $r_{out} = r_{ds,in} \parallel r_{ds,load}$. This is circuit B in Fig 19.

The amplifier can also be represented as a voltage controlled voltage source with the voltage $v_{out} = - g_{m,in}\, r_{out}\, v_{in}$ and the output resistance $r_{out} = r_{ds,in} \parallel r_{ds,load}$. This is circuit C in Fig 19. Both representations are equivalent.

Optimisation of the voltage gain (optionally)

We have seen in lectures 5 and 6 that a voltage amplifier is normally used with feedback. One example is the inverting amplifier with C_{in} and C_{fb}. One important parameter of this circuit is the open loop gain $\beta A = g_{m,in}\, r_{out}\, C_{fb}/(C_{fb} + C_{in})$. If $\beta A >> 1$, the voltage gain of the inverting amplifier becomes C_{in} / C_{fb}, i.e. it does not depend of process parameters g_m and r_{ds}. This is good since the values of C_{fb} and C_{in} are accurate and g_m and r_{ds} are prone to process variations. Therefore a large $g_{m,in}\, r_{out}$ is important because it leads to a large βA.

We have also derived in lecture 6 that a large g_m is important for a fast pulse response.

Let us find the optimal values of the following parameters: $I_{bias,}$, W and L of T_{in} and T_{load} in order to maximize g_m and voltage gain.

R_{out} is the parallel circuit of the r_{ds} resistors of T_{in} and T_{load}.

Let us write the formulas for r_{ds} and g_m.

It holds:

$$r_{ds} = \frac{LE_{sat}}{I_{dssat}} \qquad (7)$$

E_{sat} is the E-field when the drift velocity saturates. E_{sat} depends of dopant density.

For a 65 nm technology we have the following values:

E_{sat} of PMOS ~ 10.4 V/µm and E_{sat} of NMOS ~ 9.7 V/µm

µ(NMOS) = 2.64×10^{-2} m^2/Vs and µ(PMOS) = 1.45×10^{-2} m^2/Vs

C'_{ox} = 13.28 fF/µm^2 or 0.01328f/m^2

V_{th} ~ 0.4 V („regular“ V_{th} transistors)

The transconductance is calculated as dI_{dssat}/dv_{gs}.

For strong inversion it holds (s. lecture 4):

$$I_{dssat} = \frac{1}{2}\frac{W}{L}\mu C'_{ox}(V_{gs} - V_{th})^2 \qquad (8)$$

Therefore it is:

$$g_m = \frac{W}{L}\mu C'_{ox}(V_{gs} - V_{th}) = \sqrt{2\mu C'_{ox}\frac{W}{L}I_{dssat}} \qquad (9)$$

or

$$g_m = 2\frac{I_{dssat}}{V_{gs}-V_{th}} = 2\frac{I_{dssat}}{V_{dssat}} \qquad (10)$$

It holds also:

$$V_{dssat} = V_{gs} - V_{th} = \sqrt{I\frac{L}{W}\frac{2}{\mu C'_{ox}}} \qquad (10b)$$

If we increase L of the transistor T_{in} and keep other parameters constant, we increase its r_{ds} (7) but decrease g_m (9). We do not want to decrease g_m.

In order to increase both g_m and r_{out}, we have to scale up both W and L of the input transistor.

Disadvantage: This increases the layout of the transistor and its input capacity c_{gs}. A large input capacity is bad: it can reduce amplification and make the amplifier slower as it is shown at the end of lecture 6.

Optimization of Tin is also difficult.

We would recommend the following optimization method:

Optimisation of T_{in}:

1) We start from the specifications for power consumption and fix an I_{ds} current accordingly. (The power consumption is $I_{ds} \times VDD$.) Let us assume $I_{ds} = 40\ \mu A$.
2) A transistor length is defined. In analogue circuits, L should be at least $3 \times L_{min}$, as the transistors with the smaller length do not have a "nice" characteristic (r_{ds} is small). $L_{in} = m \times L_{min}$ (m=3). In our case $L_{min} = 65$ nm and $L_{in} = 200$ nm.
3) W of the input transistor is scaled up starting from W_{min} until the saturation voltage V_{dssat} drops to 100 mV.

$$V_{dssat} = V_{gs} - V_{th} = \sqrt{I \frac{L}{W} \frac{2}{\mu C'_{ox}}} \quad (10b)$$

Why do we assume 100 mV? The value $V_{gs} - V_{th} = 100$ mV indicates approximately the beginning of weak inversion (lecture 4). Further increase of W does not increase g_m.

Optimisation of T_{load}

The load source T_{load} is easier to optimize because its g_m is not so important. (Actually a small g_m is better as it lowers noise.) We should only maximise r_{ds}. Therefore we choose L_{load} large.

Note, however, that by a given current, an increase of L leads to a larger $|V_{gs}|$. This follows from equation (8). For this reason the saturation voltage $|V_{dssat}| = |V_{gs}| - |V_{th}|$ also increases. The signal range at the output, for which T_{load} is in saturation, gets smaller. We can therefore proceed as follows:

First we chose a V_{dssat} that leads to acceptable signal range, e. g. $V_{dssat} = 200$ mV. Then we choose a L_{load} of about $2 \times L_{in}$. We then scale up W_{load} until we achieve $V_{dssat} = 200$ mV.

Since a PMOS transistor has about 2× smaller μ then NMOS transistor, and since $V_{dssat,load} = 2\times V_{dssat,in}$, we expect $W_{load} \sim W_{in}$.

After such optimization we obtain $r_{ds,in} < r_{ds,load}$ because $L_{load} = 2\ L_{in}$ (7).

It holds:

$$A = -g_{m,in}(r_{ds,in} || r_{ds,load}) \sim -g_{m,in} r_{ds,in} \quad (11)$$

Let us calculate a typical voltage gain:

It holds for strong inversion:

$$g_{m,in} = \frac{2I_{dssat}}{V_{dsssat}} = \frac{2 \times 40\mu A}{0.1V} = 800\mu S$$

$$r_{ds,in} = \frac{E_{sat}L_{in}}{I_{dssat}} = \frac{\frac{9.7V}{\mu m} \times 200\ nm}{40\ \mu A} = 48.5\ k\Omega$$

$$A = -\frac{2I_{dssat}}{V_{dsssat}}\frac{E_{sat}L_{in}}{I_{dssat}} = -\frac{2E_{sat}L_{in}}{V_{dsssat}} = \frac{2 \times \frac{9.7V}{\mu m} 200\ nm}{0.1V} - 38.8$$

It is difficult to obtain a higher gain than 50 in such a way.

(The circuit from the exercises has a gain of 30.)

Cascode amplifier

How can we increase the amplification? One possibility is to use of cascode – transistor T_{casc} shown in Fig 20.

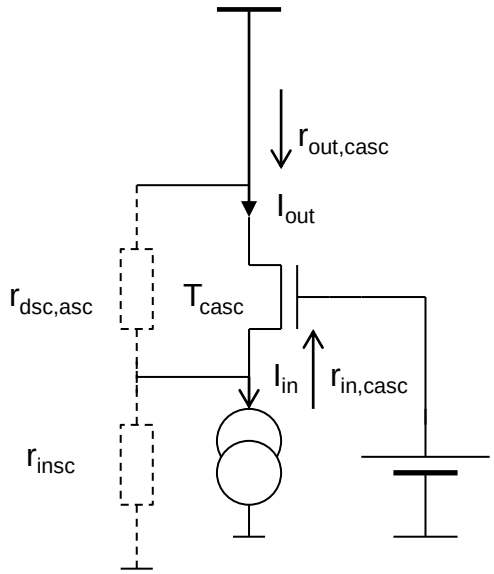


Fig 20: Cascode transistor

As we mentioned, the cascode transistor (T_{casc}) is an impedance converter, it holds: $I_{out} = I_{in}$.

The input impedance $r_{in,casc}$ (shown in Fig 20) is small, the output impedance $r_{out,casc}$ is large:

$r_{in,casc} = 1/g_{m,casc}$ (12)

$r_{out,casc} = g_{m,casc} r_{ds,casc}\, r_{insc}$ (13)

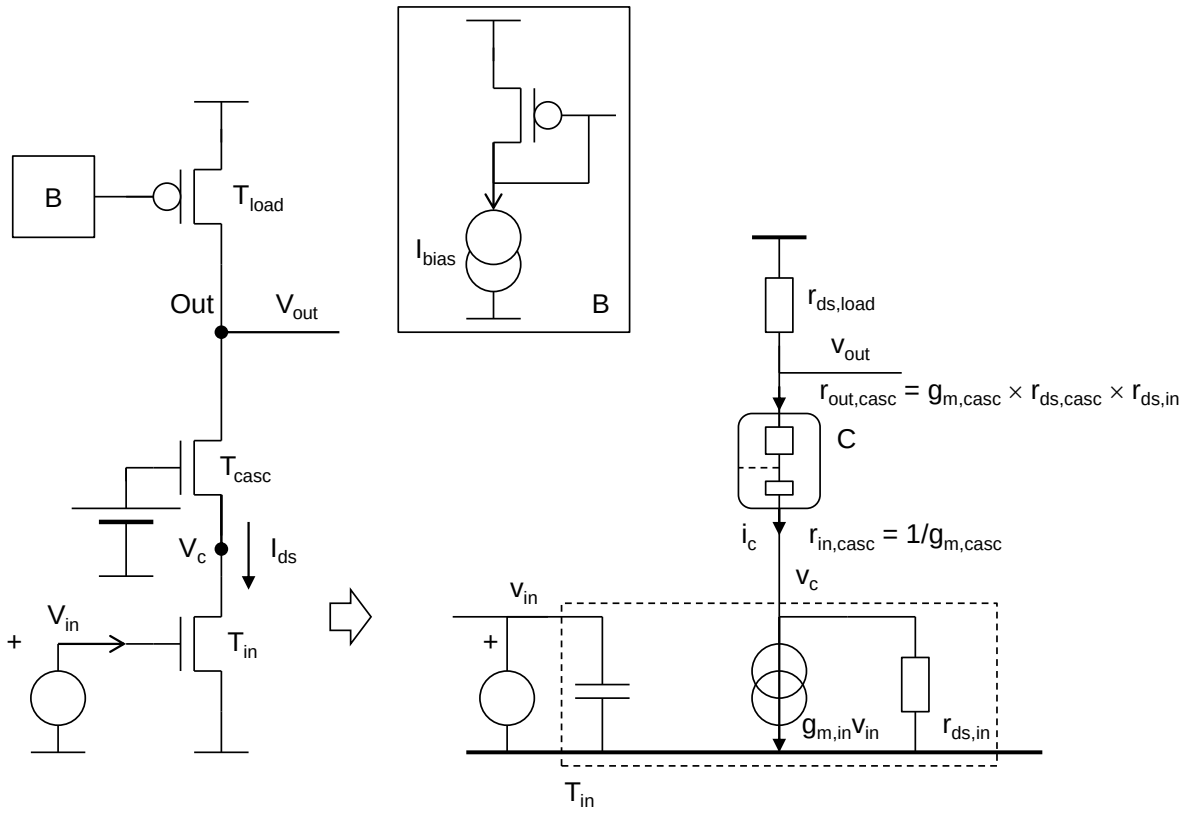


Fig 21: Common source amplifier with cascode transistor

Fig 21 shows the voltage amplifier with cascode transistor (or simply "cascode amplifier" or "amplifier with cascode"). We now have three transistors "in a line": the input transistor T_{in}, the cascode transistor T_{casc} and the load transistor T_{load}. Fig 21, right, shows the small signal schematics. The small signal current generated by T_{in} flows almost entirely through T_{casc} to the point Out.

The current generated by the current source of the transistor T_{in} ($i = g_{m,in}\, v_{in}$) splits to the current through r_{dsin} and the current through T_{casc} (denoted with C in Fig 21, right). The current through T_{casc} is calculated by the formula for current divider:

$$i_c = \frac{r_{ds,in}}{r_{ds,in} + r_{in,casc}} g_{m,in} v_{in}$$

Since $r_{in,casc}$ is smaller than $r_{ds,in}$, it holds:

$$i_c \sim g_{m,in} v_{in}$$

The current i_c flows to the node Out. The total resistance of the node Out (r_{out}) is the parallel connection of $r_{ds,load}$ and the output resistance of the cascode, $r_{out,casc}$ (13):

$$r_{out,casc} = r_{ds,load} || r_{out,casc} = r_{ds,load} || (r_{ds,in} g_{m,casc} r_{ds,casc}) \qquad (14)$$

The voltage gain is:

$$A_{casc} = -g_{m,in}\, r_{out,casc} = -g_{m,in}\,[r_{ds,load}||(r_{ds,in} g_{m,casc} r_{ds,casc})] \qquad (14)$$

Let us compare the output resistance and the voltage gain of amplifiers without and with cascode.

The output resistance without cascode was:

$$r_{out,nocasc} = r_{ds,load}||r_{ds,in} \quad (15)$$

When we optimize the amplifier following the method we described above ($L_{load} = 2L_{in}$), we obtain (7):

$$r_{ds} = \frac{LE_{sat}}{I_{dssat}}$$

And when we assume $E_{sat,pmos} \sim E_{sat,nmos}$:

$$r_{ds,load} \sim 2\, r_{ds,in}$$

It follows:

$$r_{out,nocasc} \sim r_{ds,load}||r_{ds,in} \sim r_{ds,in} \quad (16)$$

The voltage gain is:

$$A_{nocasc} = -r_{out,casc} g_{m,in} \sim -\, g_{m,in} r_{ds,in} \quad (16b)$$

Let us now consider the amplifier with cascode:

The product $g_{m,casc}\, r_{ds,casc}$ can be estimated using the formulas (7) und (10):

$$g_{m,casc} r_{ds,casc} = 2\frac{I_{dssat}}{V_{dssat}}\frac{L_{casc}E_{sat}}{I_{dssat}} = 2\frac{L_{casc}E_{sat}}{V_{dssat}}$$

Let us assume that the cascode transistor has equal dimensions as T_{in}: $L_{casc} = L_{in} = 200$ nm. Since the same DC current flows through T_{casc} and through T_{in}, we obtain:

$$g_{m,casc} r_{ds,casc} = 2\frac{L_{casc}E_{sat}}{V_{dssat}} = 2\frac{200\text{ nm} \times 9.7\frac{V}{\mu m}}{0.1} \sim 38.8$$

The output resistance with cascode is:

$$r_{out,casc} = r_{ds,load}||r_{out,casc} = (2\, r_{ds,in})||(28.8 r_{ds,in}) \sim 2 r_{ds,in} \quad (17)$$

The voltage gain with cascode is:

$$A_{casc} = -\frac{r_{out} i_c}{v_{in}} \sim -\, r_{out,casc} g_{m,in} = 2 g_{m,in} r_{ds,in} \quad (17b)$$

It follows from (17b) and (16b) that the voltage gain of cascode amplifier is by factor 2 larger than of the amplifier without cascode since $r_{out,casc}$ is 2 times larger than $r_{out,nocasc}$.

There are several possibilities to increase further the voltage gain:

We can for instance add a new PMOS cascode transistor T_{lcasc} to the current source T_{load}, as shown in Fig 22. In this way, we increase the output resistance of the load element current source from $r_{ds,load}$ (value without T_{lcasc}) to $r_{ds,load}\, g_{m,lcasc}\, r_{ds,lcasc} \sim 42\, r_{ds,load}$ (value with T_{lcasc} that has L = 400 nm and V_{dssat} = 200 mV).

It holds:

$$g_{m,casc} r_{ds,casc} = 2\frac{L_{casc} E_{sat}}{V_{dssat}} = 2\frac{400\text{ nm} \times 10.4\frac{V}{\mu m}}{0.2} \sim 41.6$$

The voltage gain is:

$$A_{doblecasc} = -g_{m,in}\left((r_{ds,load} g_{m,lcasc} r_{ds,lcasc}) \,||\, (r_{ds,in} g_{m,casc} r_{ds,casc})\right) \sim g_{m,in}\, r_{ds,in}\, g_{m,casc}\, r_{ds,casc} \quad (18)$$

The voltage gain with two cascode transistors (18) is about 20 × larger than with one transistor (17b).

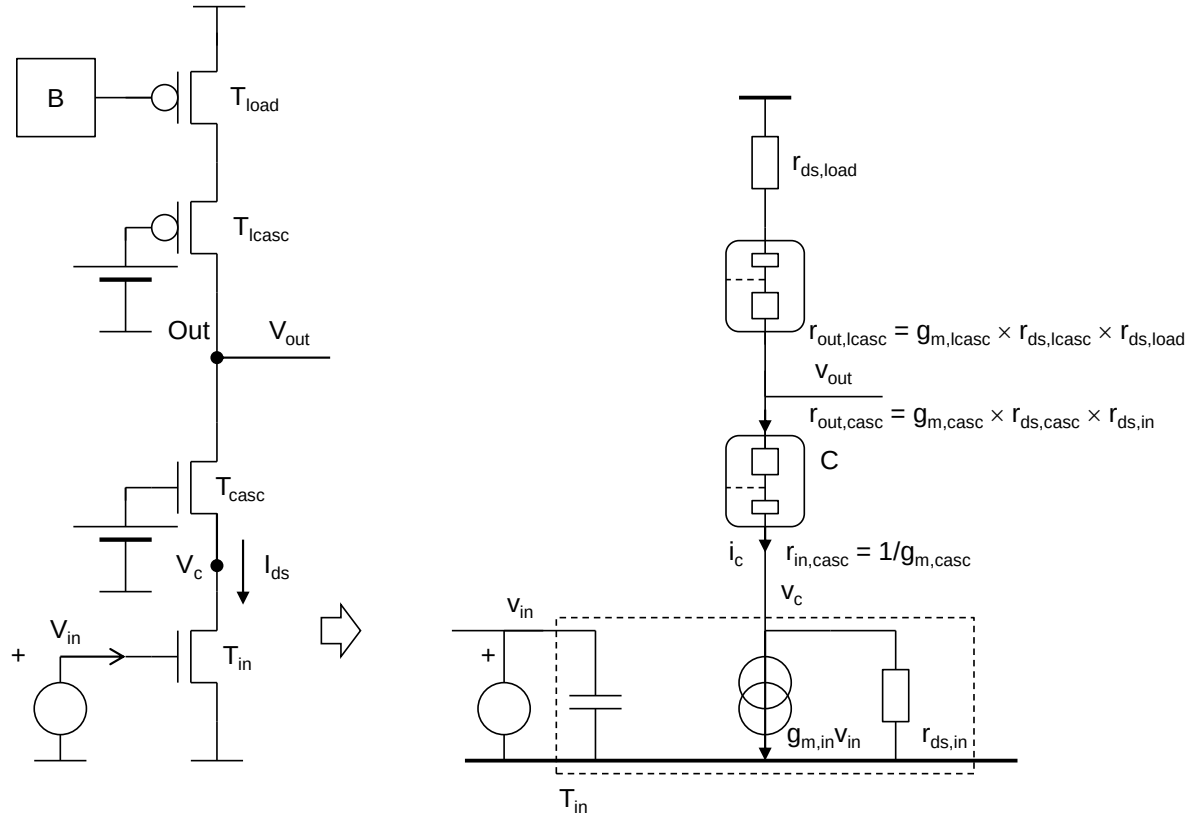


Fig 22: Common source amplifier with double cascode

Dynamic range

Another important property of amplifiers is the maximum signal range at the output. We call it dynamic range.

It is here important to mention that a small signal model is only valid when all transistors work in saturation. The transistors should be in saturation for the operating point and also when signals are added to the DC-voltages.

A voltage amplifier is often used with feedback.

If we use the feedback type as described in lectures 5/6 (inverting amplifier), we have a virtual mass at the input of the amplifier. The potential v_{IN} does not change.

An amplified signal is present at the output and the change of v_{OUT} is therefore large.

We should therefore primarily take care that the change of v_{OUT} is not too large in the way that is brings the transistors out of saturation region.

This is illustrated in Fig 21.

Let us calculate the maximum signal region at the output of the amplifier with cascode.

The potential v_{OUT} must be high enough so that both transistors T_{casc} and T_{in} are in saturation. This means:

$$v_{OUT} > V_{dssat,in} + V_{dssat,casc} = 0.1V + 0.1V = 0.2V \qquad (19)$$

This minimum voltage holds only when we chose the gate potential of T_{casc} in the way that the source potential of T_{casc} equals $V_{dssat,in.}$

The potential v_{OUT} must be low enough so that T_{load} is in saturation. This means:

$$v_{OUT} < VDD - V_{dssat,load} = 1.2V - 0.2V = 1.0V \qquad (20)$$

If we use the feedback as in lectures 5/6 (illustrated with resistance R_{fb} in Fig 23), it holds $V_{in} = V_{out.}$

Therefore:

$$V_{out} = V_{in} = V_{gs,in} = V_{dssat,in} + V_{th} = 0.1V + 0.4V = 0.5V \qquad (21)$$

The DC value V_{out} is 0.5 V. The V_{out} can decrease to 0.2 V (19) and increase to 1.0 V. If the signal is symmetrical around mean value, the maximum peak to peak amplitude is 0.6 V. This is shown in Fig 23.

Similar analysis can be carried out for the amplifier with double cascode, as shown in Fig 24.

Dynamic range is an important property. The quality of an analogue circuit depends on signal amplitude to noise ratio (SNR). The signal amplitude is often equal to the dynamic range. If we have a large dynamic range, SNR is large as well.

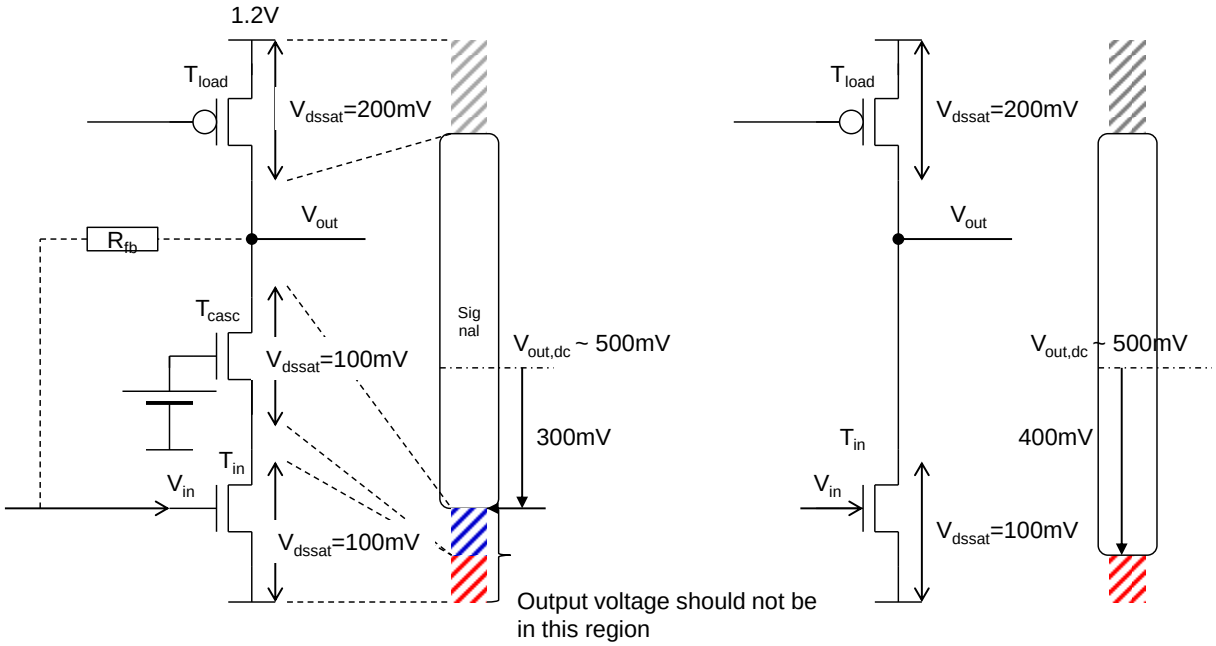


Fig 23: Dynamic range of the amplifier with cascode (left) compared with the dynamic range of the amplifier without cascode (right)

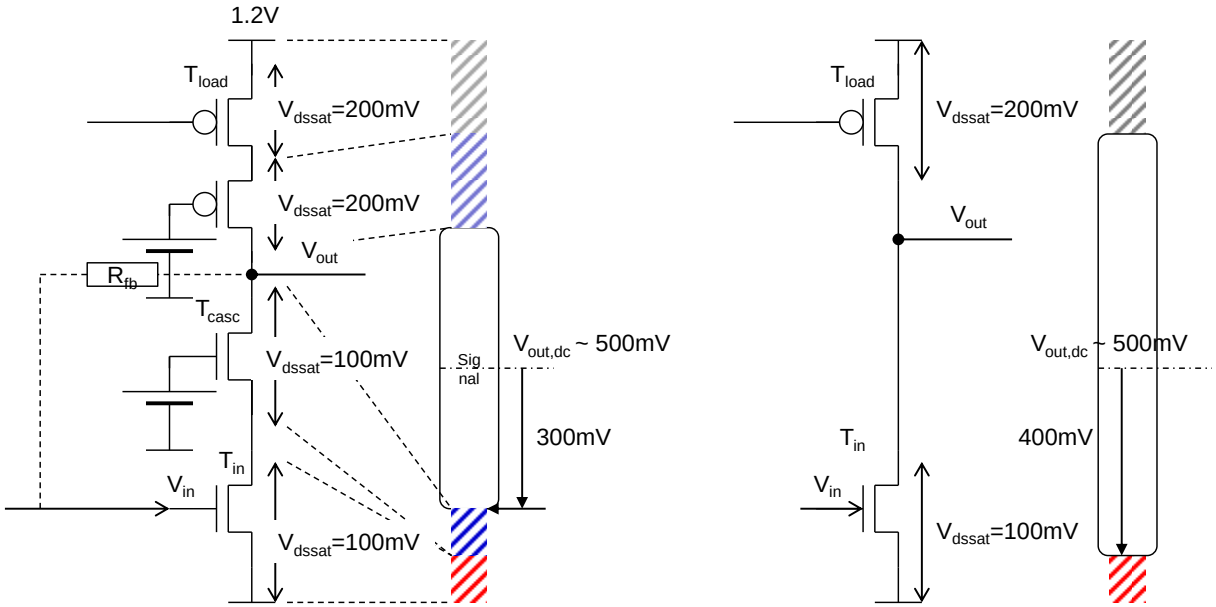


Fig 24: Dynamic range of the amplifier with double cascode (left) compared with the dynamic range of the amplifier without cascode (right)

Folded cascode amplifier

The last theme of this lecture is the folded cascode.

A cascode transistor can also be used as a circuit for adding of several currents, as shown in Fig 25.

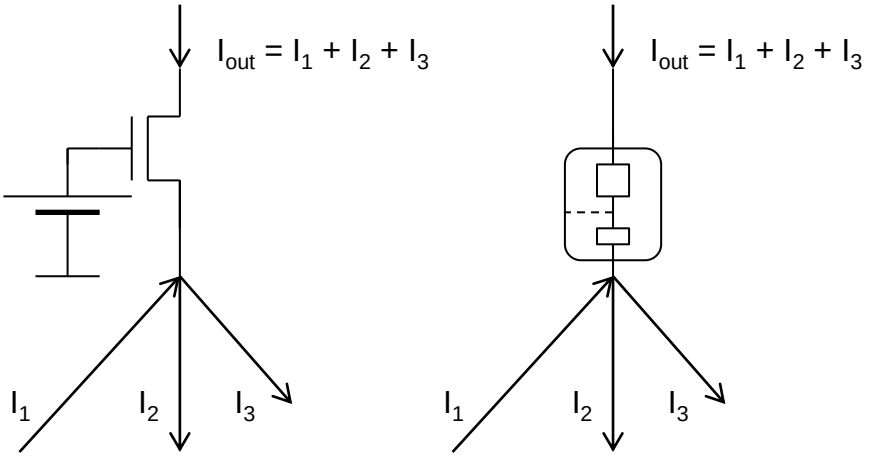


Fig 25: Adding of currents using a cascode transtor

We can use a PMOS as the cascode transistor as shown in Fig 26. Node C (Fig 26, right) is the source of T_{casc}. AC current turns around and flows as shown in Fig 26.

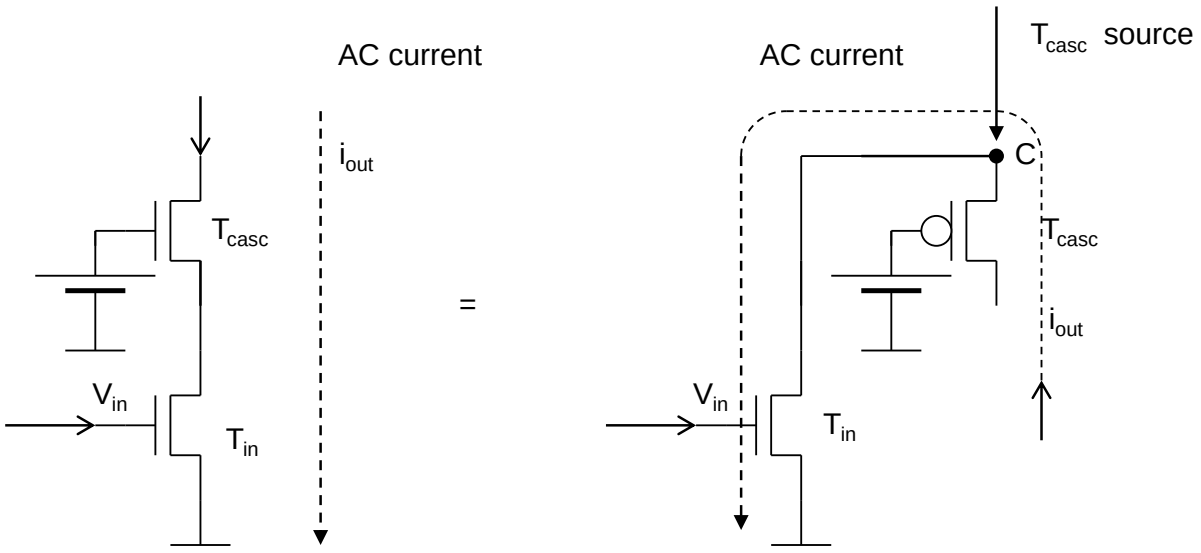


Fig 26: Folded cascode

Two more components are needed to build up a voltage amplifier (Fig 27):

A PMOS bias current source I_{bias} is used to assure a correct working point of cascode transistor T_{casc}.

A resistance R_{out} generates the output voltage.

The signal path has both its beginning and its end in the ground. In other words, if the current I_{ds} of T_{in} rises, the current $|I_{ds}|$ of T_{casc} decreases (Fig 27). This is why the circuit is called the folded cascode.

In difference to this, the circuits in Fig 21 and Fig 24 are referred to as the direct cascode amplifiers.

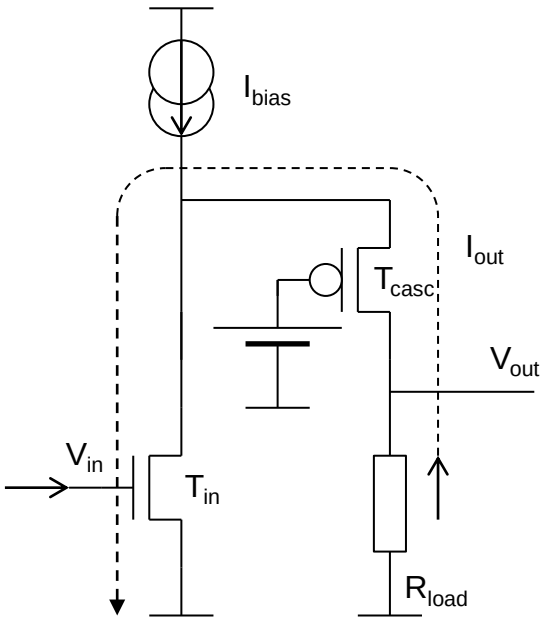


Fig 27: Folded cascode amplifier

We use an NMOS current source as the load element. The entire circuit is shown in Fig 28.

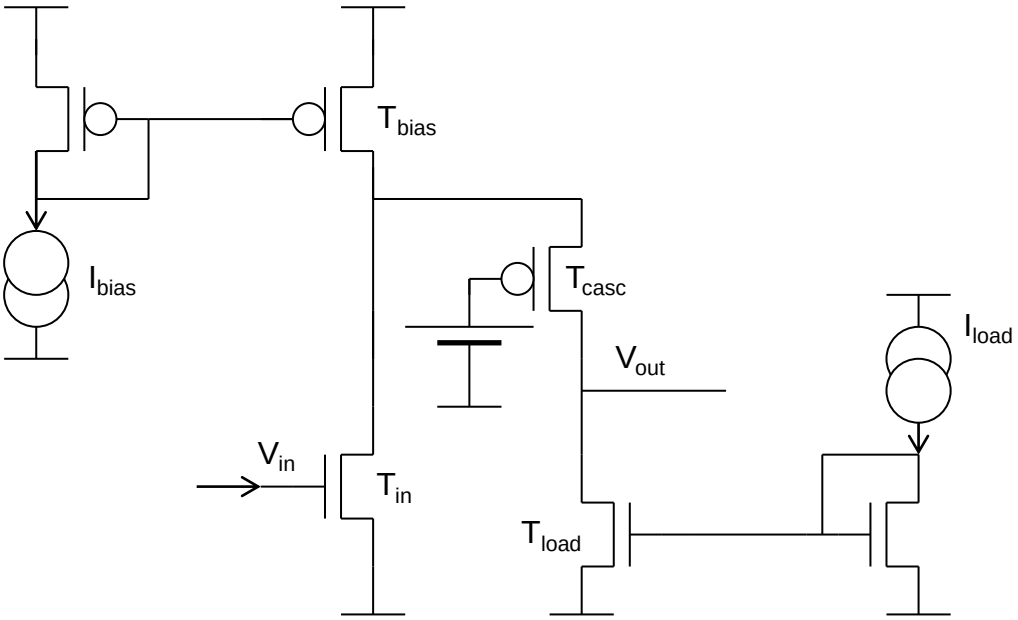


Fig 28: Folded cascode amplifier: full schematics

The small signal circuit is shown in Fig 29.

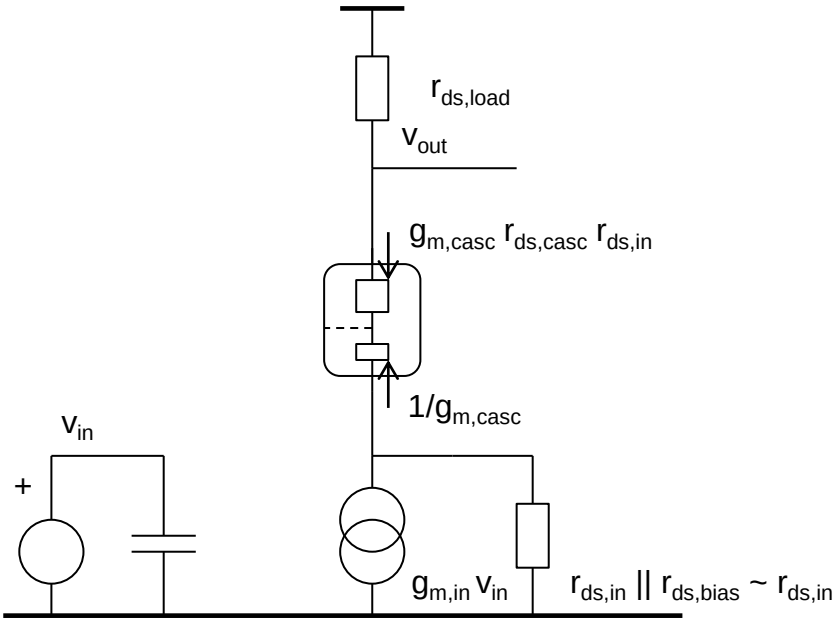


Fig 29: Folded cascode amplifier: small signal circuit

We removed all constant current sources. The PMOS bias source represents only a relatively large $r_{ds,bias}$ resistance, which is parallel to $r_{ds,in}$ resistance of the input transistor. We will neglect $r_{ds,bias}$ since it is larger than $r_{ds,in}$. NMOS load makes a load resistance $r_{ds,load}$.

When we compare this circuit with the small signal schematics of the direct cascode amplifier (Fig 21), we see that the circuits are equal. Accordingly, the parameters such as amplification, r_{out} given with the same formulas. The amplification is:

$$A = -g_{m,in}\left(r_{ds,load} || r_{ds,casc}\, g_{m,casc}\, r_{ds,in}\right) \quad (22)$$

Let us estimate the values of the parameters. For this, we consider the DC currents.

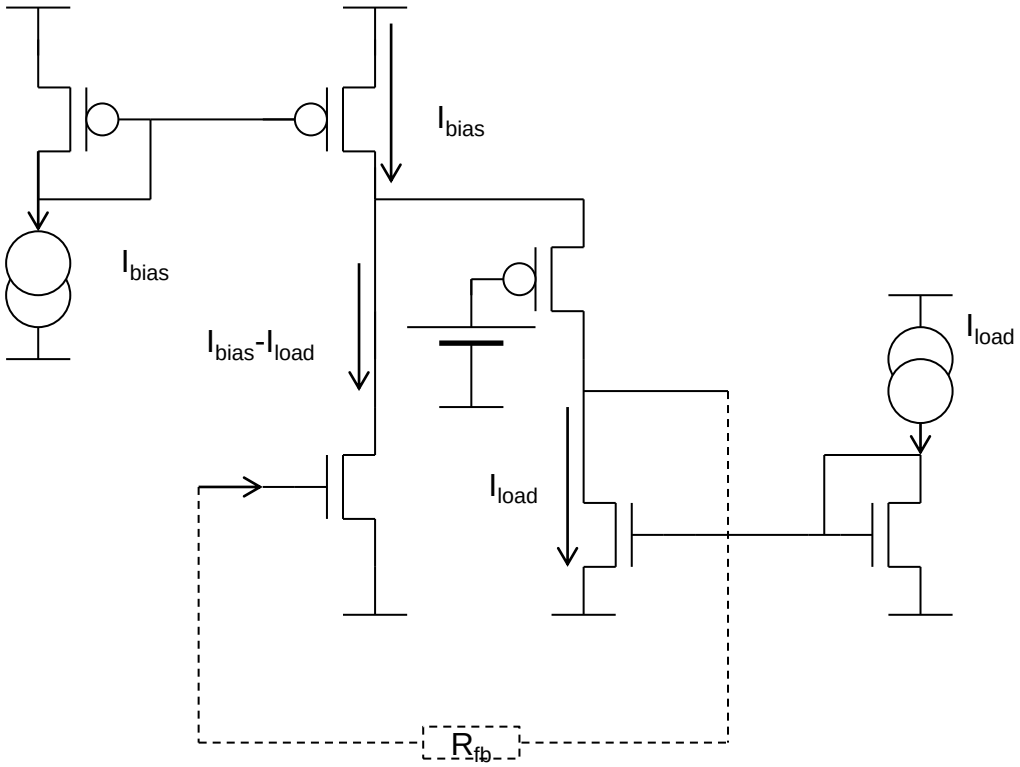


Fig 30: Folded cascode amplifier: DC-currents

DC current I_{load} flows through T_{load} and T_{casc} (Fig 30). DC current I_{bias} flows through the PMOS T_{bias}. Current $I_{bias} - I_{load}$ flows through T_{in}. I_{bias} must be larger than I_{load}, otherwise T_{in} is off.

We want to maximize both $g_{m,in}$ and $r_{ds,load}$ in order to obtain a large voltage gain. For a large $g_{m,in}$, the bias current (DC current) through the input transistor must be large. For a large resistance $r_{ds,load}$, the bias current through the load transistor must be small. In the case of the simple direct cascode amplifier (Fig 21) the two components have the same current and it was impossible to fulfil both conditions. In the case of the folded cascode, we achieve both conditions by setting $I_{load} << I_{bias.}$ A suitable choice is: $I_{load} = 0.1\ (I_{bias} - I_{load})$

Since I_{load} is 10× smaller than T_{in} bias current, L_{load} can be chosen longer than L_{in}: e.g. $L_{load} = 2L_{in}$.

In this case it holds: $r_{ds,load} = 20 \times r_{ds,in}$. (because of $r_{ds} = E_{sat}\ L / I$).

Factor $r_{ds,casc}\ g_{m,casc}$ is about 80 for L_{casc} = 400nm and $V_{dssat,casc}$ = 100 mV:

$$g_{m,casc} r_{ds,casc} = 2 \frac{L_{casc} E_{sat}}{V_{dssat}} = 2 \frac{400\ \text{nm} \times 10.4 \frac{V}{\mu m}}{0.1} \sim 83.2$$

Therefore it holds for the folded cascode:

$$A = -g_{m,in} \left(r_{ds,load} || r_{ds,casc}\, g_{m,casc}\, r_{ds,in} \right) \sim 20\, g_{m,in} r_{ds,in} \quad (23)$$

This is about 20× larger than in the case of the common source amplifier (11) (which has the gain of 40) 10× larger than in the case of simple direct cascode amplifier (17b) and about the same as in the case of the amplifier with double cascode (18).

The folded cascode is often used because it has a good voltage gain and a large dynamic range that is symmetrical around the DC value as shown in Fig 31.

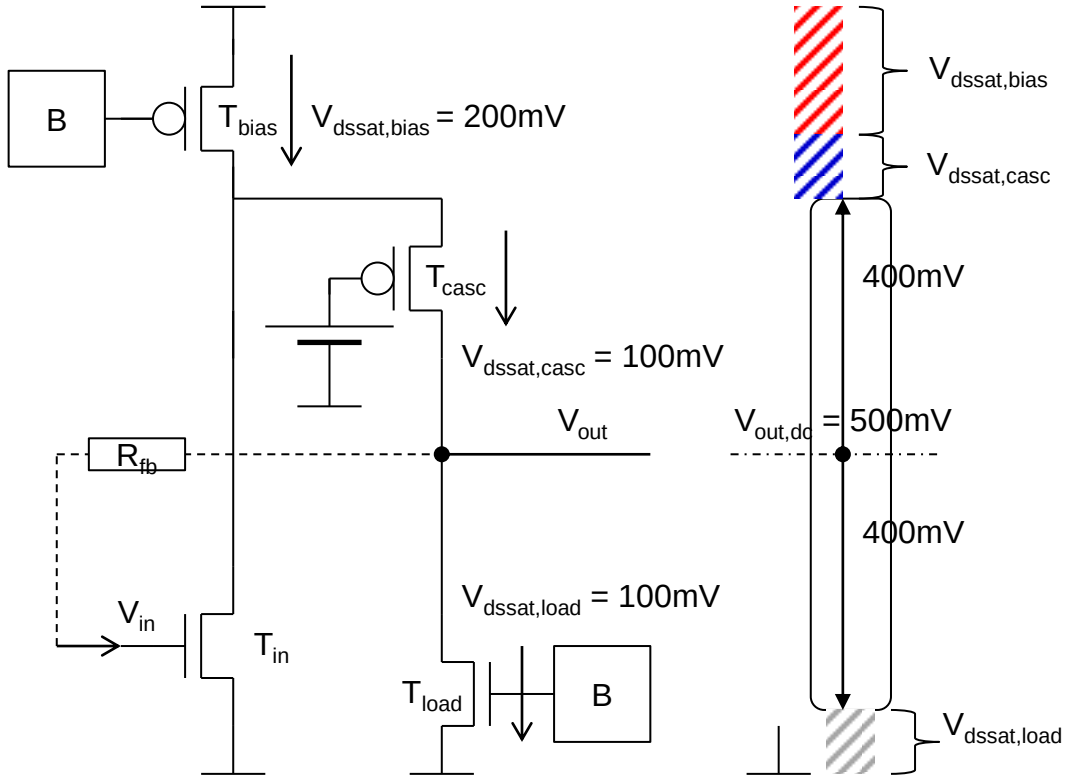


Fig 31: Folded cascode amplifier: dynamic range