Lecture 4

Themes:

General formulas for every working condition

Weak inversion

Capacitances

Small signal model

General formulas for every working condition (optionally)

The following formula that holds in triode region can be derived

$$I_{ds} = \mu C'_{ox} \frac{W}{L}\left((V_{gs} - V_{thsb})V_{ds} - n\frac{V_{ds}^{2}}{2} \right); V_{thsb} \equiv V_{th} + (n-1)V_{sb} \quad (1)$$

The derivation is in a separated document in the file „MOSFET Detailed“. (This document is optional, it is not the subject of the course.)

The formula (1) takes the body effect into account, this is why it contains factors $n = 1 + C_{dep,min}/C_{ox}$ (slope factor) and the corrected threshold voltage $V_{thsb} = V_{th} + (n-1)V_{sb}$.

The formula is not very elegant because it is asymmetrical with respect to source and drain. The transistor is, on the other hand, symmetrical. It would be better if the formula reflects this symmetry. This can be fixed in the following way.

$$I_{ds} = \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{th} - (n-1)V_{sb})^2 - \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gd} - V_{th} - (n-1)V_{db})^2 \quad (2)$$

or

$$I_{ds} = \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})^2 - \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gd} - V_{thdb})^2 \quad (2b)$$

It can be shown that formulas 2 and 2b follow from (1) when the terms in brackets are multiplied.

The formula 2b gives us the idea to represent a transistor as a parallel circuit of two ideal transistors. These ideal transistors conduct current only from drain to source and are always in saturation. Such a representation is useful to solve certain circuits.

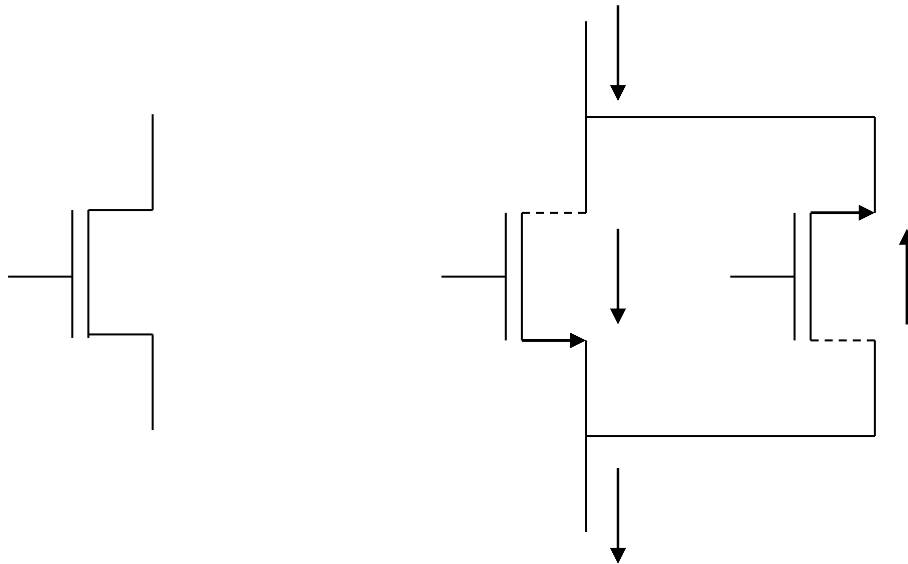


Figure 1: General transistor model

Weak inversion

During previous analysis of MOSFET, we assumed that the channel charge and the I_{ds} current equal zero for $V_{gs} < V_{th}$. We derived for instance:

$$I_{dssat} = \frac{1}{2n}\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{thsb}\right)^2$$

The formulas are based on a simplistic model of channel charge. They are not correct enough for analysis of certain circuits.

We will now consider the case when V_{gs} somewhat smaller than V_{thsb}.

We call this operation region the weak inversion (subthreshold region). In contrast to this, for $V_{gs} > V_{thsb}$ we have a strong inversion.

We considered in lecture 2 the case of V_{gs} = 0.35 V. Let us start with this.

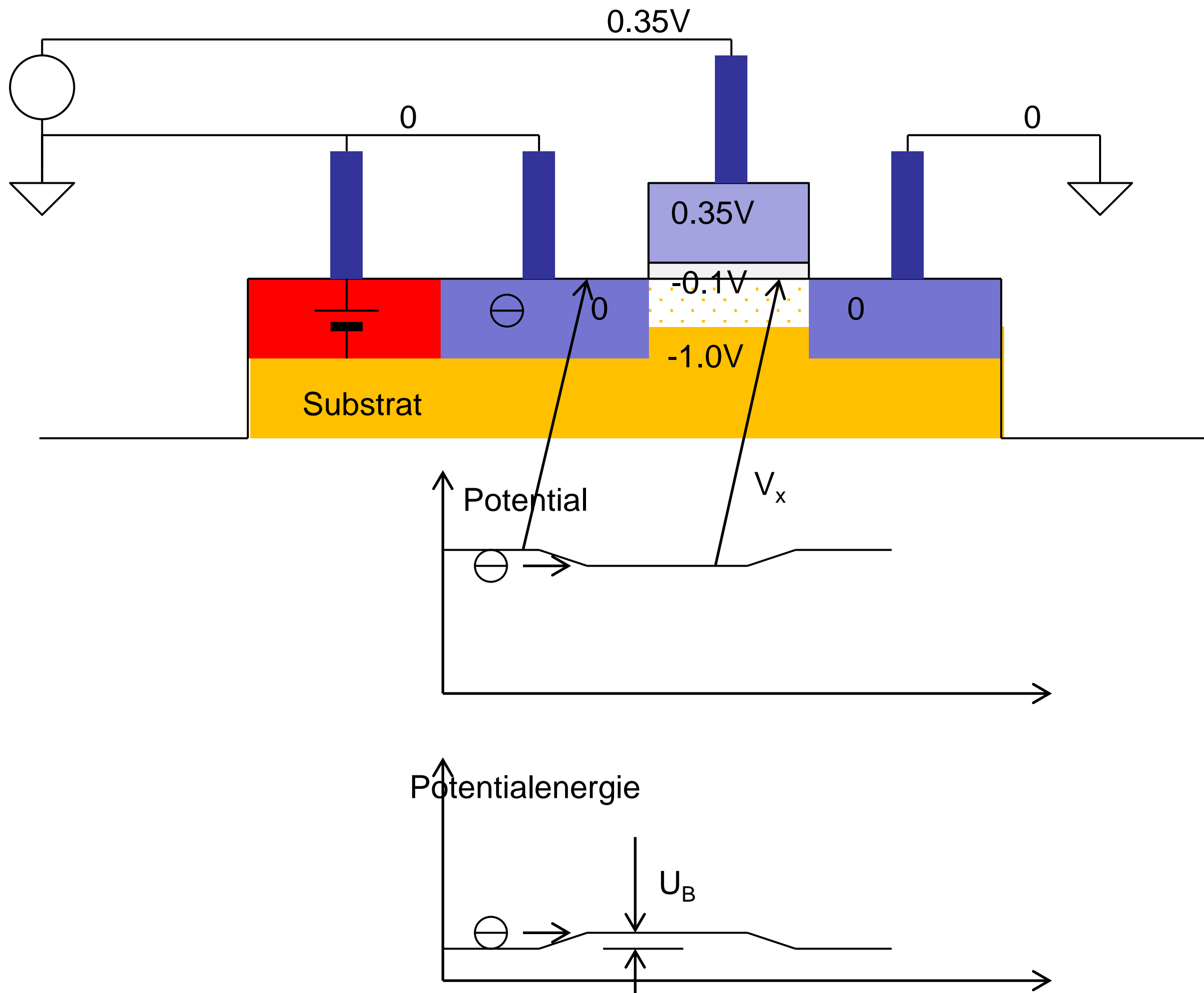


Figure 2: Potentials in the case of weak inversion

Let us repeat some results from solid state physics. Source and drain contain free electrons, because they are n-doped, and also because they have a higher electrostatic potential. Consequently, the substrate contains holes because it is at a lower electrostatic potential. The holes get collected at the places with lower potential and electrons get collected at the places with higher potential. A positive electrostatic potential is a potential barrier for positive charges. A negative electric potential is a barrier for electrons.

Let us take a look at Figure 2. The deeper substrate regions are at -1 V. The surface of the substrate below gate oxide has a potential only slightly lower than source and drain. The potential barrier for electrons coming from source into the substrate is small (0.1 V) and electrons can pass from source to drain if they get an energy > 0.1 eV from thermal oscillations of crystal lattice (from “phonons”).

When is a potential barrier small? A small barrier is comparable with the mean thermal energy of electrons. Remember that the thermal energy at room temperature (300 K) corresponds to a voltage of U_T = 26 mV. $U_T = kT/e$. The thermal energy is the average kinetic energy of an electron at a certain temperature.

Let us estimate the current between drain and source caused by the thermal energy and density gradient of electrons (diffusion current).

The first assumption is that we have a diffusion current. We need to derive the charge carrier density/area[1] in the substrate region between the source and drain. If we know the density we can derive the current using the equation for diffusion current.

We will calculate the density of charge carriers (in the case of NMOS transistor electrons) in several steps. The first step is the derivation of the electric potential underneath gate oxide as a function of vertical z-coordinate. The second step is the calculation of the charge carrier density as a function of the potential. The third step is the integration of the density function in z-direction. We will not do all steps exactly. For exact derivation, I refer to „MOSFET Detailed“.

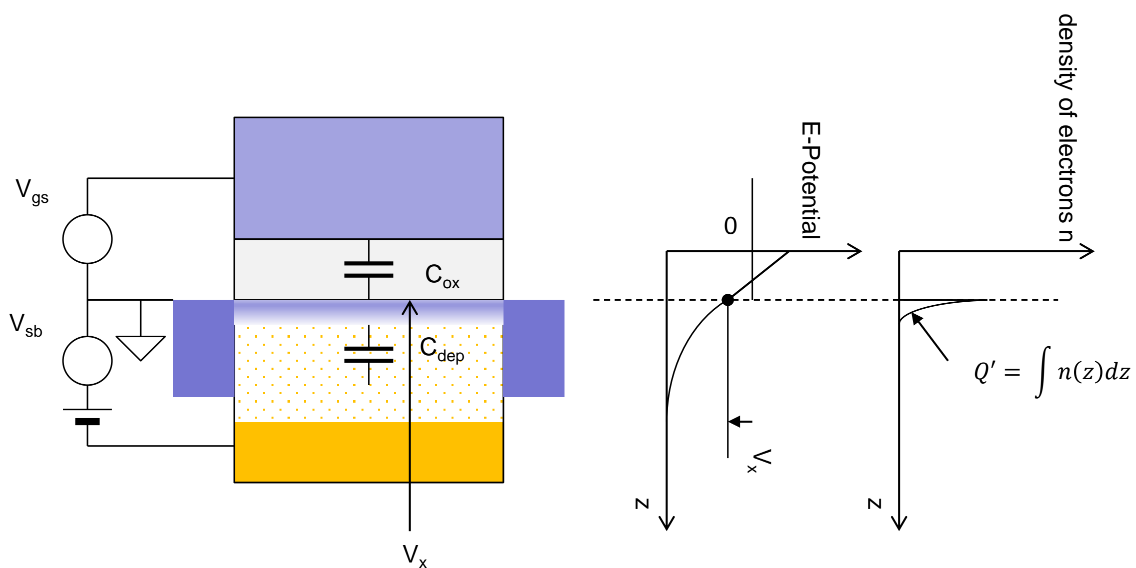


Figure 3: Weak inversion, potential and electron density within p-substrate

For instance we will not derive the exact potential vs z-coordinate dependence (see Figure 3) than just write the formula for the potential at the substrate surface (V_x) as function of V_{gs}:

$$V_x = \frac{C_{ox}}{C_{dep} + C_{ox}}(V_{gs} - V_{thsb})$$

Also in this lecture we calculate just a small difference of V_x with respect to the V_x value for $V_{gs} = V_{thsb}$. ($V_{dep} \sim V_{cont} + V_{sb}$.) It is then justified to assume:

$C_{dep} = C_{dep,min}$.

$C_{dep,min}$ is the dynamic capacitance for $V_{dep} = V_{cont}$.

[1] The density integrated in z-direction

The height of the potential barrier U_B is equal to the difference of the source potential V_s and the potential of the substrate surface V_x. For $V_{gs} = V_{thsb}$, it holds $V_x = 0$. For smaller V_{gs} the following formula is valid:

$$U_B = -V_x = -\frac{C_{ox}}{C_{dep} + C_{ox}}(V_{gs} - V_{thsb}) = -\frac{(V_{gs} - V_{thsb})}{n} \qquad (3)$$

As mentioned, a negative voltage is a (positive) potential barrier for electrons. For this reason we write the minus sign before V_x in (3).

$$Q' = C'_{dep} U_T e^{-U_B/U_T} = C'_{dep} U_T e^{(V_{gs} - V_{thsb})/nU_T}$$

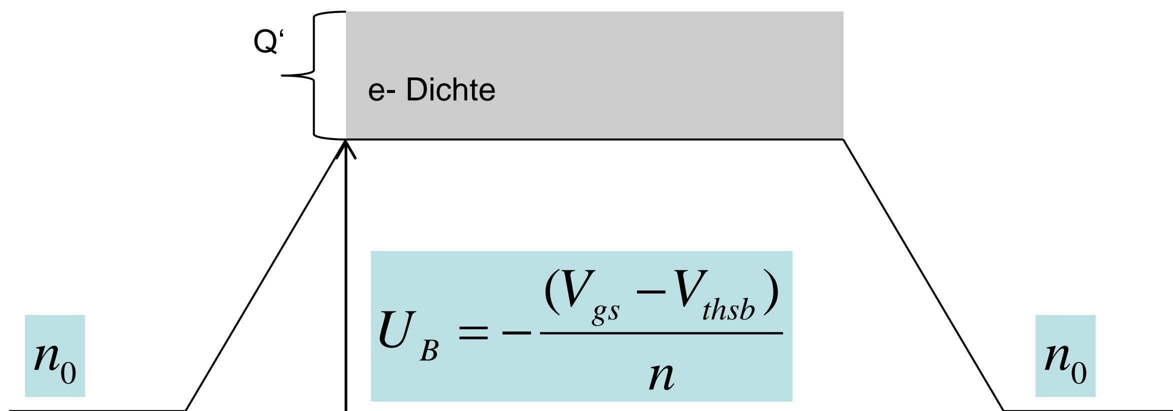


Figure 4: The density of the charge carriers in the substrate below the gate oxide for $V_{gs} < V_{th}$ and for $V_{ds} = 0$.

Let us now calculate the density of the electrons in the substrate below SiO_2. The electron density in source is $n_0 = N_d$. N_d is the density of donor atoms.

The electron density in equilibrium state is given by the Maxwell Boltzmann distribution.

The question of equilibrium is always “difficult” when currents flow, but at least we can assume that the source-channel and drain-channel junctions are in equilibrium and that electron densities in source and drain are N_d.

For this reason, the electron density at the substrate surface (in the “channel region”) is given by:

$$n = N_d e^{-U_B/U_T} \quad (4)$$

The derivation of the density per unit area is not easy. We should perform the integration in z-direction. For this we would need the function n(z). As mentioned „MOSFET Detailed“ shows the exact derivation.

The result quite intuitive.

$$Q' = \int n(z)dz = \int n_0 e^{-V(z)/U_T} dz = \cdots ???\ldots = C'_{dep}\, U_T e^{-U_B/U_T} \quad (5)$$

Q' is the charge density per area, C'_{dep} is the dynamic capacitance / area of the depleted region. (Precisely $C'_{dep} = C'_{dep,min}$, the capacitance for $V_{dep} = V_{cont}$.)

The charge density is for $V_{ds} = 0$ uniformly distributed in x-direction. Therefore the I_{ds} current is zero.

A current will flow only if there is a density gradient. A gradient will be formed when there is a voltage between drain and source.

Let us now consider the case $V_{ds} \neq 0$.

How large is the potential barrier between drain and substrate?

The threshold at the drain end of the channel region is by (n-1) V_{ds} larger than V_{thsb} because of the body effect.

The potential barrier between the drain and the substrate surface is:

$$U_{B,D} = -\frac{(V_{gd} - V_{thsb} - (n-1)V_{ds})}{n} = -\frac{(V_{gs} - V_{thsb})}{n} + \frac{(V_{ds} + (n-1)V_{ds})}{n} = U_{B,S} + V_{ds} \quad (6)$$

$U_{B,S}$ is the potential barrier between drain and substrate.

If we substitute (6) into (5) we obtain the following result: The charge density in the channel region is close to drain by exp ($-V_{ds}/U_T$) smaller than close to source. This result can be also derived when we apply Maxwell-Boltzmann formula in the drain-substrate junction region. The electron density in the drain is N_d and in substrate close to drain N_d exp ($-U_{B,D}/U_T$).

Notice the following: Maxwell-Boltzmann Formula does not "work" in the channel region. The potential is there independent of x coordinate (Figure 5), but the electron density changes from Q'_s to Q'_d. The reason for this is that this region is not in the equilibrium state when a current flows. The Fermi energy (a parameter of the Fermi-Dirac distribution) is not constant in the channel region. For this region, we cannot approximate Fermi-Dirac distribution with Maxwell-Boltzmann formula.

Summary (Figure 5):

The charge density close to source is

$$Q'_s = C'_{dep}\, U_T e^{(V_{gs} - V_{thsb})/nU_T} \quad (7)$$

The charge density close to drain is

$$Q'_d = Q'_s\, e^{-V_{ds}/U_T} \quad (8)$$

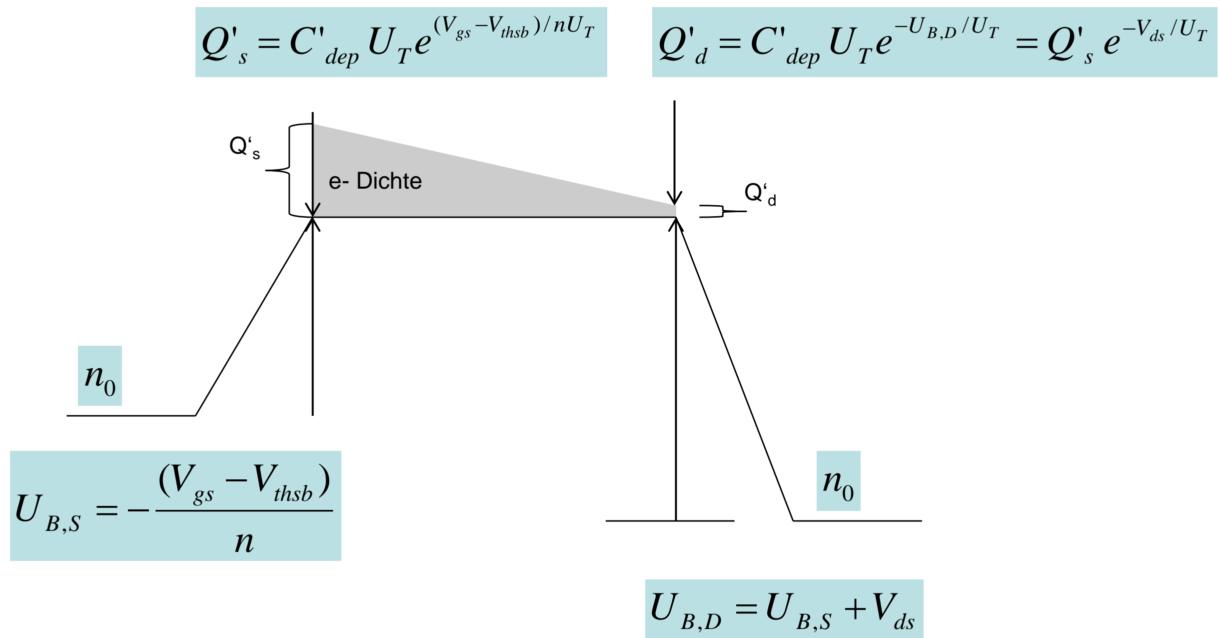


Figure 5: The density of the charge carriers in the substrate below the gate oxide for $V_{gs} < V_{th}$ and for $V_{ds} > 0$.

As equations 7 and 8 show, there is a density gradient. It yields to the following diffusion current:

$$|I| = W \cdot D \cdot \frac{dQ}{dx} \quad (9)$$

D is the diffusion constant, for which the Einstein-equation holds:

$$D/\mu = U_T \quad (10)$$

It follows:

$$I \approx W \cdot D \cdot \frac{Q'_s - Q'_d}{L} = \frac{W}{L}\mu U_T Q'_s (1 - e^{V_{ds}/U_T}) \quad (11)$$

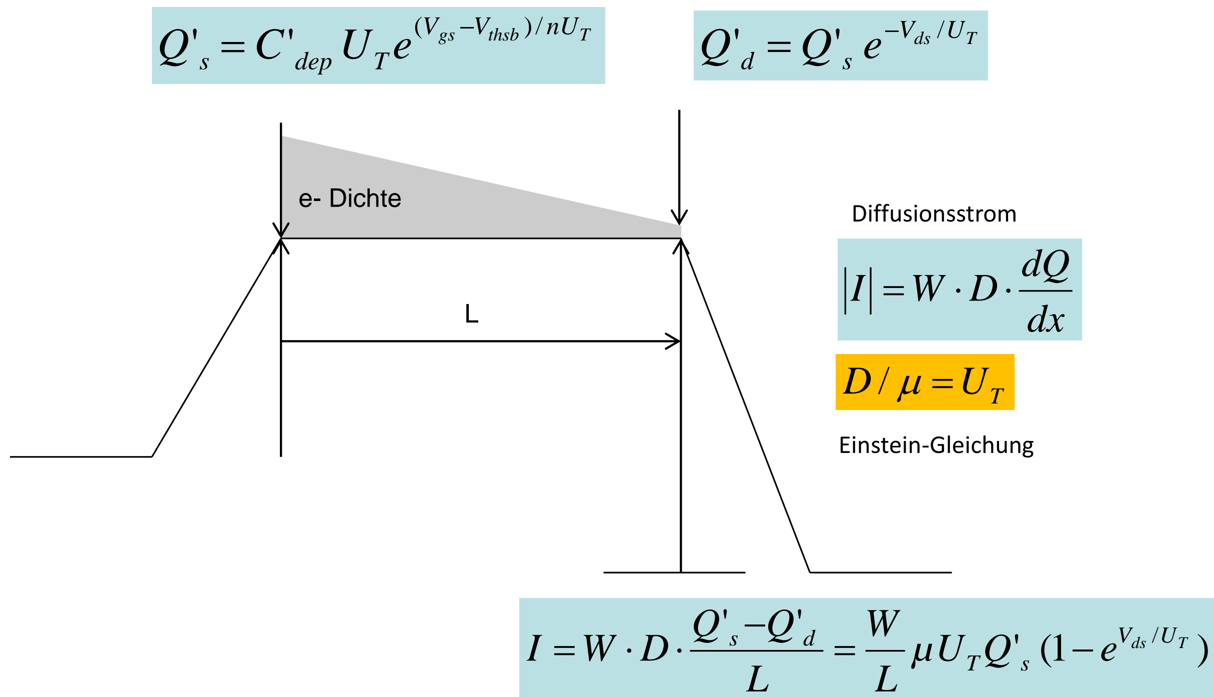


Figure 6: Diffusion current for $V_{gs} < V_{th}$

The characteristics $I_{ds} = f(V_{ds})$ (11) shows saturation behaviours for V_{ds} > a few U_T (Figure 7):

$$I_{ds} = \text{const} \cdot e^{(V_{gs}-V_{thsb})/nU_T}\left(1 - e^{-V_{ds}/U_T}\right) \quad (12)$$

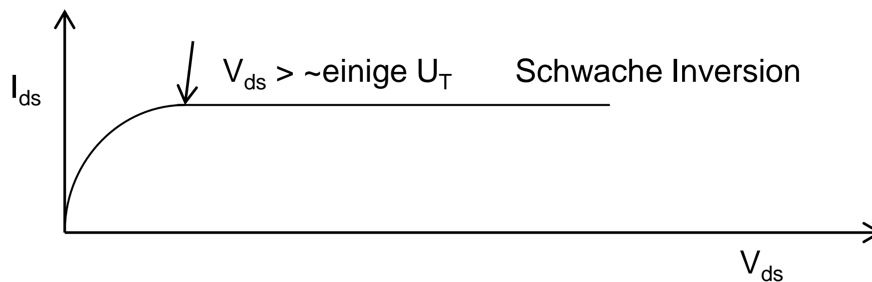


Figure 7: Saturation of the diffusion current für $V_{ds} > U_T$.

When we substitute V_{ds} > a few U_T in (11), we get:

$$I_{dssat} = \frac{W}{L}\mu U_T Q'_s \quad (13)$$

It holds also (7):

$$Q'_s = C'_{dep} U_T e^{(V_{gs}-V_{thsb})/nU_T} \qquad (14)$$

and

$$C'_{dep} = (n-1)C'_{ox} \quad (15)$$

By substituting (14) and (15) into (13) we obtain the equation for saturation current for weak inversion:

$$I_{dssat} = \frac{W}{L} \cdot \mu \cdot C'_{ox} \cdot U_T^{\,2} \cdot (n-1) \cdot e^{(V_{gs}-V_{thsb})/nU_T} \quad (16)$$

We can conclude

1) A transistor is never fully off. Assume $V_{gs} = V_{thsb}$. From equations for strong inversion we would expect $I_{dssat} = 0$. If we use equation (16) we obtain $I_{dssat} \sim W/L \times 100$ nA.

2) The condition for saturation is in weak inversion V_{ds} > a few U_T. Notice that V_{dssat} does not depend of V_{gs}, as it does in strong inversion.

Strong inversion: $V_{ds} > (V_{gs} - V_{thsb})/n$.

This is an interesting result that influences some circuits (e.g. current mirrors).

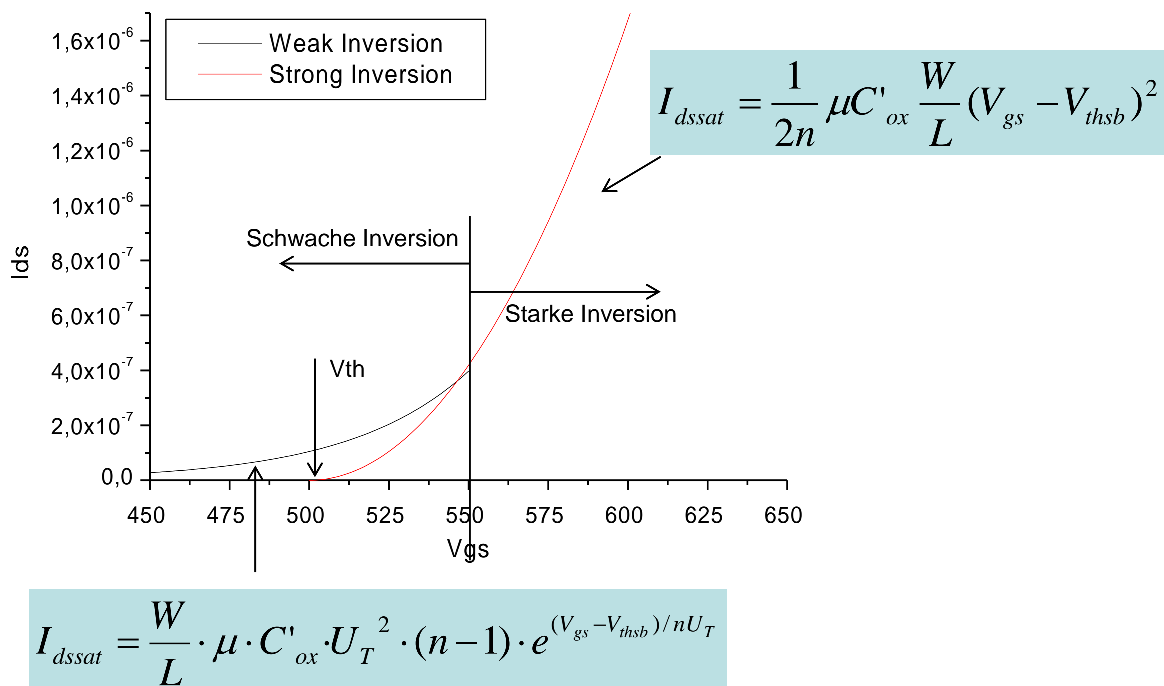


Figure 8: Simulated current as function of V_{gs}

A current of 100 nA may sound small but for many applications it is significant. Let us assume a DRAM cell with a capacitance of 10 fF. In the case of a 100nA current, the DRAM cells gets discharged in about 100 ns.

Weak inversion is one of the reasons for DC current consumption of CMOS logic gates.

We can divide the V_{gs} voltage range in weak inversion ($V_{gs} < V_{thsb}$ + a few U_T) and in strong inversion $V_{gs} > V_{thsb}$ + a few U_T, as shown in Figure 8.

For strong inversion following equation is valid:

$$I_{dssat} = \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})^2 \quad (17)$$

For weak inversion we derived (16):

$$I_{dssat} = \frac{W}{L}\cdot\mu\cdot C'_{ox}\cdot U_T^2\cdot(n-1)\cdot e^{(V_{gs}-V_{thsb})/nU_T}$$

A further consequence of weak inversion is that we cannot increase the transconductance by increasing W/L ratio beyond some value if the bias current is kept constant.

Let us calculate the transconductance as dI_{dsat}/dv_{gs}:

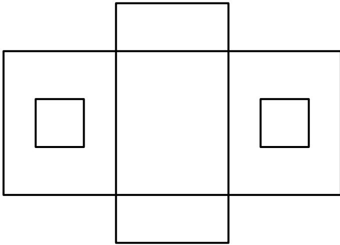
From the formula for strong inversion (17) we get:

$$g_m = \sqrt{2kI_{dssat}\cdot(W/L)}; k = \mu C'_{ox}/n \quad (18)$$

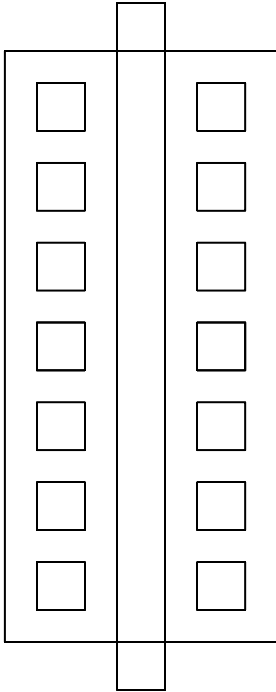
From the formula for weak inversion (16) we get:

$$g_m = I_{dssat}/nU_T \quad (19)$$

Equation (18) would imply, that we can increase g_m as much as we wish when the transistor is made shorter and wider. However this is not true. If we have a constant bias current I_{ds}, increase of W/L lead to a decrease of V_{gs} - $V_{thsb.}$ This yields from (17). This puts a transistor into weak inversion where the transconductance does not depend of W/L. The increase of g_m is stopped. The value $I_{dssat}/n \times U_T$ is the maximum transconductance that we can get from an MOS transistor for a given I_{dssat} bias current.



$$g_m = \sqrt{2kI_{dssat}(W/L)}$$



$$g_m = I_{dssat}/nU_T$$

Figure 9: Transconductances of a transistor working in strong inversion (left) and weak inversion (right) respectively.

Let us now summarize the transistor equations that we derived so far:

Strong inversion

Simple model with body effect

$$I_{ds} = \frac{\mu_0 C'_{ox} W}{L}\left((V_{gs} - V_{thsb})V_{ds} - n\frac{V_{ds}^2}{2}\right)$$

Saturation voltage

$$V_{ds} = \frac{V_{gs} - V_{thsb}}{n} \equiv V_{dssat}$$

Saturation current

$$I_{dssat} = \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})^2$$

Body effect

$$V_{thsb} = V_{th} + (n-1)V_{sb}$$

n is the slope factor, $n = 1 + C_{dep,min} / C_{ox} \sim 1.25$.

If we do not want to take body effect into account we can set n = 1.

Model that assumes velocity saturation

$$I_{ds} = \frac{\mu_0 C'_{ox} W}{L\left(1 + \frac{V_{ds}}{LE_{sat}}\right)}\left((V_{gs} - V_{thsb})V_{ds} - n\frac{V_{ds}^2}{2}\right)$$

Saturation voltage

$$V_{ds} = \frac{V_{gs} - V_{thsb}}{n\alpha} \equiv V_{dssat}$$

$$\alpha = (1 + \frac{V_{gs}}{nE_{sat}L})$$

Saturation current

$$I_{dssat} = \frac{1}{2n\alpha}\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})^2$$

Weak inversion

$$I_{ds} = \frac{W}{L} \cdot \mu \cdot C'_{ox} \cdot U_T^{\ 2} \cdot (n-1) \cdot e^{(V_{gs}-V_{thsb})/nU_T} (1 - e^{-Vds/U_T})$$

Saturation voltage

z.B. $V_{ds} > 3U_T$

Saturation current

$$I_{dssat} = \frac{W}{L} \cdot \mu \cdot C'_{ox} \cdot U_T^{\ 2} \cdot (n-1) \cdot e^{(V_{gs}-V_{thsb})/nU_T}$$

Early-effect

$$I_{ds} = I_{dssat}(1 + (V_{ds} - V_{dssat})/E_{sat}L)$$

Threshold voltage

$$V_{th} = \frac{2C'_{dep,min}}{C'_{ox}} \times V_{cont} = \frac{\sqrt{2eN_a\varepsilon_0\varepsilon_{Si}V_{cont}}}{C'_{ox}}$$

$$V_{cont} = 2U_T \ln(\frac{N_a}{n_i})$$

The following values hold in a 65 nm technology

E_{sat} for PMOS ~ 10.4 V/µm and E_{sat} for NMOS ~ 9.7 V/µm

µ(NMOS) = 2.64×10^{-2} m^2/Vs and µ(PMOS) = 1.45×10^{-2} m^2/Vs

C'_{ox} = 13.28 fF/µm^2 or 0.01328f/m^2

Capacitances in MOS structure

The depletion regions and electrodes in the MOS structure contain charge, as shown in Figure 10. The amount of charge depends on voltages between electrodes. This is reason why capacitances are formed. The relationships between the charge in depleted regions and the voltages are non-linear. So-called dynamic capacitances are defined as dQ(V)/dV in the working point. These dynamic capacitances are used for the small signal model of transistor.

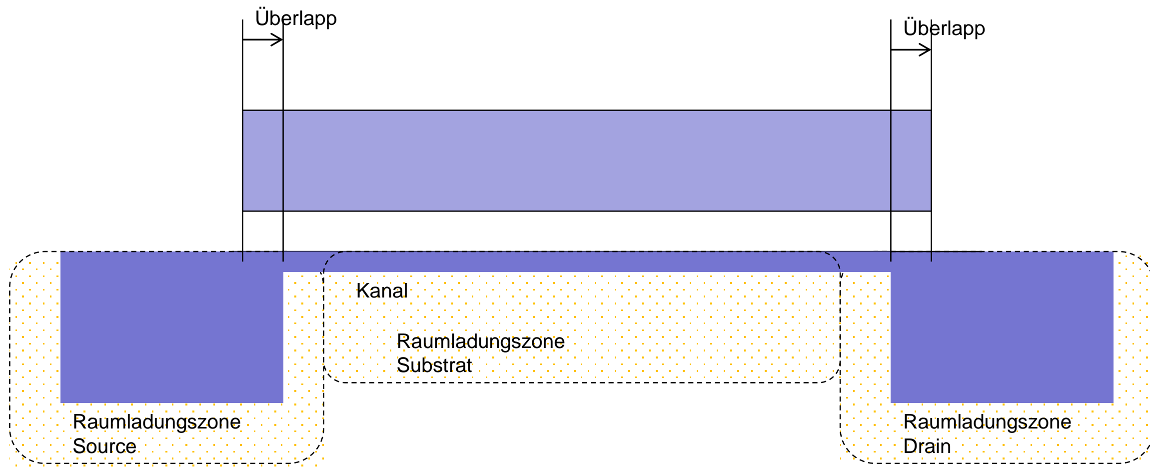


Figure 10: Regions with space charge within a MOSFET

Gate capacitance

The most important capacitance in transistor is its gate capacitance. We have already seen that there are two capacitances below the gate. The oxide capacitance $C_{ox} = C'_{ox} \times W \times L$ and the capacitance of the depletion zone $C_{dep} = C'_{dep} \times W \times L$. C'_{ox} and C'_{dep} are the capacitances per unit area. Depending on operation region, weak- or strong inversion, the gate capacitance differs.

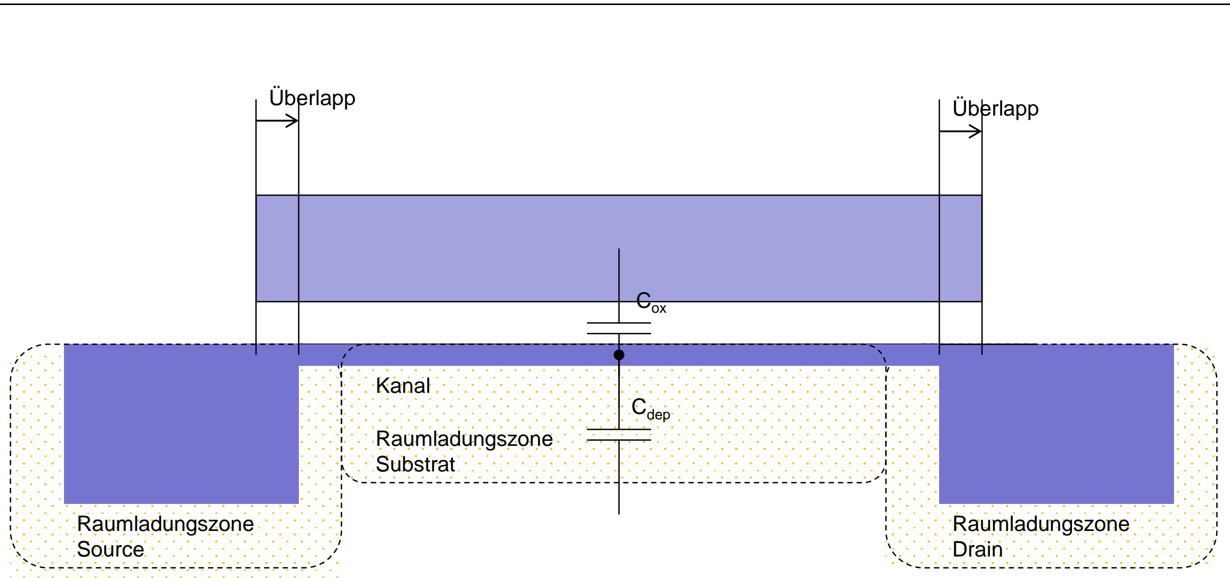


Figure 11: Gate capacitance

C_{gate} in weak inversion

The gate capacitance in weak inversion (Figure 12) is the series circuit of C_{ox} and C_{dep}

$$C_{gate} = C_{gb} = WL\frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}}$$

The gate capacitance connects gate and substrate.

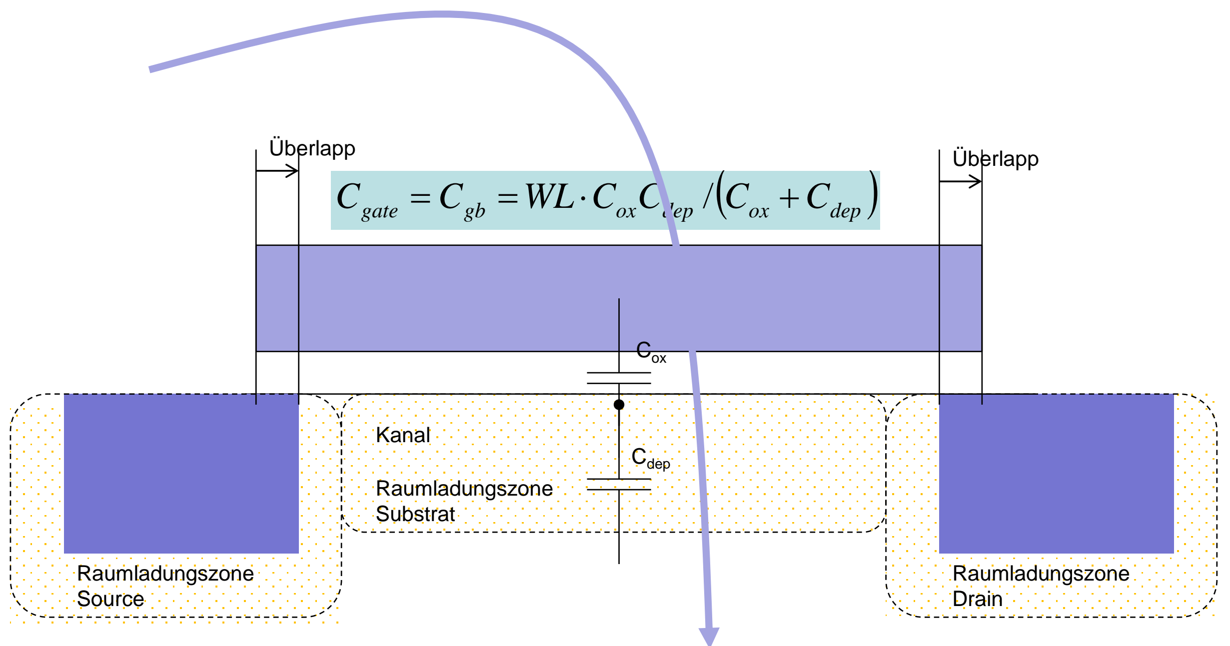


Figure 12: Gate capacitance in weak inversion

C_{gate} in strong inversion and V_{ds} = 0

The voltage between the contacts of the C_{dep} is, in strong inversion, fixed since the source and the drain are "shorted" by the channel. That's why we don't see C_{dep} when we change the voltage at the gate. The charge amount in the depletion zone does not change. Of the original two capacitances only C_{ox} remains. The gate capacitance is then:

$$C_{gate} = C_{gsd} = WLC'_{ox}$$

The gate capacitance is therefore larger than in weak inversion.

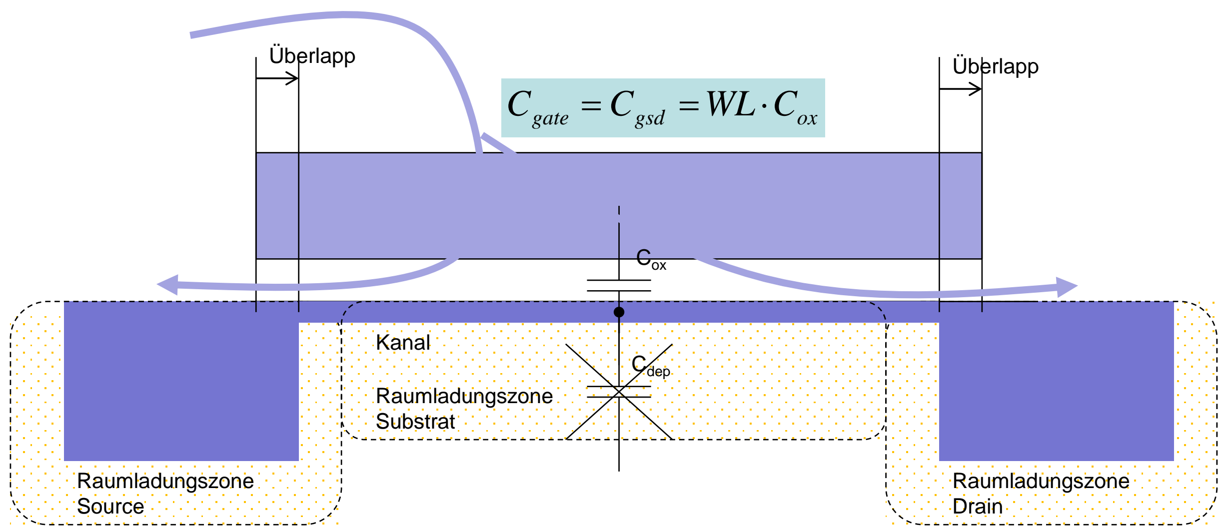


Figure 13: Gate capacitance in strong inversion for $V_{ds} = 0$.

C_{gate} in strong inversion and saturation ($V_{ds} > V_{dssat}$)

It can be shown that the charge ampunt in the channel is approximately 2/3 from that for $V_{ds} = 0$. Therefore, the gate capacitance is approximately:

$$C_{gate} = \frac{2}{3} WLC'_{ox}$$

If we have $V_{ds} > V_{dssat}$ (saturation), the channel is detached from drain. As consequence of this, the gate capacitance only applies between gate and source.

$$C_{gate} = C_{gs} = \frac{2}{3} WLC'_{ox}$$

There is no capacitance between drain and gate, as Figure 14 shows.

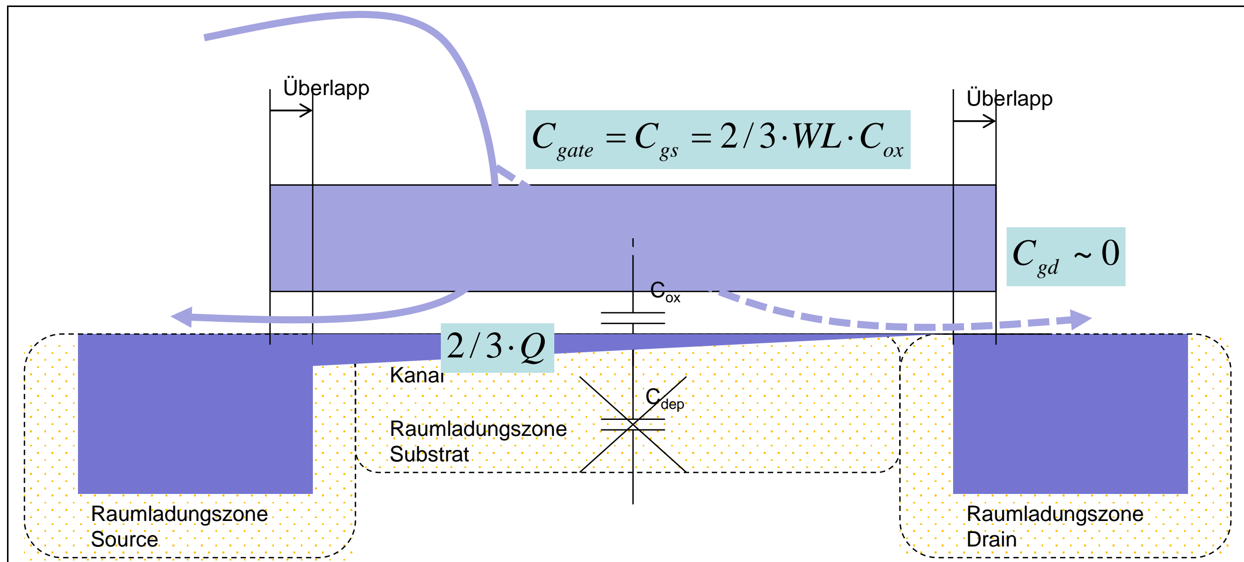


Figure 14: Gate capacitance in strong inversion for $V_{ds} > V_{dssat}$.

In addition to gate capacitances, we have the following smaller capacitances:

PN junction capacitances (junction capacitances) C_{jd}, C_{js}.

Overlapping capacitances $C_{gs,ovl}$ and $C_{gd,ovl}$. These capacitances are created because the source and drain areas extend partially under the gate oxide gate.

The drain gate capacitor $C_{gd,ovl}$ is especially important because it intruduces feedback between transistor drain and gate. Drain is usually the output and gate the input of an amplifier.

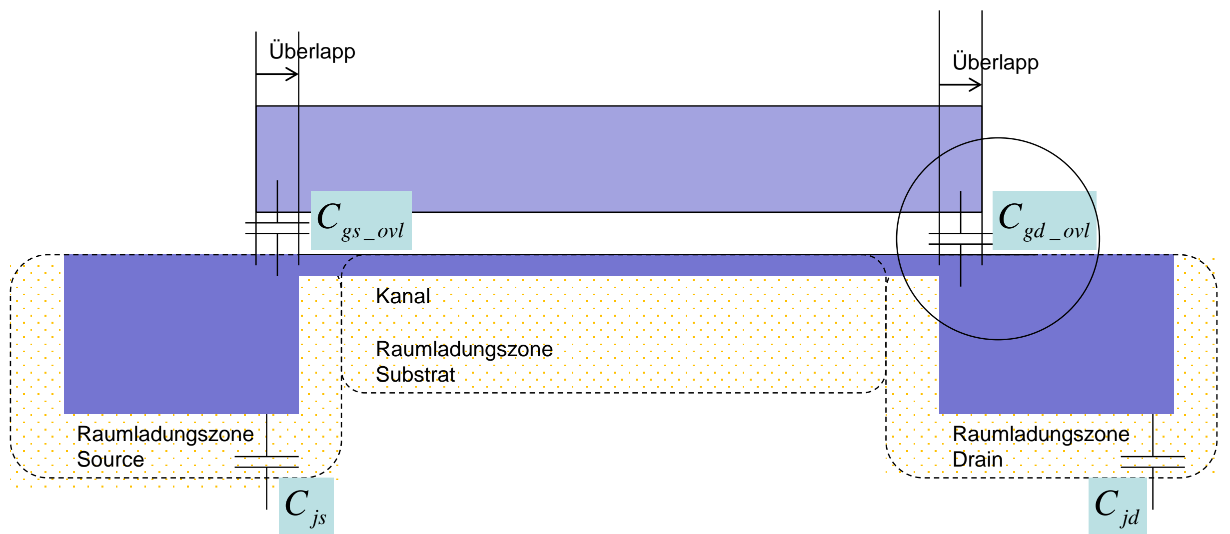


Figure 15: Additonal capacitances

Small signal model of an MOSFET

Figure 16 shows the full small signal model of an MOSFET.

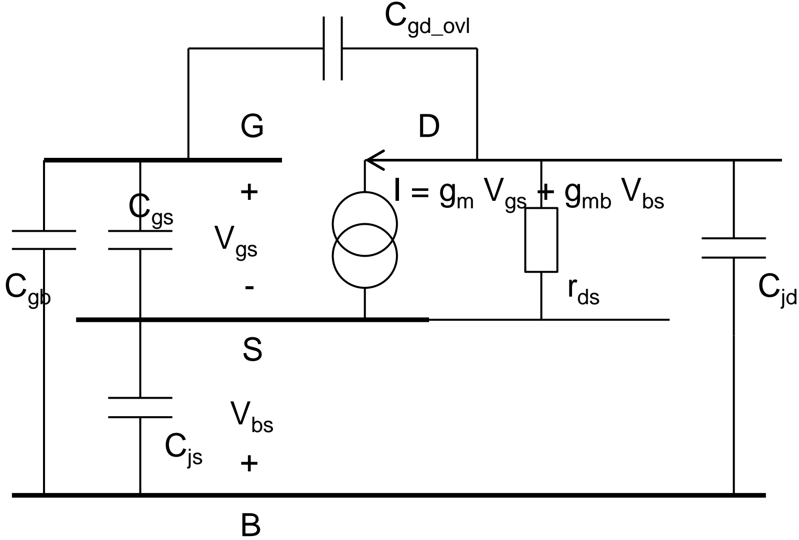


Figure 16: Small signal model of a MOSFET