Lecture 1

Our group, the ASIC and Detector Laboratory (KIT-ADL) https://adl.ipe.kit.edu/english/, develops microchips for scientific and medical applications, for example for detectors at the particle accelerators, and for 3D ultrasound tomography or ion therapy.

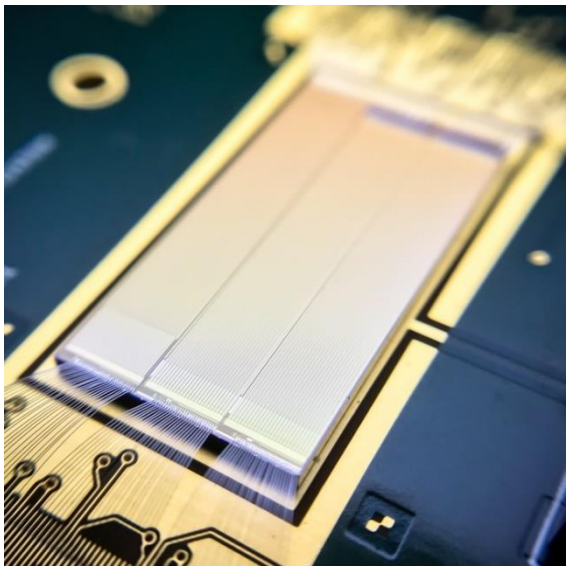


Figure 1: CMOS pixel sensor developed at KIT-ADL

Analog Circuit Design

The topic of the course DAS is the design of integrated analog circuits in CMOS technology.

The course includes *lectures* and *exercises (practical part)*. In the **exercises**, we will use chip design software to design circuits. We start with the simple circuits, which are then combined and extended. At the end, an analog-to-digital converter is designed.

The themes of the lectures are: CMOS semiconductor technology and transistors, analysis of circuits with feedback. CMOS amplifiers: starting from simpler circuits such as the common source amplifier to multi-stage, differential and switched amplifiers. Analog-to-digital converters.

No special previous knowledge is required for this course.

As supplementary literature, I recommend the following book:

"Design of Analog CMOS Integrated Circuits" by Behzad Razavi

https://primo.bibliothek.kit.edu

Introduction: CMOS

The circuits in this course are based on CMOS technology. CMOS: complementary metal oxide semiconductor.

CMOS integrated circuit is one of the most important inventions of the 20th century. CMOS has enabled powerful microprocessors and computers. It was invented by F. M. Wanlass in 1963. https://patents.google.com/patent/US3356858A/en

CMOS ICs developed in past 50 years with exponential speed – the number of transistors on microchips doubles every two years. This trend continues till now, it is called Moores Law.

More about the development of semiconductor technology can be found in the document DAS_2021_1_ZusThema_EntwicklungHalbleiter

(ILIAS or https://adl.ipe.kit.edu/english/28.php)

Interesting TV documentaries

- Die Silicon Valley-Revolution: Wie ein paar Freaks die Welt veränderten Doku (2017) – YouTube
- (The Silicon Valley Revolution: How a Few Nerds Changed the World | Netflix)
- Silicon Valley (1): Die Geschichte der "Fairchild Eight" – YouTube
- [Doku] Silicon Valley - 2 - Vom Halbleiter zum Mikroprozessor (HD) – YouTube

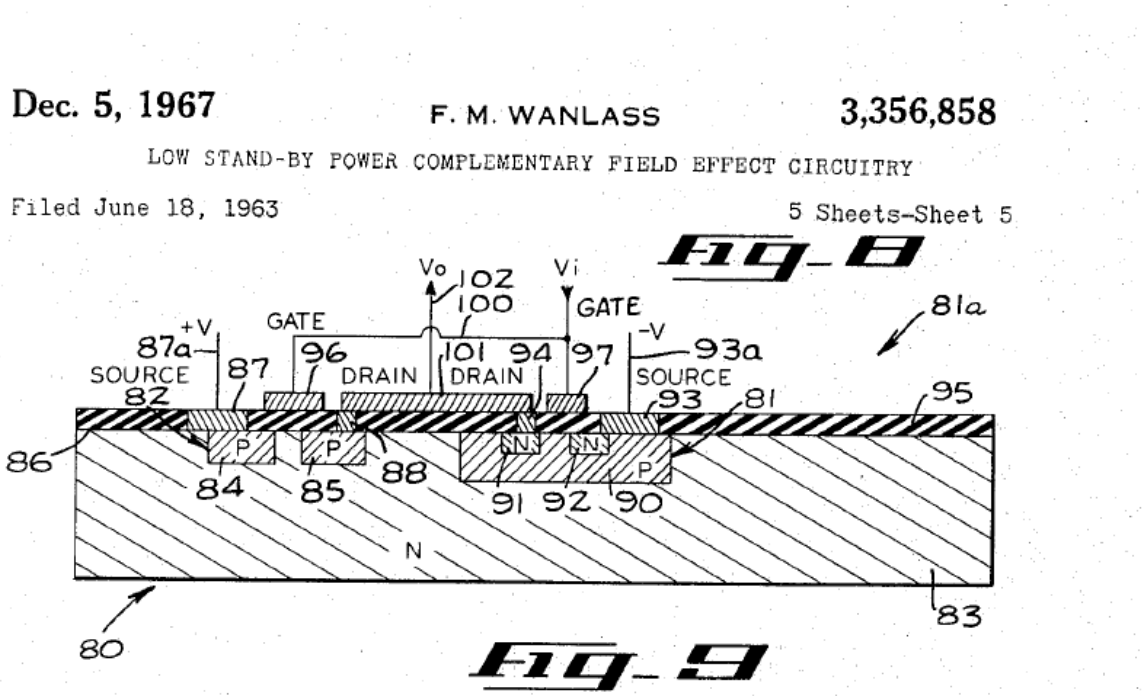


Figure 2: Drawing from the CMOS patent of F. N. Wanlass

CMOS technology is especially suitable for digital circuits: CMOS components based on field-effect transistors (FETs) are small and consume little amount of power.

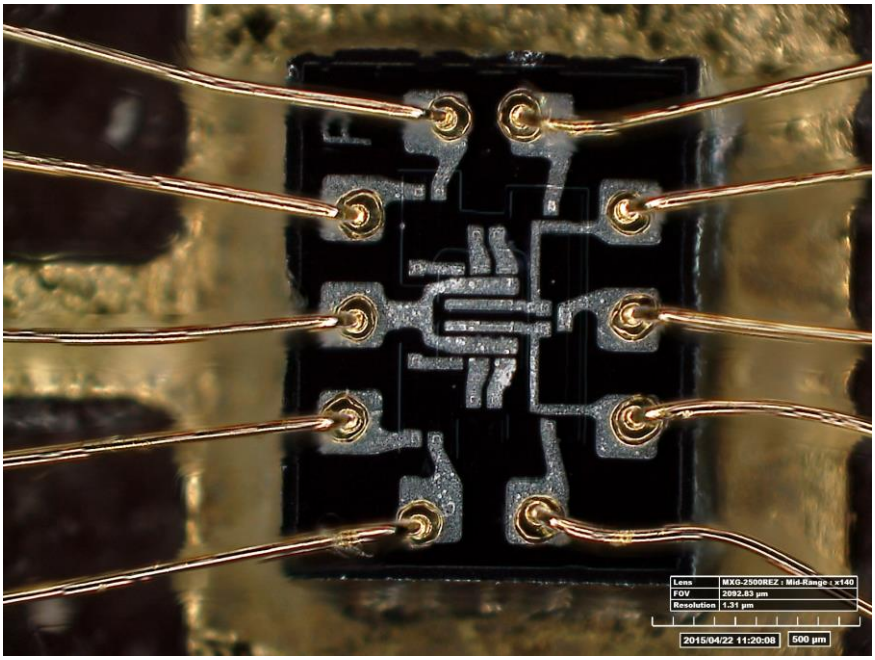


Figure 3: One of the first integrated circuits.
https://airandspace.si.edu/stories/editorial/apollo-guidance-computer-and-first-silicon-chips

Chip Manufacturing

This section gives a short overview of the production of CMOS integrated circuits. Microchips are produced on the silicon wafers in a process similar to the printing of images (lithography).

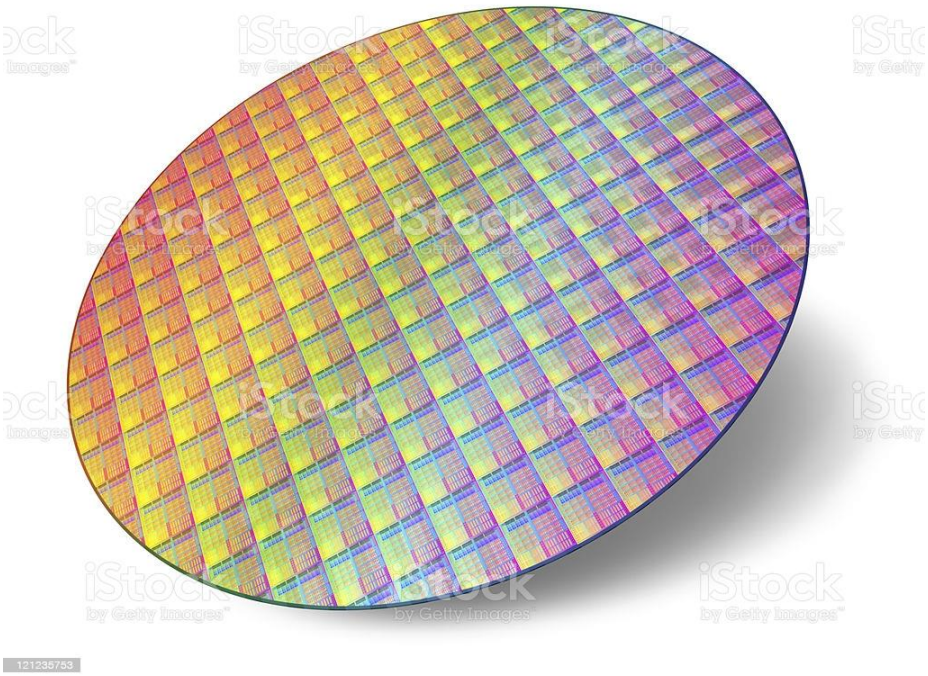


Abbildung 4: Wafer mit Recticles

The wafers typically have a diameter of 200 mm or 300 mm.

The layers of the chip: 1. silicon regions (mono- and polycrystal), 2. insulators (SiO_2, and other materials), 3. Contacts (Vias) (Tungsten, Al), 4. Metal layers (Al and Cu) are produced by processes such as epitaxy, chemical deposition and oxidation.

The layers are structured by etching (wet- (chemical), plasma- and ion-etching). Photoresist is used to protect the areas that should not be etched.

Photoresist is structured (exposed and then developed) with UV light, the template for this structuring is called a mask.

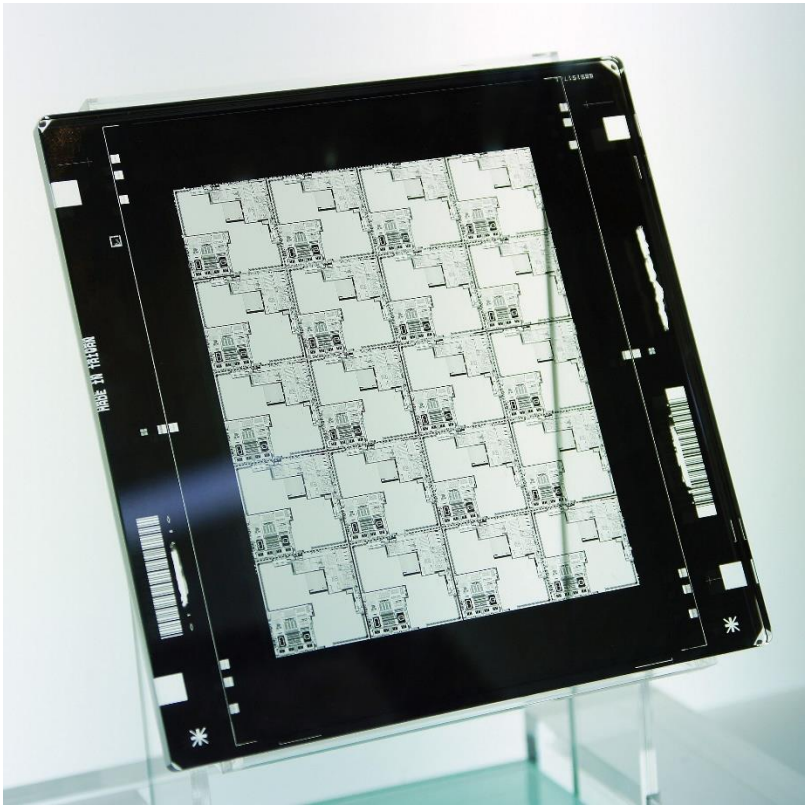


Figure 5: Mask for photolithography. https://en.wikipedia.org/wiki/Photomask

Silicon regions are doped by diffusion or ion implantation. Also, here, the stencils (e.g. made of SiO_2) are used, which are structured with the photoresist.

The production of a wafer requires about 400 individual steps and at least 30 masks. The masks are made with the help of projectors (steppers) with e.g. 4x reduction projected onto silicon. A well-known manufacturer of equipment for Photolithography is ASML (Netherlands).

Figure 6: Stepper (Projector) https://www.asml.com/en/products/duv-lithography-systems/twinscan-nxt2000i

The size of the image is limited to about 2.5 cm x 2.5 cm. It is the maximum size of a chip. We call the image of the mask the *reticle*. On a wafer, the mask is projected several times (typically >50 times) with a fixed offset, so that we have several identical reticles.

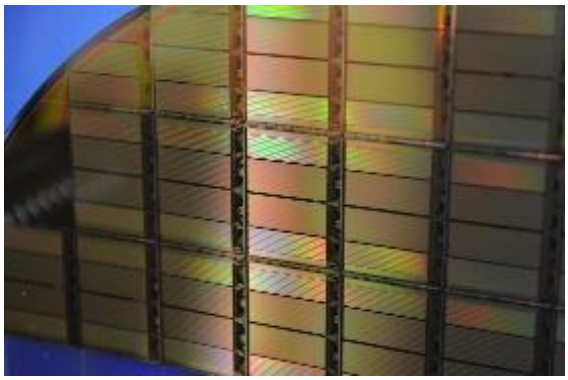


Figure 7: CMOS Wafer (KIT-ADL)

Several chips are often placed in the reticle.

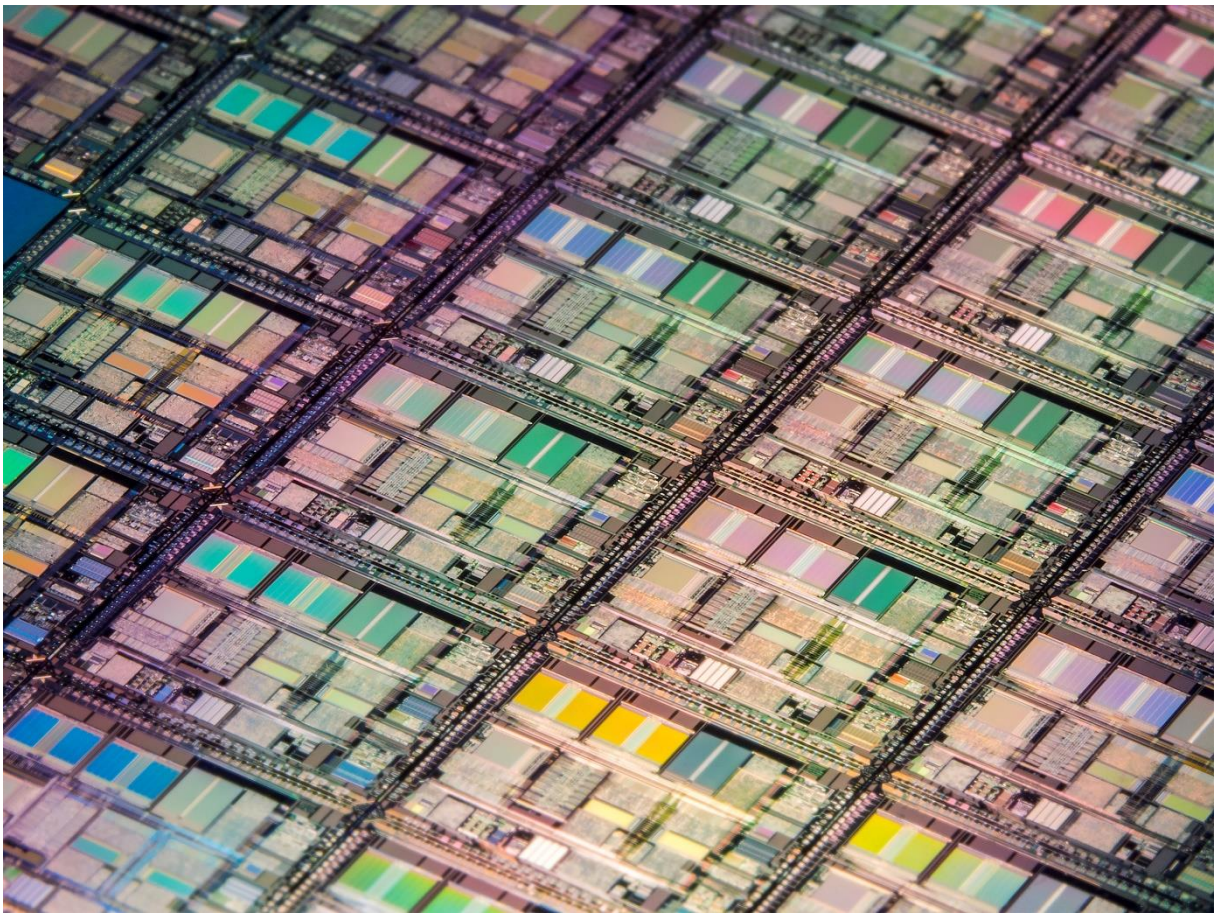


Figure 8: Reticles with chips. *https://www.renishaw.com/en/advanced-position-encoders-in-photolithography--42654*

Literature

https://de.wikipedia.org/wiki/Stepper_(Halbleitertechnik)

https://www.halbleiter.org/chipfertigung/

Youtube Lecture:

How Photolithography works | Part 1/6 – Introduction – YouTube

till

How Photolithography works | Part 6/6 – Resolution Enhancement - YouTub

The technical drawings of mask layers are called the layout.

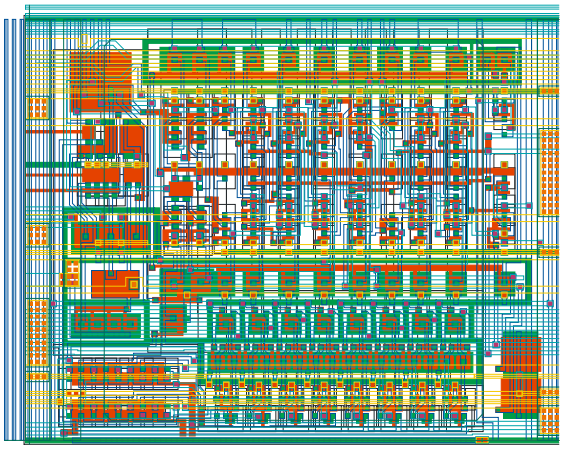


Figure 9: Layout

Chip Design

Chip design is a process that begins with the specification of an electronic device and ends with the layout design. The chips are then manufactured by a chip manufacturer (foundry). They are integrated into a system (chip packaging), characterized and, if necessary, a new version is designed.

Specification of a chip is important task. It is useful to sketch a circuit "on paper" and to calculate important values approximately before starting using software tools. That is why in this course we explain different methods for circuit analysis without software.

Software Tools

Analog chip design is done with CAD software. We use the program package Cadence (https://www.cadence.com) in this course. Cadence includes many program tools.

Circuit and Layout Editor (Virtuoso)

Simulator (INCISIV and MMSIM)

Verification of the layout (Assura)

Layout versus Schematics (Assura LVS) and Design Rule Check (Assura DRC)

We also need the transistor models, already made design blocks, DRC rules. These data are provided within a design kit.

Cadence requires licenses. The license fees are higher for commercial use. Universities pay less when Cadence is used for teaching or research projects.

Chip Manufacturers and Technology Processes

At the beginning of design process the most suitable chip manufacturer should be chosen. The most famous manufacturers are: TSMC, UMC, Globalfoundries. In Germany they are: X-Fab, Lfoundry. Our group works with AMS, Lfoundry, IHP, X-Fab…

Each manufacturer often offers several processes.

This can be e.g. a logic CMOS process, a CMOS technology with extra components for analogue design or for optical sensors, it can be a high-voltage CMOS (HVCMOS) process, an SOI- or a BiCMOS process.

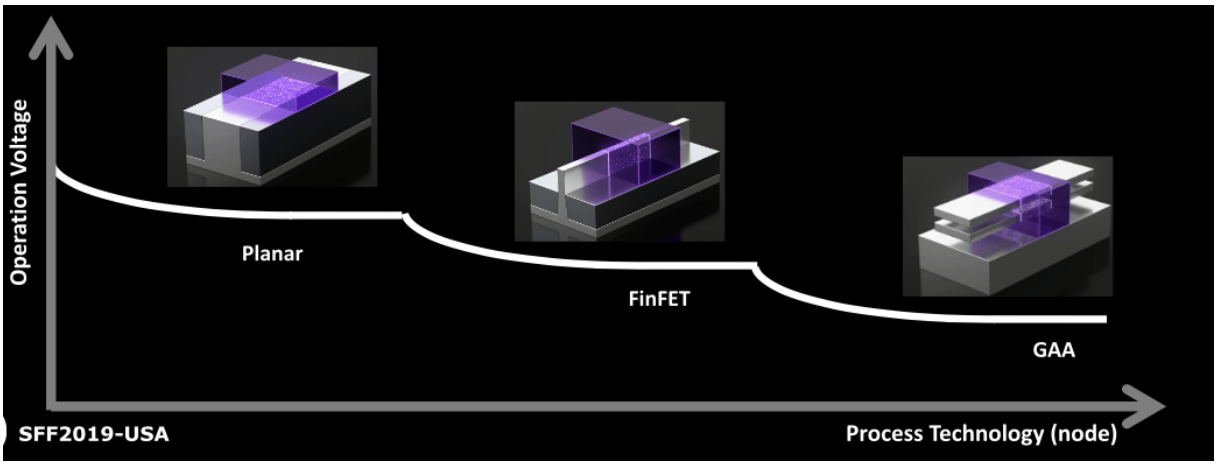
The latest are FinFET, Fully Depleted SOI or nanowire Gate all around processes.

All processes are also classified by structure size in process nodes, e.g. 0.35µm, 0.18µm, 0.13µm, 0.11µm, 90, 65, 55, 40, 28, 22, 16, 12, 7, 6, 5nm.

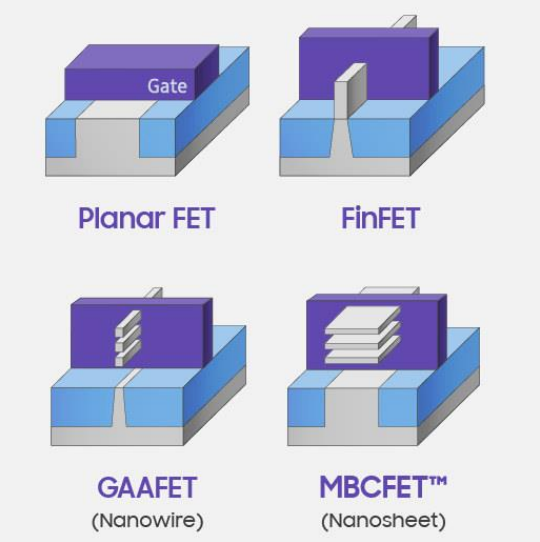
https://de.wikipedia.org/wiki/Technologieknoten

Smaller processes are more modern, more expensive, and analogue design is more difficult

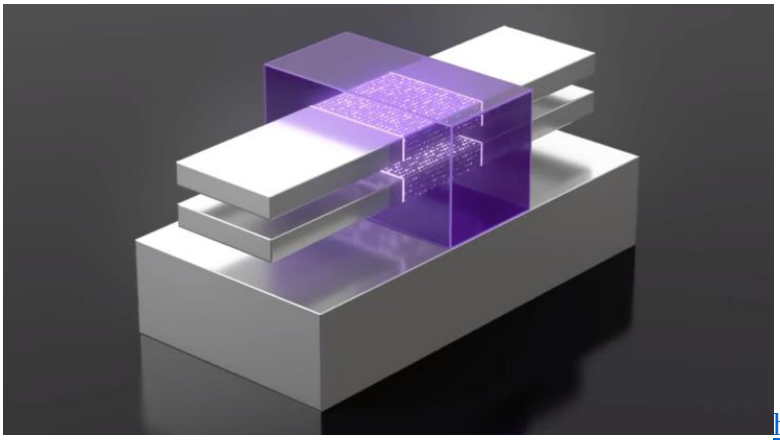
The process node size refers to minimum feature size (gate length) in a planar process. In the case of a non-planar process, the size in nm refers to the gate length of an imaginary planar transistor which would take the same are.



https://semiengineering.com/5nm-vs-3nm/



https://www.cnx-software.com/2019/05/17/mbcfet-process-technology-3nm-processors/



https://wccftech.com/samsung-announces-3nm-mbcfet-process-5nm-production-in-2020/

Figure 10: Different types of transistors

Europractice

Some foundries can be contacted directly. Some only work directly with larger clients. There are organisations that mediate between smaller clients and foundries – one is Europractice. https://europractice-ic.com/
Europractice represents chip manufacturers and offers support. KIT is an Europractice member. For smaller quantities and smaller chips, it does not make sense to have the entire mask set manufactured. In a 180 nm process, the price of a mask set is ~100 k€. Europractice offers Multiproject Wafer (MPW) runs.

https://europractice-ic.com/mpw-prototyping/general/mpw-minisic/
Here, many customers share the reticle space. A customer then gets about 40-100 chips at a price starting at about 1 k€/mm2 area (example 180 nm technology).

Design-Kit

Once we have chosen a process, we need simulation models and the layout rules. We need special libraries that can then be integrated into the chip design software, e.g. Cadence. Such a library with technology files is called the process design kit - PDK.

(Transistors are different in every process and the transistor models are complicated. An example of a MOSFET model is BSIM.)

Design-Flow

The sequence of design steps is referred to as the design flow.

We distinguish between the analogue and digital design flow.

The design steps are shown in the figure.

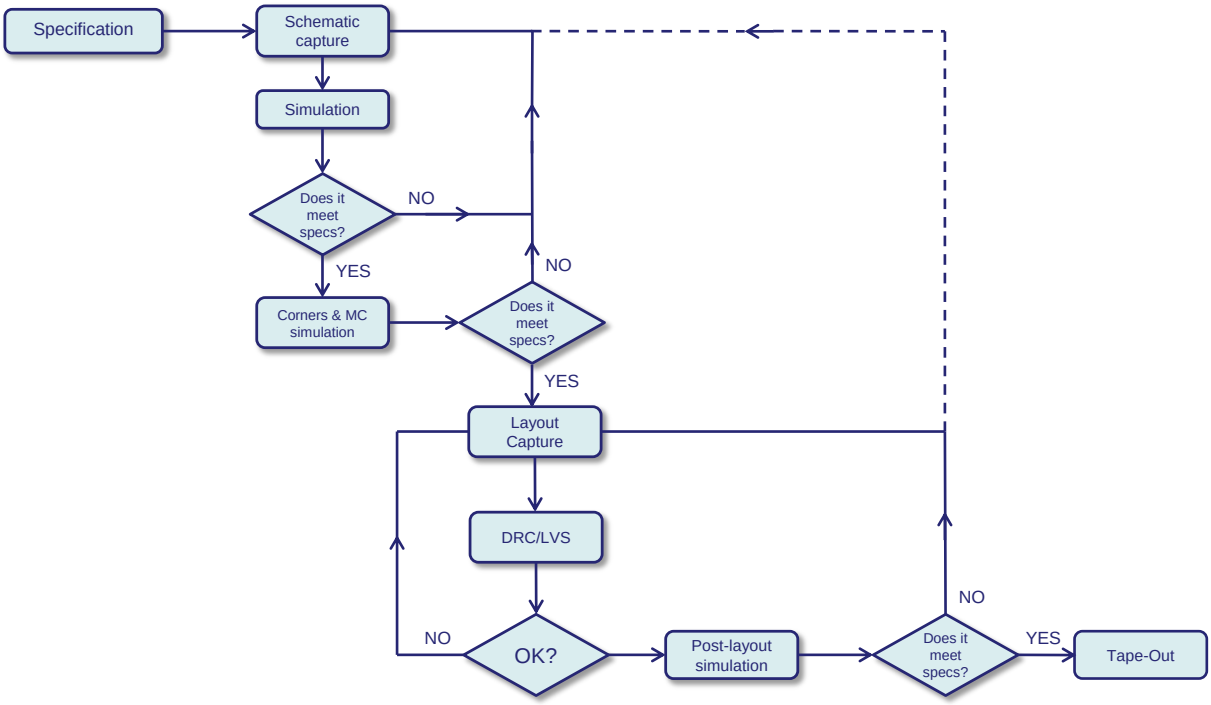


Figure 11: Design Flow for Analog Circuits

Schematic

In analogue design flow, the first step is schematic design. The schematic is drawn using the schematic editor. The basic component is a transistor. We sometimes also use capacitors, resistors and diodes. Candence supports the modular structure of circuits. You can generate a symbol from each schematic. This allows the use of this circuit in other schematics. To generate a symbol, inputs and outputs must be defined. A symbol has the same inputs/outputs as its schematic.

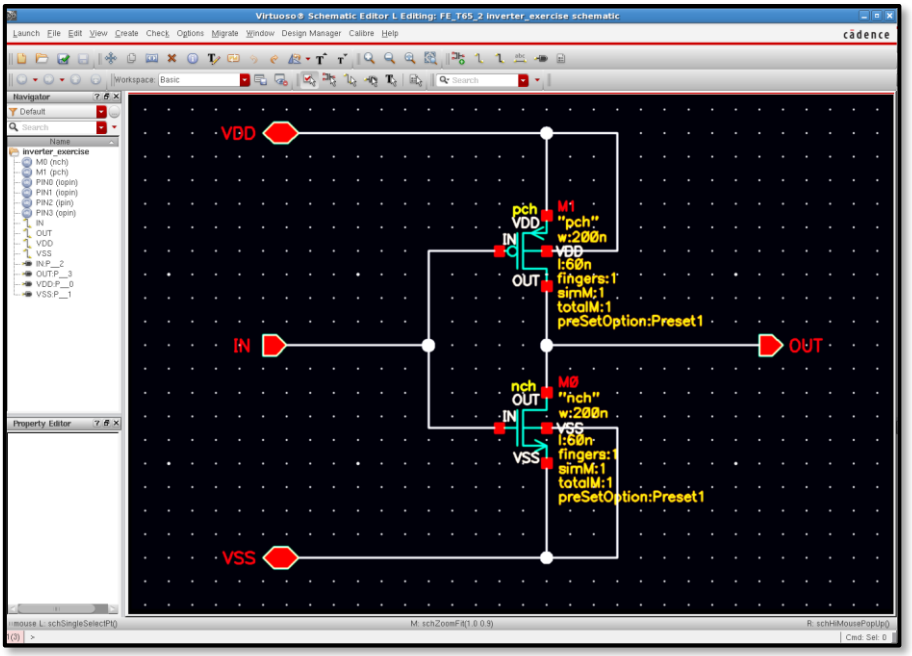


Figure 12: Schematic Editor

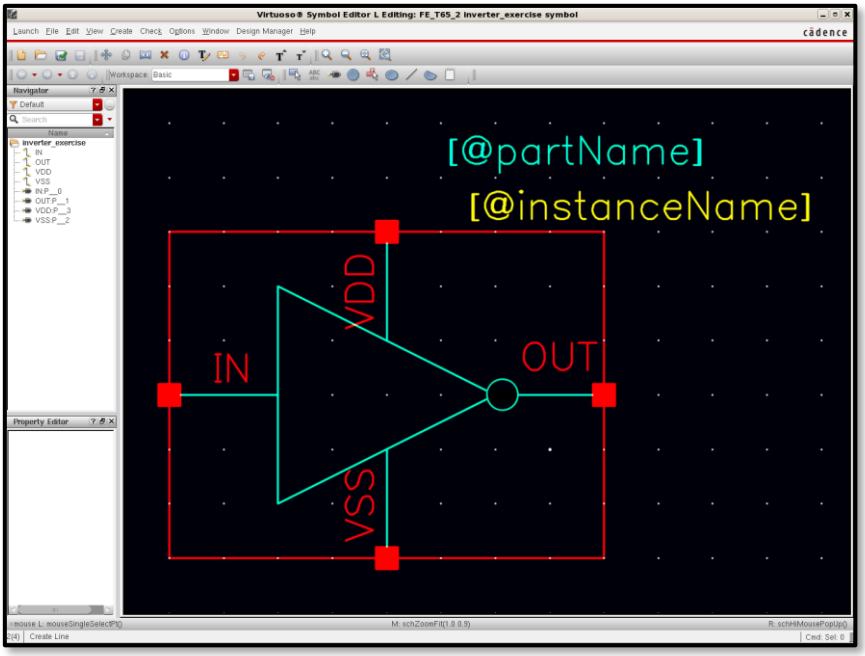


Figure 13: Symbol

Simulation

The circuit can be simulated. There are three main simulation tools – for analogue, mixed mode or digital simulation. The analogue simulators can do DC-, AC- or large signal analysis in the time domain (transient simulation).

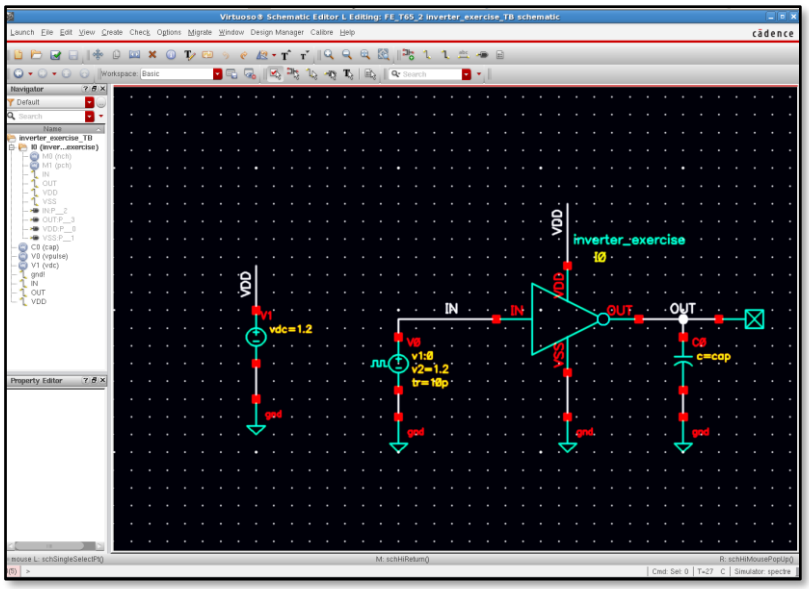


Figure 14: Test bench for analogue simulation

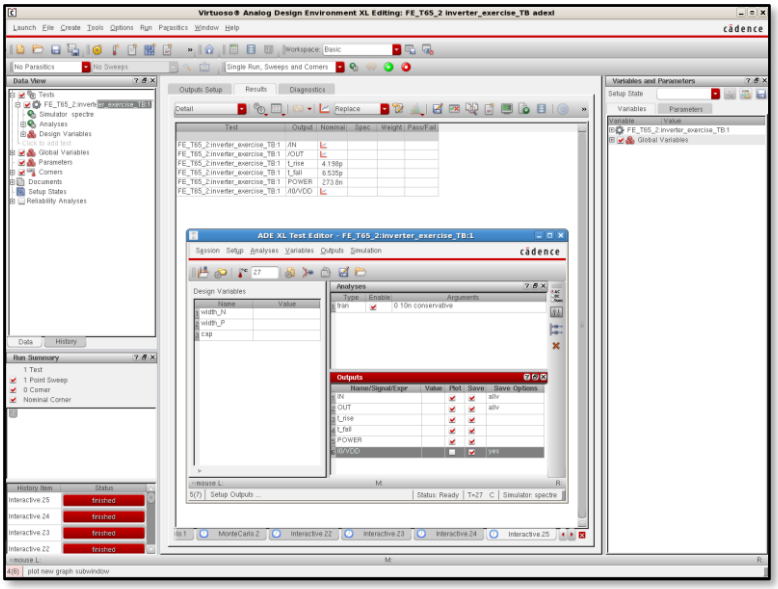


Figure 15: Analog Simulator GUI

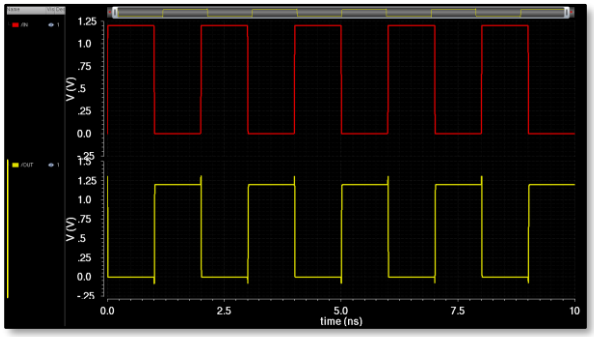


Figure 16: Result of a transient simulation

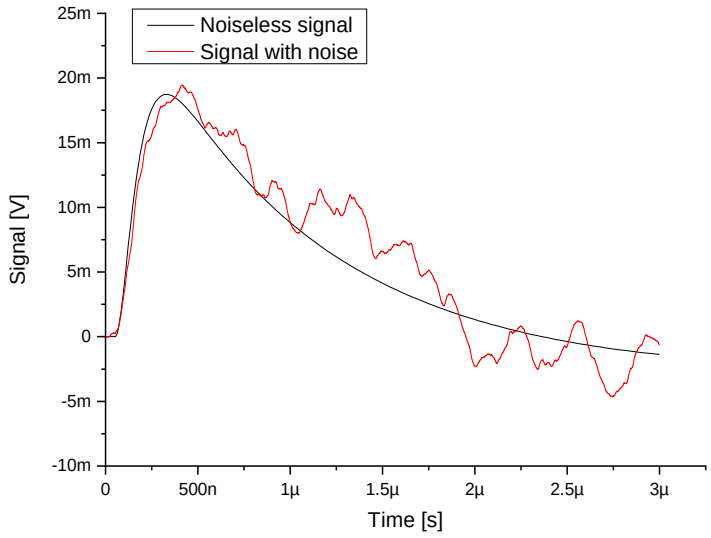


Figure 17: Noise Simulation

It is possible to simulate the noise in the frequency and time domain. Further, it is also possible to simulate parameter fluctuations.

Noise: We look at a component. We investigate how currents and voltages change in time in the absence of signals because of the thermal movement of electrons or electron trapping.

Mismatch: We look at several identical components. We investigate statistical variation of currents/voltages from component to component.

Layout

When the simulation results meet the specifications, the layout is made. The layout consists of several drawings. These represent the mask layers used for the production of transistors and metal layers.

Layout is drawn using the layout editor. This editor resembles somewhat a usual drawing program, where you can draw polygons, paths and other objects.

There are however many additional options.

For instance, it is possible to build a hierarchy.

For example, you can group the structures and use them as a block.

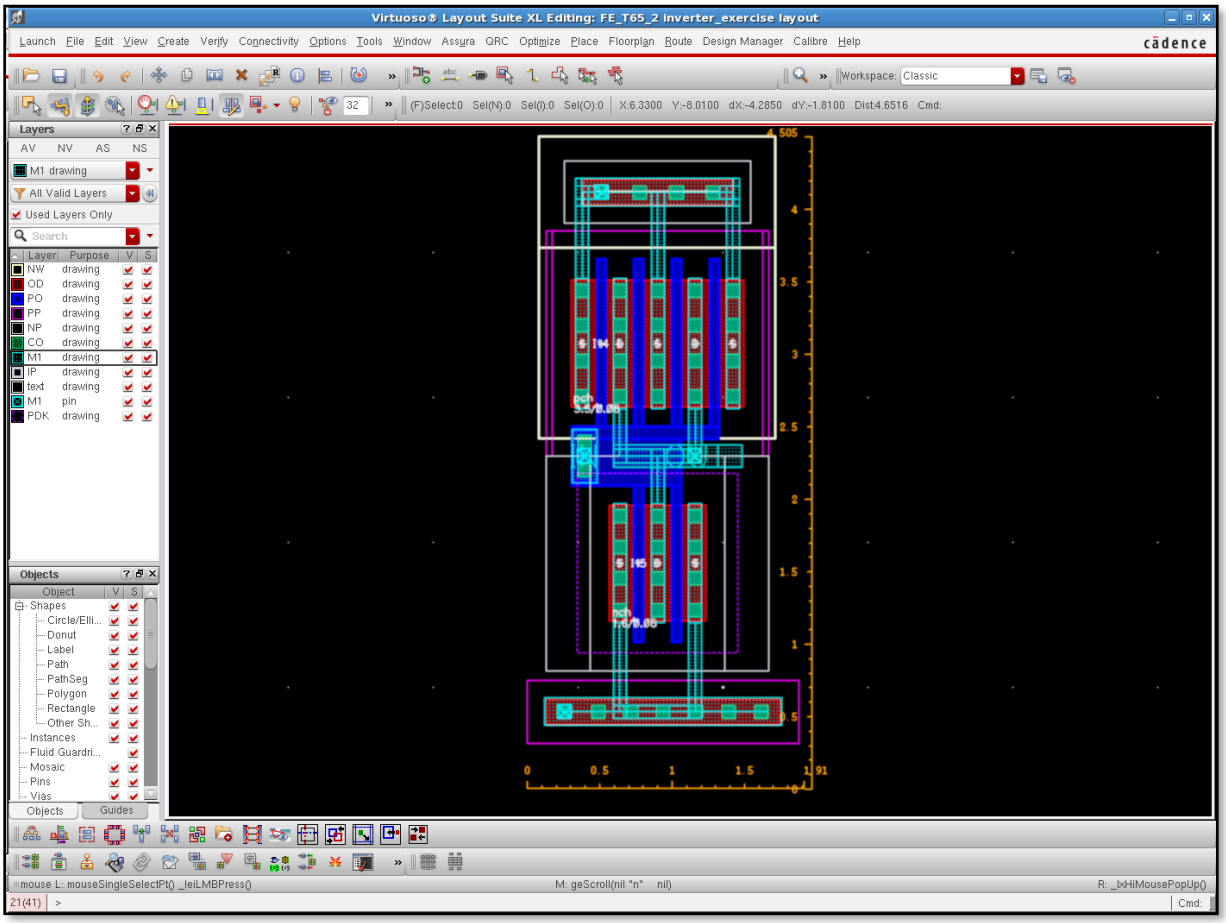


Figure 18: Layout Editor

This block in the layout software is similar to an object (instance) of a class in a programming language. You can have many instances (objects) of the same kind in a design. In cadence, these "classes" are called cells. A cell has different views. For example, there is schematic view or layout view.

A semi-automatic generation of a layout from a schematic is also possible.

Layout rules have to be met – e.g. the transistors must not be smaller than the technology allows. It is possible to check whether the design meets the rules. This check is called DRC (Design Rule Check).

It is also possible to extract the schematic from a layout in the form of a netlist. This allows the tool to check whether a layout corresponds to its schematic. This is called LVS – Check (Layout versus Schematics)

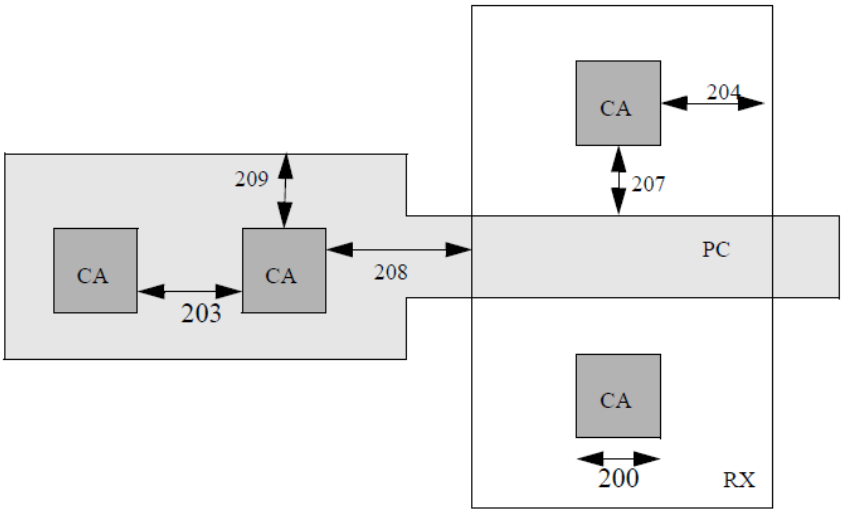


Figure 19: Design Rules

Circuit Design

Proper structuring is helpful in circuit design. Almost every analogue circuit is based on a few basic components. The examples are the common source amplifier, the source follower, the cascode (the common gate amplifier), the current mirror and the differential amplifier. These basic components consist of transistors. The more complex circuits, such as operational amplifiers or analogue-to-digital converters (ADCs), consist of basic components. The systems consist of circuits.

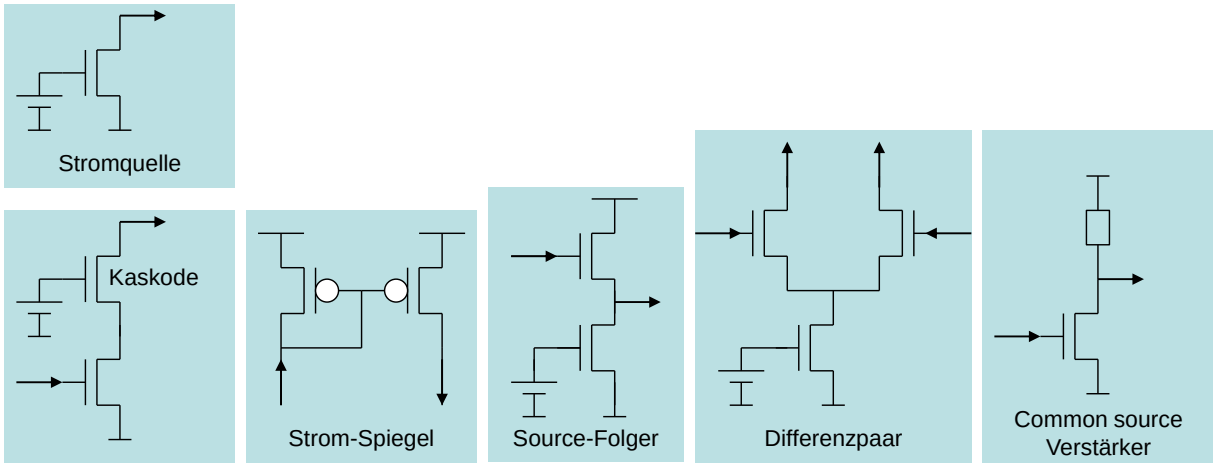


Figure 20: Basic Components

Structure of a microchip

A chip consists of many circuits that are connected with each other.

The use of cells and instances in cadence allows us to use the same circuits multiple times. Schematics and layouts have the same hierarchical structure.

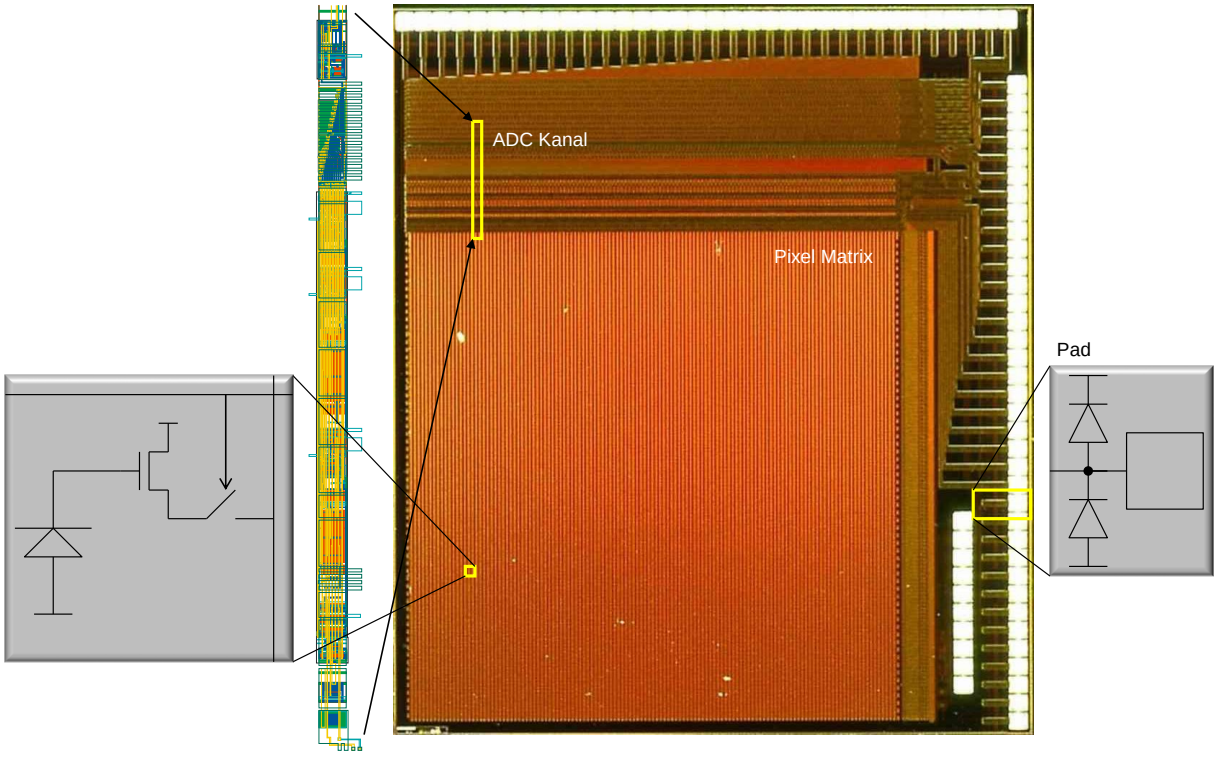


Figure 21: Photo of a CMOS pixel sensor with important circuits

Let us take a pixel sensor as an example. The sensor is based on diodes.

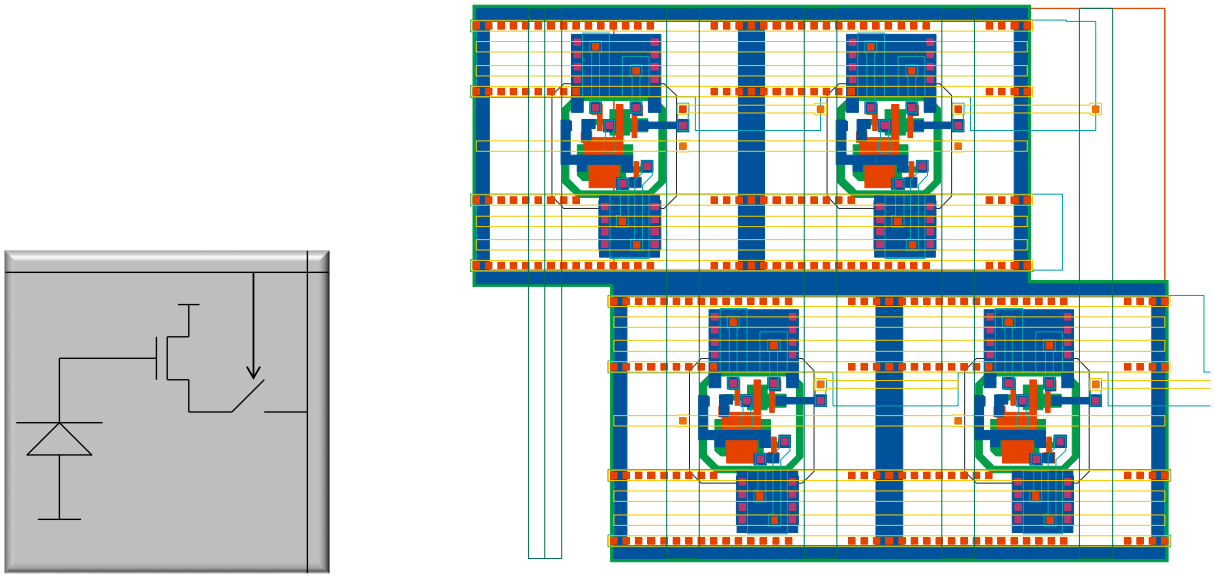


Figure 22: Pixels Schematic and Layout

Pixel

The amplifiers in pixels are based on the simple components – e.g. a source follower.

Hierarchy

The pixels are organized in columns, and the columns form a matrix. Such intuitive hierarchy is used in the schematic and the layout. Therefore, we can first design a pixel as a circuit, then simulate it, draw the layout, and do DRC/LVS checks. Then we build a column and the whole matrix. It is better to reduce the number of different layouts and schematics (number of "classes" or cells) in a design. Why? If we change something later in the pixel layout, the change will be done in each pixel cell and we do not have to do it multiple times.

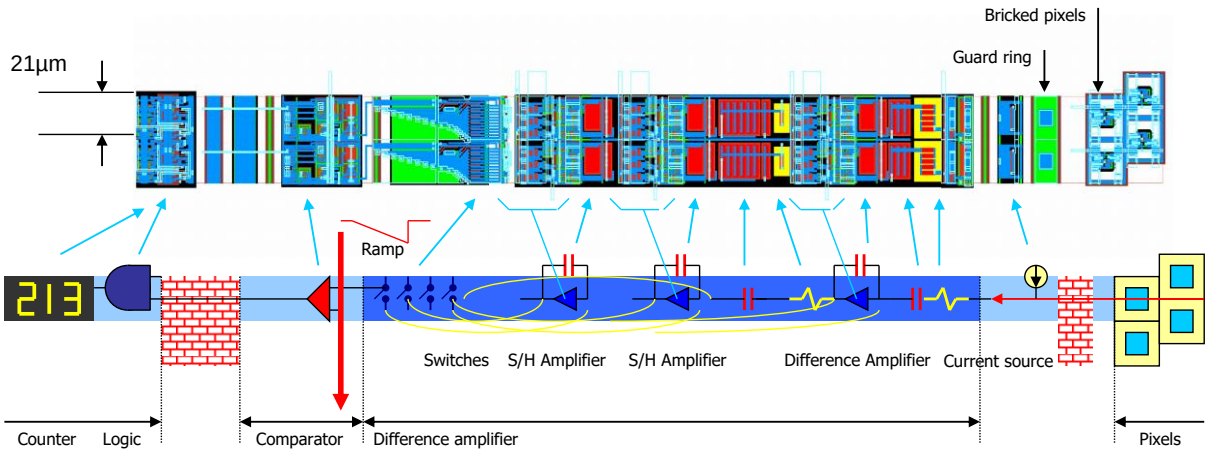


Figure 23: Readout Electronics – Layout and Block Diagram

ADC

The sensor chip contains the ADCs, which digitize pixel signals. (One ADC per column.) These ADCs are located on the chip periphery. ADC is a system of several components – e.g. amplifier, comparator, DAC, a digital circuit for control.

Digital circuit

Often there is also a digital circuit that receives and processes the ADC signals and sends them out of the chip in a proper format. The digital components consist of standard logic cells (flip-flop, AND, ODER, etc.). These are often provided by companies. You can either assemble a digital circuit "by hand" from these components or design it with a synthesis tool from the HDL code. The chips, which contain both analogue and digital components, are called mixed-mode chips (mixed-signal chips). Mixed-signal simulation is also possible, where the analogue circuits are simulated with analogue simulators (equations are solved numerically), while the digital circuits are simulated in digital way. The simulators contain the interfaces between the digital and analogue blocks which transfer binary signals (0 and 1) into physical signals (voltages).

Pads

A chip also has the IO (input-output) contacts (pads). These pads are connected to a printed circuit board or chip package using machines “wire bonders”. The chip pads contain so-called electrostatic discharge (ESD) protection circuits. They protect against overvoltage, which can damage gate oxide.

Analog circuit design

Design of analogue integrated circuits is similar as design of circuits with discrete components

There are some differences: When designing discrete circuits on a printed circuit board, we should choose the right one from thousands of commercial components. In analogue CMOS chip design, most circuits are based only on two components: the NMOS and the PMOS field-effect transistor. MOSFET is a versatile component: it can be used as an amplifier, current source, resistor, capacitor, switch and a diode. It is therefore important to know the transistor behaviour and modelling. Another speciality of IC design is that a resistor and a diode are rarely used. The quality of normal resistors on a chip is quite poor – their values fluctuate up to +-10%. The diodes in the forward direction can induce a short circuit (the latchup effect). On the other hand, capacitors in the CMOS have good quality and precise capacitance. For this reason, resistors are often replaced by capacitors. The diodes are replaced by transistors.

Often the analogue components on a CMOS chip are not as good as the analogue circuits in a customized technology. For instance, a CCD sensor is better in terms of signal-to-noise ratio than a CMOS sensor. The amplifiers in bipolar technology may be faster or less noisy than the CMOS amplifiers. However, CMOS chips have the advantage that they can also contain digital circuits. These circuits can correct the errors due to imperfect analogue processing. This can compensate for the disadvantages of CMOS circuits. One example is the CMOS pixel sensor. By implementing circuits for readout and image processing on the chip where the pixel matrix is located, better image quality is achieved than with CCDs (despite of worse senor matrix).