Lecture 10 and Lecture 11

The topic of the lecture 10 and 11 are the amplifiers with two amplifying stages.

We will present two application examples: the voltage amplifier and the linear regulator

Implementation of the voltage amplifier with a single-stage amplifier

Implementation of the voltage amplifier/linear regulator with two-stage amplifier - generic circuit

Step response

Condition for aperiodic response

Nyquist stability criterion

Voltage amplifier with two amplifier stages with and without frequency compensation

Linear low dropout regulator (LDO regulator) implemented with a two-stage amplifier with frequency compensation

Miller effect

Integrator

Lecture 10

Two-stage amplifiers

In the previous lectures, we presented, among others, the common source amplifier and the operational amplifier with current mirror. Both amplifiers have a voltage-controlled current source in their small-signal model (Figure 1, top). This current source can be converted into a voltage source, as shown in Figure 1, bottom.

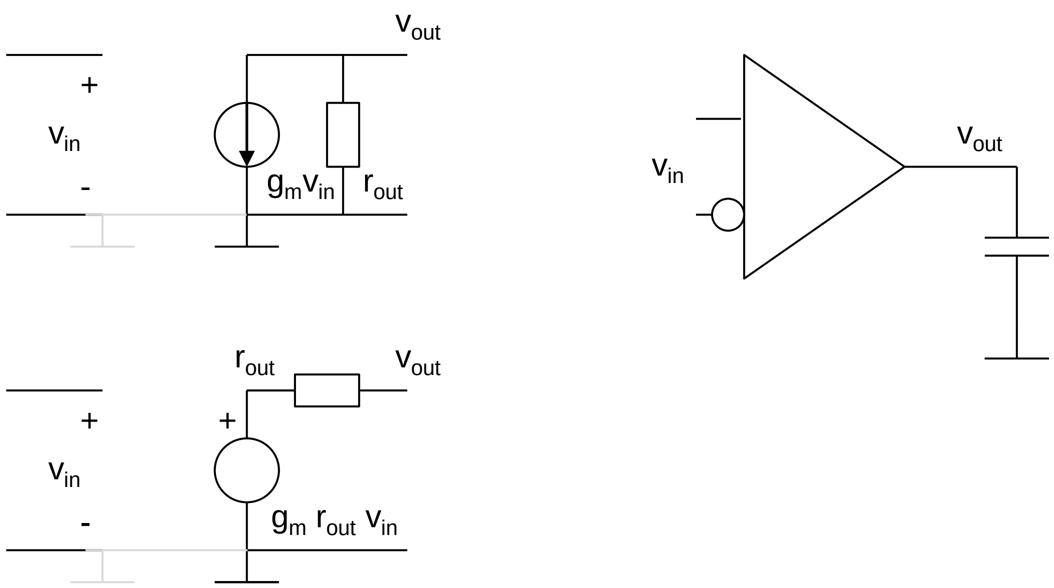
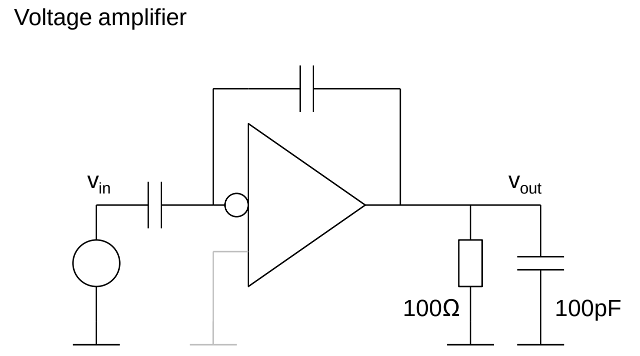


Fig 1: Single-stage amplifier, small signal model with current source (top), small signal model with voltage source (bottom) and symbol (right)

Since the small signal model contains a single voltage controlled source, we call these amplifiers single-stage amplifiers.

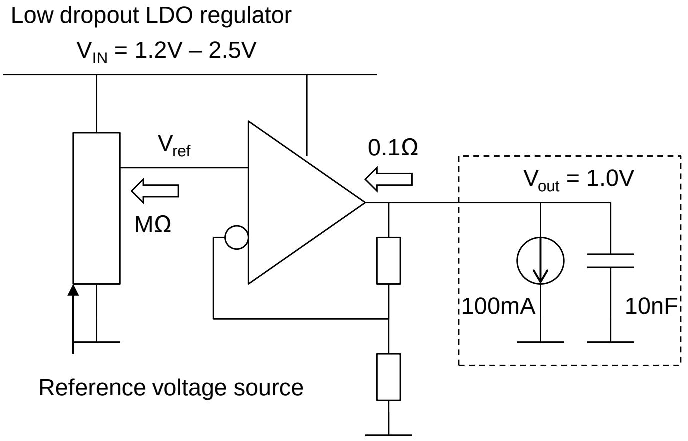
A single-stage amplifier is a good choice when the amplifier has to drive a purely capacitive load that is not very large (< p F). This is usually the case when the amplifiers perform on-chip signal processing.

In this lecture we will introduce the amplifiers with two stages.



Voltage amplifier

Parameter	Wert
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20



LDO regulator

Parameter	Wert
C_{load}	10nF
I_{load}	0-100mA
r_{out}	0.1Ω

Fig 2: Voltage amplifier and linear regulator and their specifications

Let us introduce two application examples (Fig 2).

1) A voltage amplifier with feedback is to be designed. The amplifier output is connected to a chip pad and it should drive a line with a 100 Ω termination resistance. The capacitive load at the pad is 100 pF. The amplifier should have a gain with feedback (closed loop gain) of 50. The open loop gain A_{OL} should be 1000.
2) A power supply voltage VDD = 1 V for a chip should be generated from a voltage V_{IN} which is not particularly precise: V_{IN} = 1.2 - 2.5 V. (V_{IN} can be generated by a battery.) A reference voltage generator of V_{ref} = 1 V (or less) is available. This generator produces a constant voltage V_{ref} that is independent of V_{IN}. Its output resistance is high ($r_{out,\ ref}$ ~ 1 MΩ). The current consumption of the chip is 0-100 mA. The chip can be modelled with a 10 nF capacitor and a current source. We use a so-called linear regulator (low dropout LDO linear regulator) for this task. The linear regulator is based on a differential amplifier with feedback (non-inverting amplifier) and a reference voltage source. The regulator should have an output resistance of 0.1 Ω (Figure 2).

In both cases we could use a single-stage amplifier. However, this would not be the best solution for the reasons described here:

To achieve an open loop gain of 1000 we would have to use an amplifier with a folded cascode.

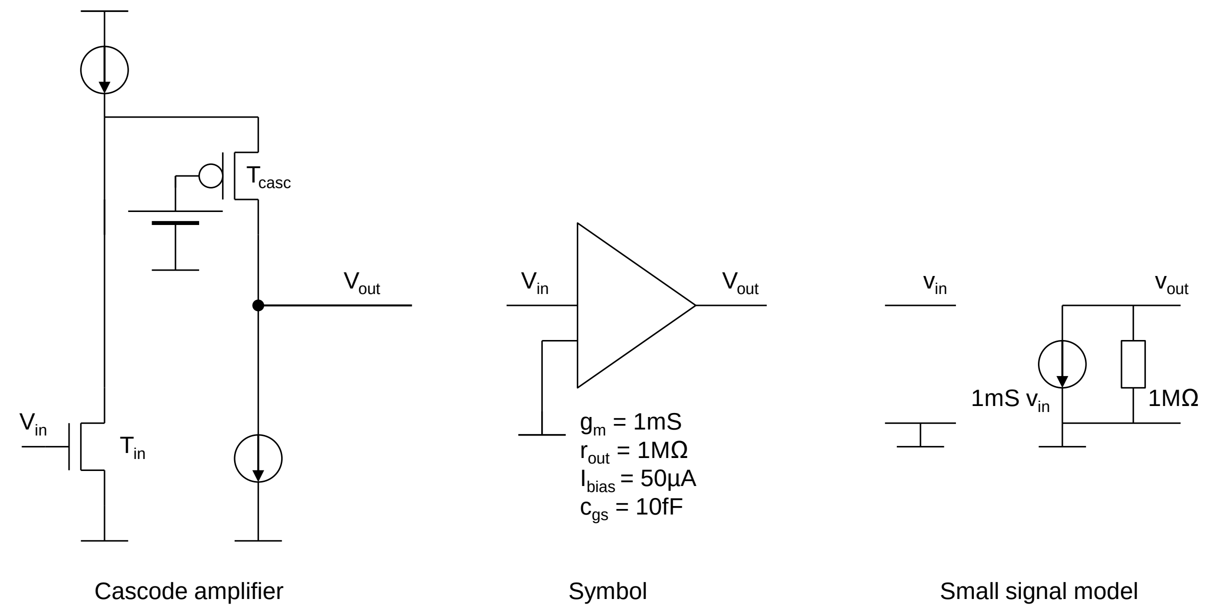


Fig 3: Amplifier with folded cascode - the standard variant with I_{bias} = 50 µA

The amplifier that we presented in lecture 8 had a current gain of g_m = 1 mS with a bias current of I_{bias} = 50 µA. We call our amplifier with 50 µA bias current the *standard amplifier* (Figure 3). The standard cascode amplifier has an output resistance of r_{out} = 1 MΩ and a voltage gain of g_m r_{out} = 1000.

If this amplifier drives a load resistance of R_{load} = 100 Ω, its open loop gain is reduced to:

$A_{OL} = g_m (r_{out} \,||\, R_{load}) \sim g_m R_{load} = 0.1$ (Figure 4).

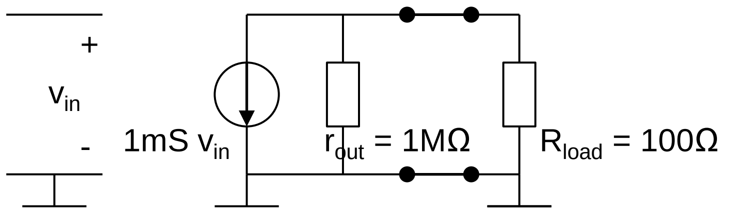


Fig 4: The standard amplifier with load resistance

In order to achieve larger amplification, we have to *match the impedances* and connect several standard amplifiers in parallel until we reach $r_{out} \sim R_{load}$.

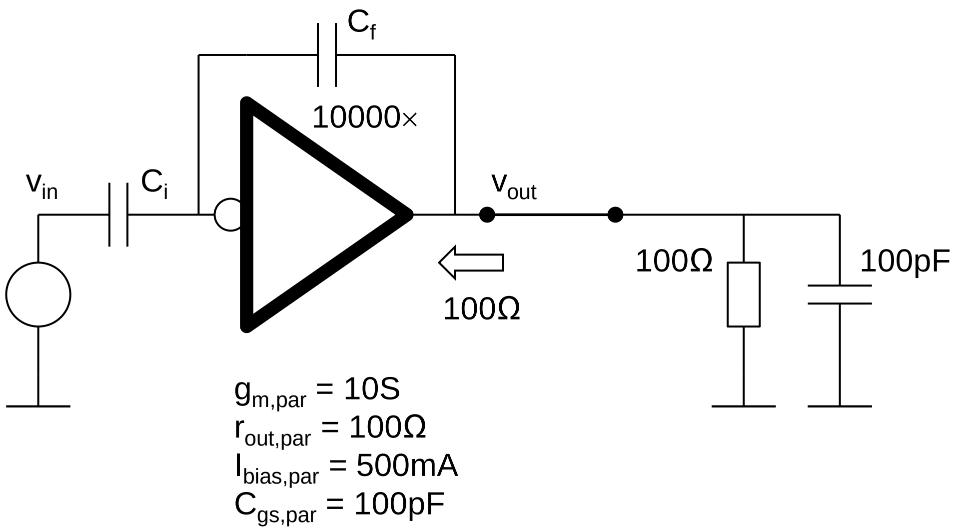


Fig 5: Single-stage amplifier, matching of impedances

If we connect 10000 amplifiers in parallel, the full circuit has the transconductance:

$g_{m,\ par} = 10000 \times g_m = 10$ Si

and the output resistance

$r_{out,\ par} = r_{out} / 10000 = 100\ \Omega$ (Figure 5).

The open loop gain (absolute value) is about

$|\ A_{OL}\ | = g_{m,\ par}\ (r_{out,\ par} \parallel R_{load}) \sim 0.5\ g_{m,\ par}\ R_{load} = 500.$

(One half of the specified) The total bias current is

$I_{bias,\ par} = 10000 \times I_{bias} = 500$ mA.

We will neglect that the DC current through R_{load} contributes to the transistor bias current and thereby influences its transconductance.

Therefore we only achieve half of the specified gain and have to accept a very large bias current and a large layout area. The large bias current leads to a large power consumption. The gate capacitance would also be large, approximately:

$C_{gs,\ par} = 10000 \times 10$ fF $= 100$ pF.

We could achieve the gain of 50 by choosing $C_i / C_f = 50$. In the case of $C_i << C_{gs,\ par}$ following applies:

$$|\beta A_{OL}| = \frac{C_f}{C_i + C_{gs,par} + C_f}|A_{OL}| \sim \frac{1}{1 + \frac{C_{gs,par}}{C_i}}\frac{C_f}{C_i}|A_{OL}| \ll \frac{C_f}{C_i}|A_{OL}| = 10$$

The closed loop gain (gain with feedback)

$A_{FB} = \frac{A_{IN}A_{OL}}{1+|\beta A_{OL}|}$

Would the strongly depend on A_{OL}, because the fraction in Mason's gain formula cannot be reduced by shortening A_{OL}.

For this reason, let us chose:

$C_i = C_{gs,par} = 100$ pF und $C_f = 2$pF.

It follows:

$|\beta A_{OL}| = 5$

The rise time of the step response is given by the following formula (Lecture 6):

$$\tau_r \sim \frac{C_{load}(C_{gs}+C_i)}{g_m C_f} \sim 2|A_{FB}|\frac{C_{load}}{g_m} \sim 100\,\frac{100\text{pF}}{10\text{Si}} = 1\text{ns} \quad (1)$$

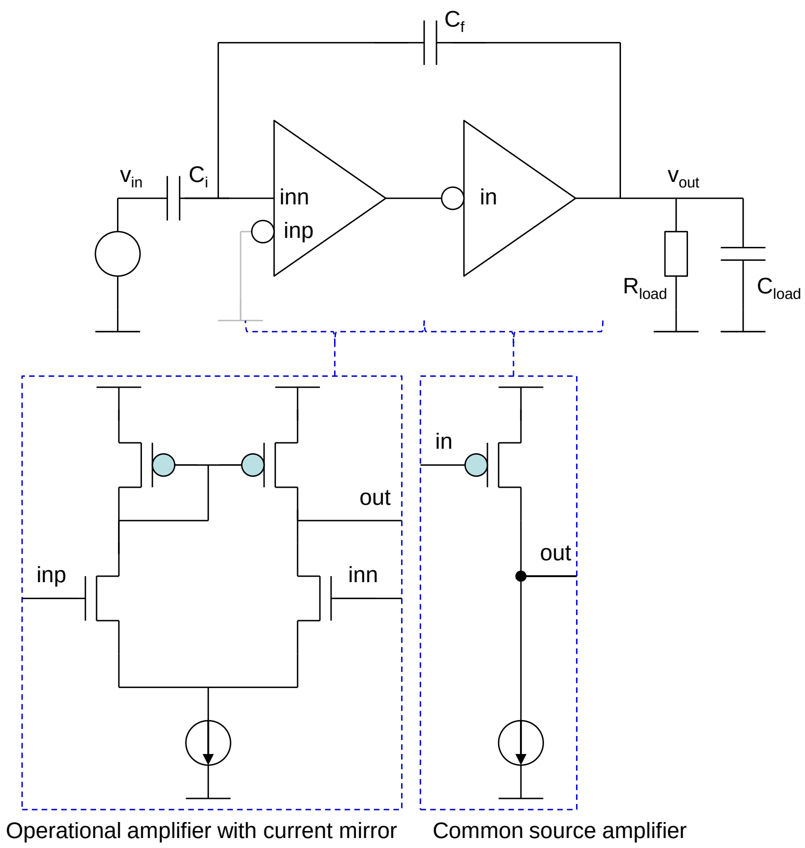
Note that, if the input source has an internal resistance R_i, the time constant at the input is $\tau_i = R_iC_i$. This time constant slows down the amplifier significantly. For $R_i = 100\Omega$, we get:

$$\tau_i \sim R_iC_i = 100\text{pF} \times 100\Omega = 10\text{ns} \qquad (2)$$

Disadvantages of the circuit of Figure 5 are a large power consumption, a large layout area and a large capacitive load C_i for the input source.

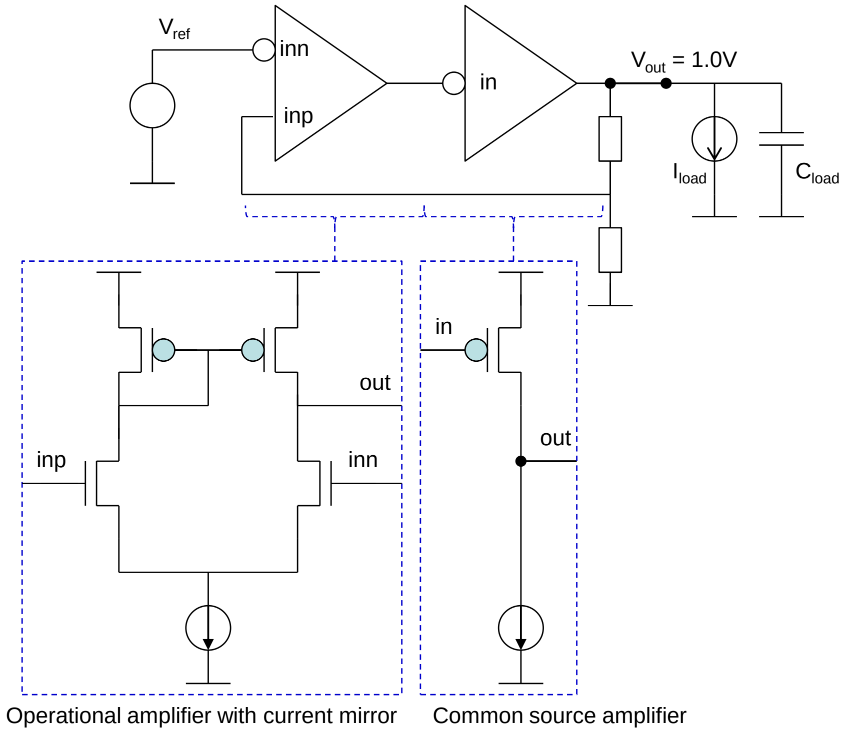
Two-stage amplifiers

Another solution for the implementation of the voltage amplifier and the regulator is to connect two amplifier stages in series.



Voltage amplifier	
Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20

Fig 6: Voltage amplifier implemented with two amplifier stages



LDO regulator	
Parameter	Value
C_{load}	10nF
I_{load}	0-100mA
r_{out}	0.1Ω

Fig 7: Linear regulator implemented with two amplifier stages

Figure 6 shows the voltage amplifier with feedback that employs two amplifier stages.

The linear regulator is shown in Figure 7. The input source is the reference source V_{ref}.

We will discuss the voltage amplifier first.

Voltage amplifier with two stages

Let us derive the transfer function of the two-stage voltage amplifier with feedback. Figure 8 (bottom part) shows the small signal model. We use generic names for the capacitances and resistances at the amplifier outputs C_1, C_2, R_1 and R_2.

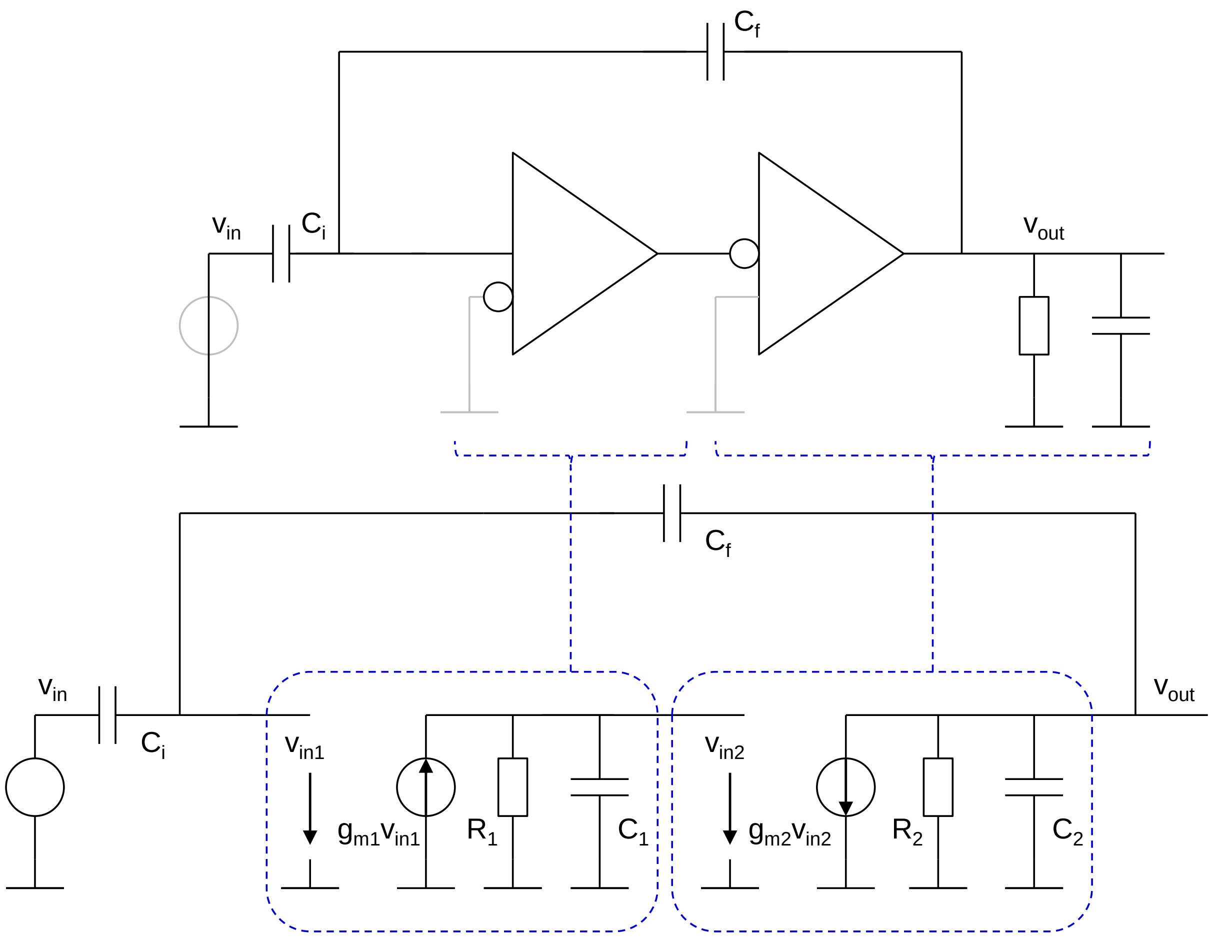


Fig 8: Voltage amplifier based on two amplifying stages and feedback. Top: block circuit. Bottom: small signal model.

The voltage gain with feedback is defined as:

$$A_{FB}(s) = \frac{v_{out}(s)}{v_{in}(s)}$$

It can be calculated using Mason's formula:

$$A_{FB}(s) = \frac{FF + A_{IN}A_{OL}}{1 - \beta A_{OL}} \quad (3)$$

A_{IN} and β are real numbers in our case.

The following applies:

$$\beta = \frac{C_f}{C_f + C_i} \qquad (4)$$

and

$$A_{IN} = \frac{C_i}{C_f + C_i} \quad (5)$$

Let us make the following assumption: The impedance:

$$Z_2(s) = \frac{1}{sC_2}||R_2 = \frac{R_2}{sR_2C_2+1} \quad (6)$$

is smaller than other impedances. Therefore it follows:

FF = 0,

and

$$A_{FB}(s) = \frac{A_{IN}A_{OL}}{1-\beta A_{OL}} \quad (7)$$

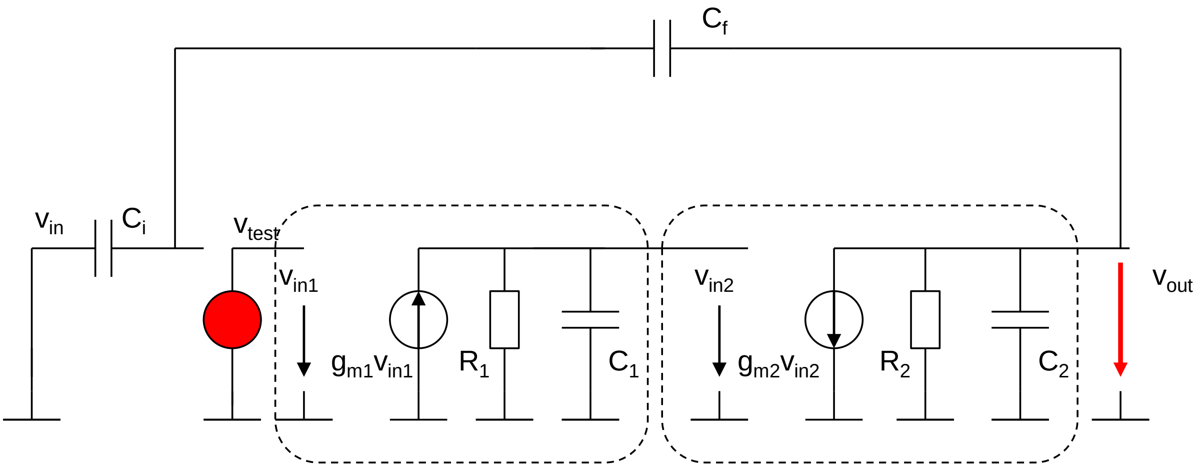


Fig 9: Test circuit for calculation of the open loop gain

Figure 9 shows the test circuit for calculation of the open loop gain

$$A_{OL}(s) = v_{out(s)}/v_{test}$$

The open loop gain is:

$$A_{OL}(s) = -g_{m1}Z_1g_{m2}Z_2 \quad (8)$$

Z_1 and Z_2 are the impedances *seen* by the sources g_{m1} and g_{m2}:

$$Z_1(s) = \frac{1}{sC_1}||R_1 = \frac{R_1}{sR_1C_1+1} \quad (9)$$

$$Z_2(s) = \frac{1}{sC_2}||\frac{C_f+C_i}{sC_fC_i}||R_2 = \frac{R_2}{sR_2C_2+1} \quad (10)$$

We have assumed that the serial capacitance of C_f and C_i: $C_f C_i/(C_f + C_i) \sim C_f$ is much smaller than C_2.

If we substitute (9) and (10) in (8), we obtain:

$$A_{OL}(s) = \frac{-g_{m1}R_1g_{m2}R_2}{(1+sR_1C_1)(1+sR_2C_2)} \quad (11)$$

Let us define two time constants and two voltage gains:

$$\tau_1 \equiv R_1C_1,\ \tau_2 \equiv R_2C_2,\ A_1 \equiv g_{m1}R_1,\ A_2 \equiv g_{m2}R_2 \quad (12)$$

Let us also define the DC open loop gain:

$$A_{OL,DC} \equiv -g_{m1}R_1g_{m2}R_2 \quad (13)$$

It holds then:

$$A_{OL}(s) = \frac{A_{OL,DC}}{(1+s\tau_1)(1+s\tau_2)} = \frac{A_{OL,DC}}{\tau_1\tau_2s^2+(\tau_1+\tau_2)s+1} \quad (14)$$

If we insert (4), (5) and (14) in (3) we obtain the transfer function of the circuit with feedback:

$$A_{FB}(s) = \frac{A_{IN}A_{OL,DC}}{1-\beta A_{OL,DC}} \frac{1}{\frac{\tau_1\tau_2}{1-\beta A_{OL,DC}}s^2+\frac{(\tau_1+\tau_2)}{1-\beta A_{OL,DC}}s+1} = A_{FB,DC}\frac{1}{Q(s)} \quad (15)$$

Q is the characteristic polynomial of the transfer function.

Influence of poles of A_{IN} on step response of A_{FB}

If we replace the complex frequency *s* with the derivative (*d/dt*) operator in (15), we obtain the differential equation for the output voltage. The step response has the following form:

$$u_{out,imp}(t) \equiv h(t)(C_0 + C_1e^{\lambda_1 t} + C_2e^{\lambda_2 t}) \quad (16)$$

Factors λ1 and λ2 are the solutions (roots) of the polynomial Q (s) in (15), or the poles of $A_{FB}(s)$.

$$Q(\lambda) = 0$$

The polynomial Q (s) can be represented in the following canonical form:

$$\frac{\tau_1\tau_2}{1-\beta A_{OL,DC}}s^2 + \frac{(\tau_1+\tau_2)}{1-\beta A_{OL,DC}}s + 1 = \left(\frac{s}{\omega_0}\right)^2 + \left(\frac{1}{Q}\right)\left(\frac{s}{\omega_0}\right) + 1 \quad (17)$$

The factors are:

1) Poles of $A_{IN}(s)$:

$$\omega_1 = \frac{1}{\tau_1};\ \omega_2 = \frac{1}{\tau_2} \quad (18)$$

2) Resonance frequency:

$$\omega_0 = \sqrt{\omega_1\omega_2(1-\beta A_{OL,DC})} \quad (19)$$

3) Quality factor:

$$Q = \frac{\omega_0}{\omega_1+\omega_2} = \frac{\sqrt{\omega_1\omega_2(1-\beta A_{OL,DC})}}{\omega_1+\omega_2} \qquad (20)$$

The roots of Q(s) are:

$$\lambda_{12} = -\overline{\omega} \pm \overline{\omega}\sqrt{1-4Q^2};\ \overline{\omega} = \frac{\omega_1+\omega_2}{2} \qquad (21)$$

For

$$4Q^2 - 1 > 0 \Rightarrow Q > \frac{1}{2} \qquad (22)$$

the step response is periodic or contains sine and cosine terms.

$$u_{out,imp}(t) = h(t)\left[A_0 + e^{-\overline{\omega}t}\left(A_1 \cos\left(\sqrt{4Q^2-1}\,\overline{\omega}t\right) + A_2 \sin\left(\sqrt{4Q^2-1}\,\overline{\omega}t\right)\right)\right] \qquad (23)$$

with $A_0 = 1$, $A_1 = -1$ und $A_2 = 1/(4Q^2 - 1)^{0.5}$.

For

$$4Q^2 - 1 < 0 \Rightarrow Q < \frac{1}{2} \qquad (24)$$

the step response is aperiodic and exponential with real time constants:

$\tau_{1,fb} = -1/\lambda_1$ and $\tau_{2,fb} = -1/\lambda_2$:

$$u_{out,imp}(t) = h(t)[C_0 + C_1 e^{-\tau_{1,fb}t} + C_2 e^{-\tau_{2,fb}t}] \qquad (25)$$

with $C_0 = 1$, $C_1 = -\lambda_2/(\lambda_2 - \lambda_1)$ und $C_2 = \lambda_1/(\lambda_2 - \lambda_1)$.

The condition (24) leads to the following equation:

$$Q = \frac{\sqrt{\omega_1\omega_2(1-\beta A_{OL,DC})}}{\omega_1+\omega_2} < \frac{1}{2} \qquad (26)$$

If we assume that the time constants in $A_{OL}(s)$ τ_1 and τ_2 are very different:

$$\tau_1 \gg \tau_2;\ \omega_1 \ll \omega_2$$

and if we assume that $\beta_{AOL,\,DC}$ is negative and has a large amount, the formula (26) simplifies as follows:

$$Q \sim \frac{\sqrt{\omega_1\omega_2|\beta A_{OL,DC}|}}{\omega_2} < \frac{1}{2} \Rightarrow \frac{\omega_1|\beta A_{OL,DC}|}{\omega_2} < \frac{1}{4}$$

or:

$$\tau_2 < \frac{1}{4}\frac{\tau_1}{|\beta A_{OL,DC}|} \qquad (27)$$

The second time constant τ_2 must be smaller than the first time constant τ_1 divided by 4 | βA_{DC} |. Since | βA_{DC} | is normally >> 1 (in our example | βA_{DC} | = 20), the second time constant must be much smaller than the first so that the step response does not oscillate. Very different time constants in the open gain lead to exponential behaviour.

If the following holds:

$$\tau_2 \ll \frac{1}{4}\frac{\tau_1}{|\beta A_{OL,DC}|}$$

It holds also Q << 1.

(Note that Q is always greater than 0.)

The step response is then approximately:

$$u_{out,imp}(t) \sim h(t)\left[1 - e^{-\frac{t}{\tau_r}}\right] \qquad (28)$$

With the rise time:

$$\tau_r = \frac{\tau_1}{\beta A_{OL,DC}} \qquad (29)$$

We define here the bandwidth of amplifier B as

$$B = \frac{1}{2\pi\tau_r} \qquad (30)$$

The larger time constant τ_1 is also called the dominant time constant, since it determines the step response.

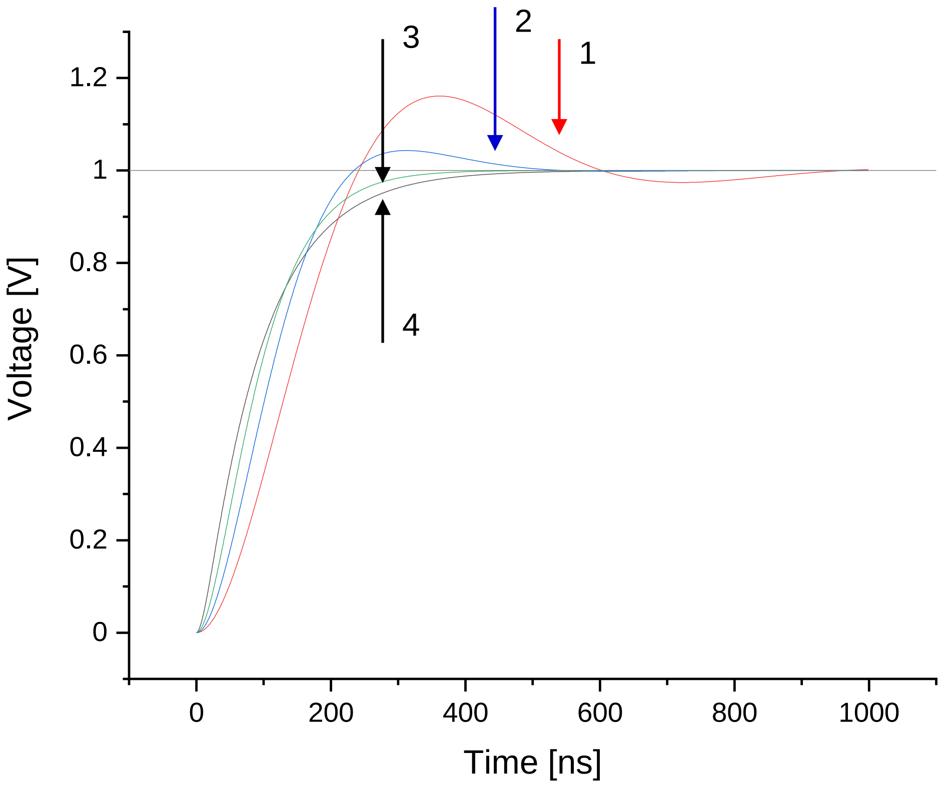


Fig 10: Step responses for different βA_{OL} functions with Q values: 1) Q ~ 1; 2) Q ~ 0.707; 3) Q ~ 0.5 and 4) Q ~ 0.32. βA_{DC} = 100.

Figure 10 shows the step responses which correspond to the βA_{OL} having the parameters from the following table.

Case	$\boldsymbol{\omega_1}$	$\boldsymbol{\omega_2}$	**Q**	**Ratio** $\boldsymbol{\tau_1/\tau_2}$ **($\boldsymbol{\beta A_{DC}}$ = 100)**	**PM**
1	0.1MHz	100×ω_1	1	$\tau_2 > \frac{1}{2}\frac{\tau_1}{\lvert\beta A_{OL,DC}\rvert}$	53°
2	0.1MHz	200×ω_1	0.707	$\tau_2 = \frac{1}{2}\frac{\tau_1}{\lvert\beta A_{OL,DC}\rvert}$	67°
3	0.1MHz	400×ω_1	0.5	$\tau_2 = \frac{1}{4}\frac{\tau_1}{\lvert\beta A_{OL,DC}\rvert}$	77°
4	0.1MHz	1000×ω_1	0.32	$\tau_2 < \frac{1}{4}\frac{\tau_1}{\lvert\beta A_{OL,DC}\rvert}$	85°

The step response (3) for Q = 0.5 that is equivalent to

$$\tau_2 = \frac{1}{4}\frac{\tau_1}{|\beta A_{OL,DC}|}$$

differs only a little from the aperiodic step response for Q < 0.5:

$$u_{out,imp}(t) \sim h(t)\left[1 - e^{-\frac{t}{\tau_r}}\right];\ \tau_r = \frac{\tau_1}{\beta A_{OL,DC}}$$

Note that the step response (2) in Figure 10 for

$$Q = \frac{1}{\sqrt{2}} = 0.707\ \Rightarrow \tau_2 = \frac{1}{2}\frac{\tau_1}{|\beta A_{OL,DC}|}$$

first reaches the amplitude of 1 has no undershoot.

It is interesting that the two-stage amplifier would have real time constants and exponential time behaviour with no feedback. By using feedback, the time response can become periodic, as if we had L and C in the circuit. That is the reason why it is possible to realize oscillators employing feedback. These oscillators do not need inductors.

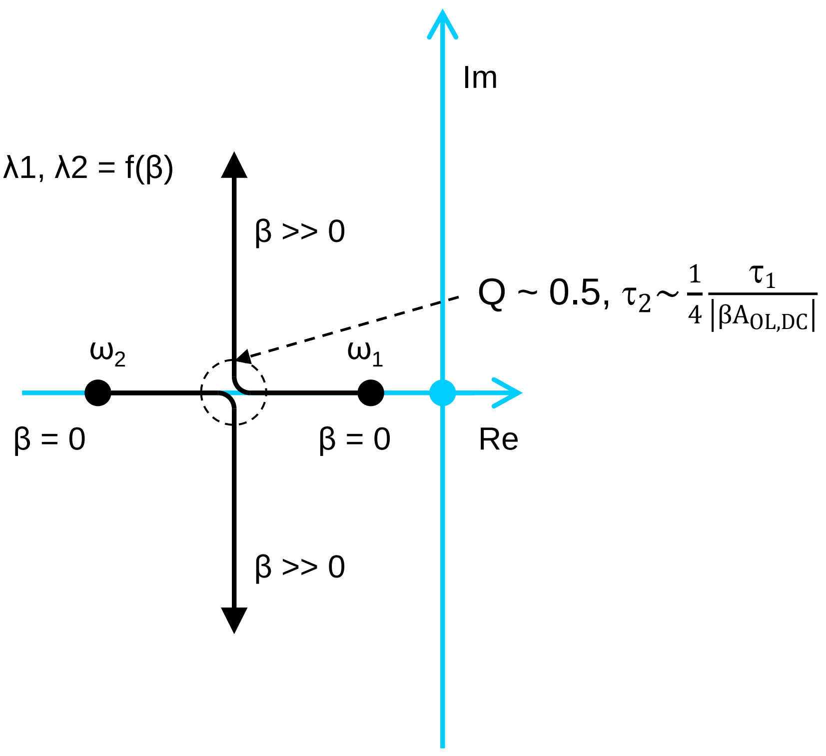


Fig 11: Position of poles of $A_{FB}(s)$ when the strength of the feedback β increases

Figure 11 shows how the roots λ_1 and λ_2 of the characteristic polynomial Q (s) of

$$A_{FB}(s) = \frac{A_{IN}A_{OL}(s)}{1-\beta A_{OL}(s)} \equiv \frac{P(s)}{Q(s)}$$

(poles of AFB (s)) move in a complex plane if we increase the strength of the negative feedback β starting from 0. Without negative feedback (β = 0) the poles of A_{FB} (s) are equal to the poles of A_{OL} (s): $\lambda_1 = \omega_1$ and $\lambda_2 = \omega_2$. The poles are real numbers. When the negative feedback increases, the poles move towards each other (Q increases) until they become equal for Q = 0.5 $\lambda_1 = \lambda_2 = (\omega_1 + \omega_2) / 2$. For Q > 0.5, the poles become complex with a constant real part $= (\omega_1 + \omega_2) / 2$. The imaginary parts have the same magnitude and opposite signs. The step response contains then sine and cosine terms.

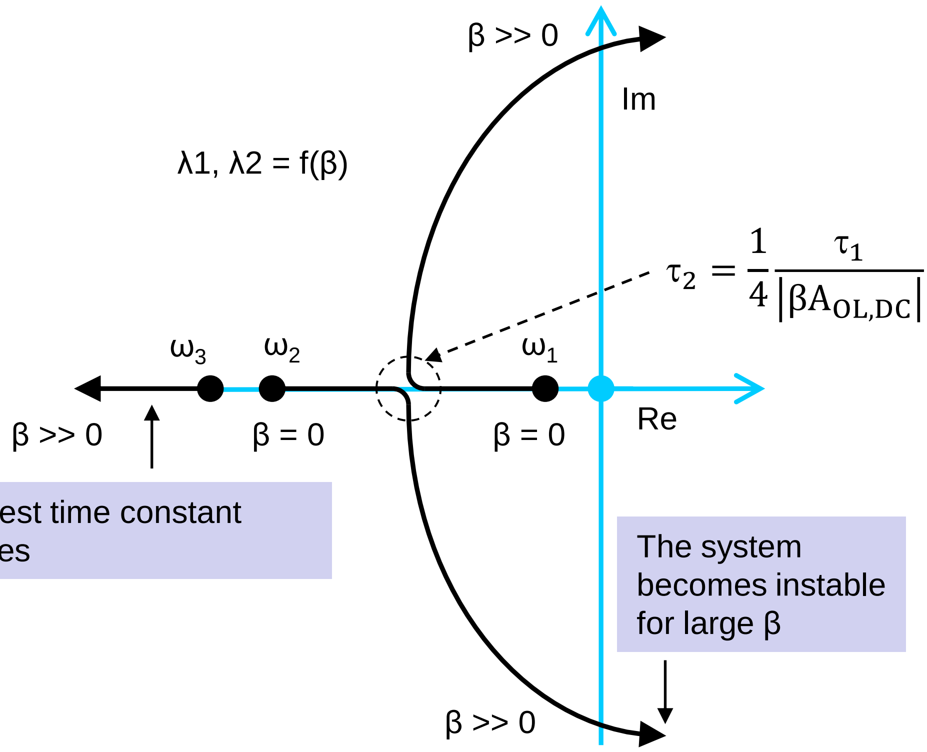


Fig 12: Position of three poles of $A_{FB}(s)$ when the strength of the feedback β increases

Figure 12 shows the case where $A_{IN}(s)$ has three poles ω_1, ω_2 and ω_3. We can perform a similar analysis as above and plot in a complex plane how the poles of $A_{FB}(s)$ move when we increase the strength of the negative feedback β. The poles of $A_{FB}(s)$ are real for β = 0: $\lambda_1 = \omega_1$, $\lambda_2 = \omega_2$ and $\lambda_3 = \omega_3$. The two smaller poles move towards each other and become complex. The third pole remains real and its magnitude increases, the corresponding time constant gets smaller. The only difference to the second order system is that the real part of the complex poles can also become positive for high β. The amplitude of the oscillation then increases until the circuit is no longer linear. The circuit becomes unstable.

The conditions for a step response without oscillations are nearly equal for 2nd - and 3rd order systems. This means that all formulas from this lecture can also be used in the case of $A_{IN}(s)$ with three poles.

Nyquist stability criterion

There is a method that tells us in the general case whether the poles of

$$A_{FB}(s) = \frac{A_{IN}(s)A_{OL}(s)}{1-\beta A(s)} \qquad (31)$$

have a negative real part, or whether the corresponding circuit with feedback is stable. The assumption is that all factors have a frequency dependence:

$$\beta A(s) = \frac{L(s)}{M(s)};\ A_{IN}(s)A_{OL}(s) = \frac{N(s)}{O(s)} \qquad (32)$$

This method is Nyquist's stability criterion. Nyquist's stability criterion is based on the Bode diagram.

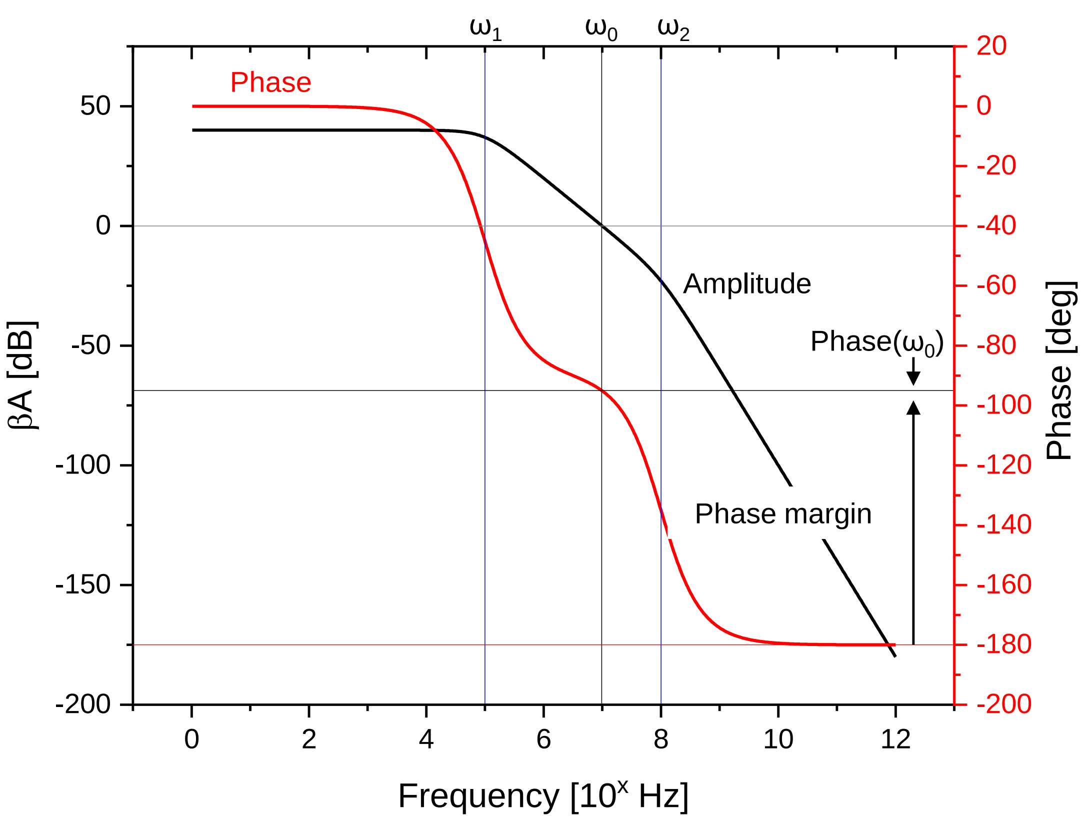


Fig 13: Bode diagram

The Bode diagram of a transfer function $\beta A(j\omega)$ with two time constants

$$\beta A(j\omega) = \frac{A}{(j\omega/\omega_1+1)(j\omega/\omega_2+1)} \qquad (33)$$

is shown in Figure 13. The left Y-axis is $|\beta A(j\omega)|$ in dB or $20\log(|\beta A(j\omega)|)$.

$$|\beta A(j\omega)| = \frac{A}{\sqrt{\left(\left(\frac{\omega}{\omega_1}\right)^2+1\right)\left(\left(\frac{\omega}{\omega_2}\right)^2+1\right)}} \qquad (34)$$

X–axis is log(ω).

The frequencies ω_1 = 0.1 MHz and ω_2 = 100 MHz are the poles of βA (jω). The slope after the first pole is -20dB / decade and after the second pole -40dB / decade.

The right Y axis is the phase of βA (jω):

$$\text{Phase}(\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_1}\right) - \tan^{-1}\left(\frac{\omega}{\omega_2}\right) \qquad (35)$$

The phase changes by -90° around each pole ω (in the region from 0.1 ω to 10 ω).

We define the zero crossing frequency ω_0 as the frequency that fulfils the following condition

$|\beta A(j\omega_0)| = 1$ ($|\beta A(j\omega_0)| = 0$ dB)

A circuit with feedback is stable [1] (see slides DAS_2020_10_Nyquist_Beweis.pptx) if the absolute value of the phase change of the loop gain βA(iω) from ω = 0 to $\omega = \omega_0$ is less than 180 °.

We call the difference 180 ° minus the absolute value of the phase change the *phase margin* (PM) (Figure 13).

The condition for the validity of the Nyquist criterion is that the functions βA(s) and $A_{IN}(s)$ $A_{OL}(s)$ have no poles with a positive real part.

[1] The poles of A_{FB} (iω) have negative real parts

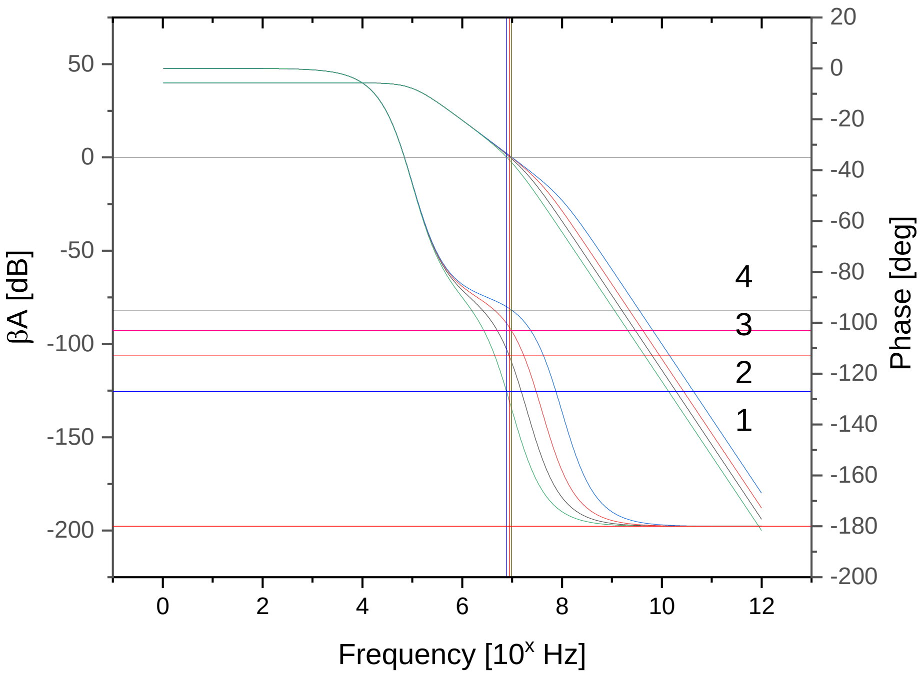


Fig 14: Bode diagrams of βA(s) functions with the parameters from the table

Figure 14 shows Bode diagrams for the βA_{OL} functions with parameters from the table. (It holds also $\beta A_{OL,DC} = 100$.) The parameters are the same as in Figure 10. βA_{OL} with phase reserve < 67 ° leads to a periodic step response.

Case	**ω_1**	**ω_2**	**Q**	**PM**
1	0.1MHz	$100\times\omega_1$	1	53°
2	0.1MHz	$200\times\omega_1$	0.707	67°
3	0.1MHz	$400\times\omega_1$	0.5	77°
4	0.1MHz	$1000\times\omega_1$	0.32	85°

The condition for aperiodic step response

$$\tau_2 = \frac{1}{4}\frac{\tau_1}{|\beta A_{DC}|}; Q = 0.5$$

corresponds to a phase reserve of = 77 °.

The conditions for the fastest step response

$\tau_2 = \frac{1}{2}\frac{\tau_1}{|\beta A_{DC}|}; Q = 0.707$

corresponds to a phase reserve of 67 °.

The more the first and second time constants are separated, the greater the phase reserve.

First implementation of the two-stage voltage amplifier

We will start with the specifications in the table:

Voltage amplifier	
Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20

We can optimize the amplifier in two ways:

1) The current consumption (power consumption) should be minimal.
2) The bandwidth defined by equation (30) should be as large as possible - the rise time of the step response should be minimal.

We will optimize the amplifier for small power consumption.

We use a simple operational amplifier with a current mirror as the first amplifier stage and a common source amplifier with an active load (without cascode) as the second stage. Our standard amplifiers (amplifiers in standard size) have I_{bias} = 50 µA, g_m = 1 mS, r_{out} = 50 kΩ. The voltage gain of the amplifier without a resistive load is A = g_m r_{out} = 50. If we use the standard amplifier as the second stage and connect it to R_{load} = 100 Ω, it has a voltage gain of only:

$A_2 = g_m(r_{out}||R_{load}) \sim g_m R_{load} = 0.1$

A_2 is defined here as an absolute value, the actual gain dv_{out} / dv_{in} is negative (= -A_2).

The two-stage amplifier would in this case have a gain of only $A = A_1 A_2 = 50 \times 0.1 = 5$.

We need at least a gain $A_2 = 20$ to achieve the specified total gain of 1000.

In the case of the second stage, we will therefore connect as many common source amplifiers in parallel until the gain becomes 20:

$$A_2 = g_{m,par}(r_{out,par}||R_{load}) \sim 20$$

We need to use around 200 standard amplifiers (Figure 15).

In this case it holds:

$$g_{m2} = g_{m,par} = 200 \times 1mS = 200mS \quad (36)$$

$$r_{out2} = r_{out,par} = 50k\Omega/200 = 250\Omega \quad (37)$$

and

$$A_2 = g_2(r_{out,2}||R_{load}) \sim g_{m2}R_{load} = 20 \quad (38)$$

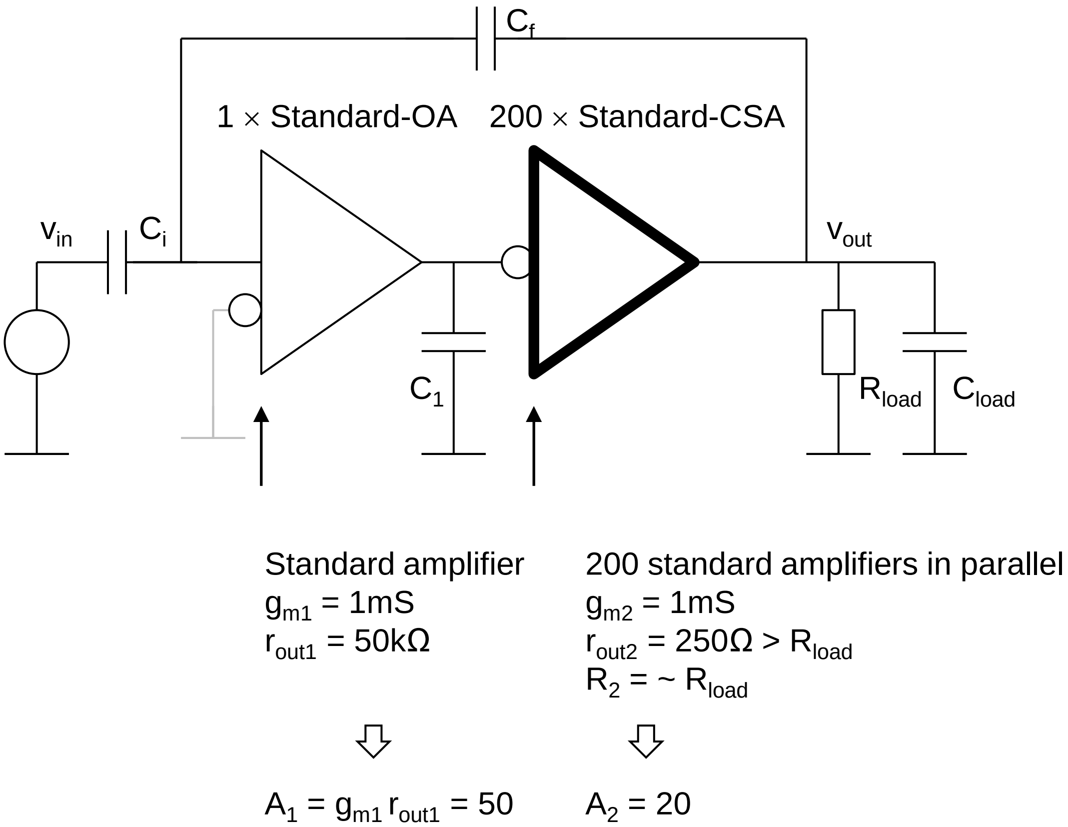


Fig 15: Two-stage voltage amplifier, implementation with the standard amplifiers (amplifier with $I_{bias} = 50\ \mu A$). The first amplifier stage is implemented with a standard size operational amplifier (OA). The second amplifier stage consists of 200 common source amplifiers (CSA) (each standard size) in parallel.

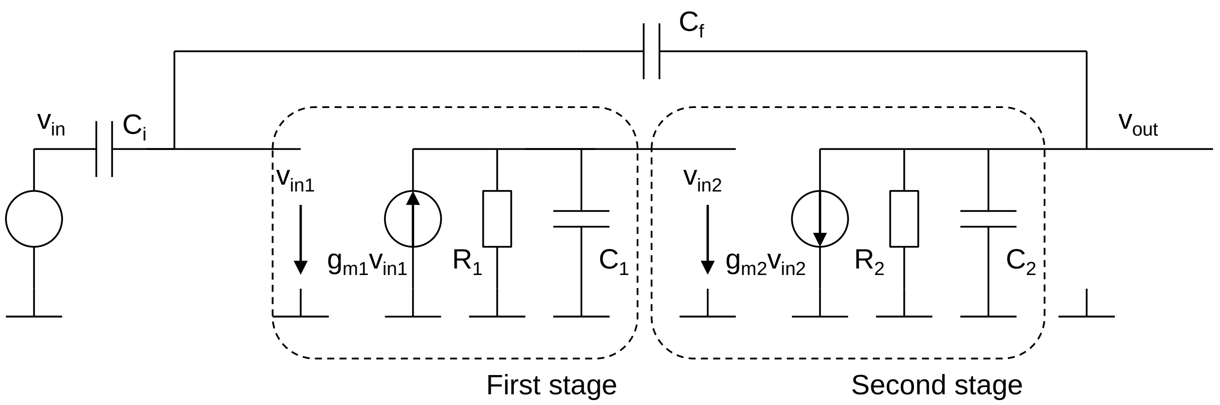


Fig 16: Two-stage voltage amplifier - small signal model

The implemented circuit show in Figure 15 corresponds to the generic circuit in Figure 16 if the values from the following table apply:

Generic circuit	**Implemented circuit**	**Value**
R_1	r_{out1}	50kΩ
R_2	R_{load}	100Ω
C_2	C_{load}	100pF
C_1	C_1	TBD
g_{m1}	g_{m1}	1mS
g_{m2}	g_{m2}	200mS
A_1	$g_{m1}r_{out1}$	50
A_2	$g_{m1}R_{load}$	20

Let us now calculate the factors β, A_{IN}, and A_{OL}.

We will implement the feedback using two capacitors C_i and C_f. We put C_i = 50 C_f. The value for C_f can be chosen relatively freely, we set C_f = 200 fF. (Larger C_f values result in less noise.)

In this case, we get:

$$\beta = \frac{C_f}{C_f + C_i} = 0.02 \qquad (39)$$

and

$$A_{IN} = \frac{C_i}{C_f + C_i} \sim 1 \qquad (40)$$

The open loop gain is (s. (14)):

$$A_{OL}(s) = \frac{-g_{m1} r_{out1} g_{m2} R_{load}}{(1 + s r_{out1} C_1)(1 + s R_{load} C_{load})} = \frac{-A_1 A_2}{(1 + s\tau_1)(1 + s\tau_2)} \qquad (41)$$

This formula is equal to (14).

A_{FB} and the step response are described with formulas (15), (23) and (25).

Stability

Let us now calculate the value of capacitance C_1 required to obtain an step response without oscillations.

The condition for τ_2 for an step response without overshoot is (27):

$$\tau_2 < \frac{1}{4} \frac{\tau_1}{|\beta A_{OL,DC}|}$$

The dominant time constant τ_1 is then:

$$\tau_1 > 4|\beta A_{OL,DC}| R_{load} C_{load} = 4 \times 20 \times 10 \text{ ns} = 800 \text{ ns} \qquad (42)$$

This condition can be achieved by suitable C_1:

$$\tau_1 = r_{out1} C_1 > 4|\beta A_{OL,DC}| R_{load} C_{load} \Rightarrow C_1 > \frac{4 \times 20 \times 10 \text{ ns}}{50 \text{k}\Omega} = 16\text{pF} \qquad (43)$$

The rise time of the step response is then approximately:

$$\tau_r \sim \frac{\tau_1}{\beta A_{OL,DC}} = \frac{C_1}{\beta g_{m1} A_2} > \frac{4|\beta A_{OL,DC}| R_{load} C_{load}}{\beta A_{OL,DC}} = 4 R_{load} C_{load} = 40\text{ns} \qquad (44)$$

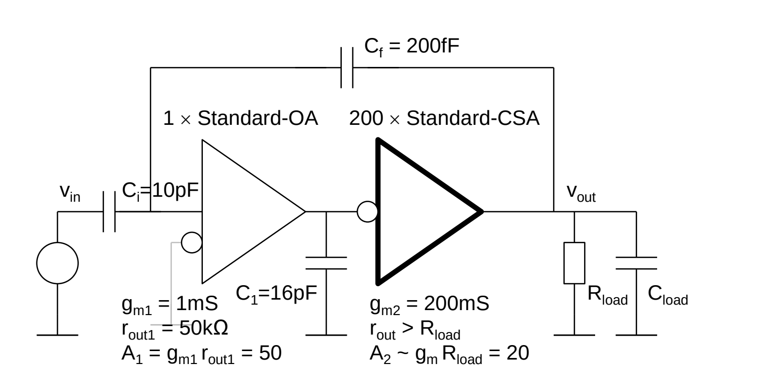
Unfortunately τ_r is relatively long, which makes the step response slow and reduces the bandwidth.

The following table summarizes the results:

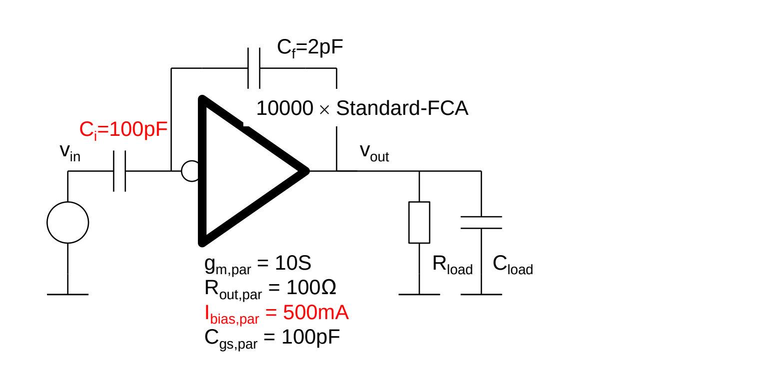
Generic circuit	Implemented circuit	Value
R_1	r_{out1}	50kΩ

R_2	R_{load}	100Ω
C_2	C_{load}	100pF
C_1	C_1	16pF
g_{m1}	g_{m1}	1mS
g_{m2}	g_{m2}	200mS
A_1	$g_{m1}r_{out1}$	50
A_2	$g_{m1}R_{load}$	20
τ_1	$r_{out1}\ C_1$	$4\beta A\tau_2$
τ_2	$R_{load}\ C_{load}$	10ns
βA	βA_1A_2	20

Conclusion: The two-stage amplifier meets the specification for open loop gain and has about 50× less power consumption than the single-stage amplifier. The minimum rise time of the step response is about 40× worse than the rise time in the case of the single-stage amplifier. Figure 17 shows the comparison.



Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20
τ_r	$4C_{load}R_{load}$ = 40ns
I_{bias}	(201 I_0) 10.1mA



Parameter	Value
C_{load}	100pF
R_{load}	100Ω
A_{FB}	<50
A_{OL}	500
βA	10
τ_r	$2A_{FB}C_{load}/g_m$=1ns
I_{bias}	(10000 I_0) 500mA

Fig 17: Comparison between voltage amplifiers with two stages (top) and with one stage (bottom). Disadvantages are marked in red - e.g. in the case of single-stage amplifier, high power consumption or high input capacitance. OA - operational amplifier, CSA - common source amplifier, FCA - folded cascode amplifier.

Lecture 11

Implementation 2 (frequency compensation)

We have seen that a two-stage amplifier can achieve high gain with low power consumption. The simple variant of Figure 15 has a relatively small bandwidth (30) when the feedback was used.

We can achieve an improvement by connecting the capacitance C_1 between the input and the output of the second stage (Figure 18). This technique is called frequency compensation. The DC gain of the second stage must be negative. The capacitance between the input and the output of the second stage separates the time constants (pole splitting) and thus reduces the oscillations and improves the bandwidth. We will discuss it in this chapter.

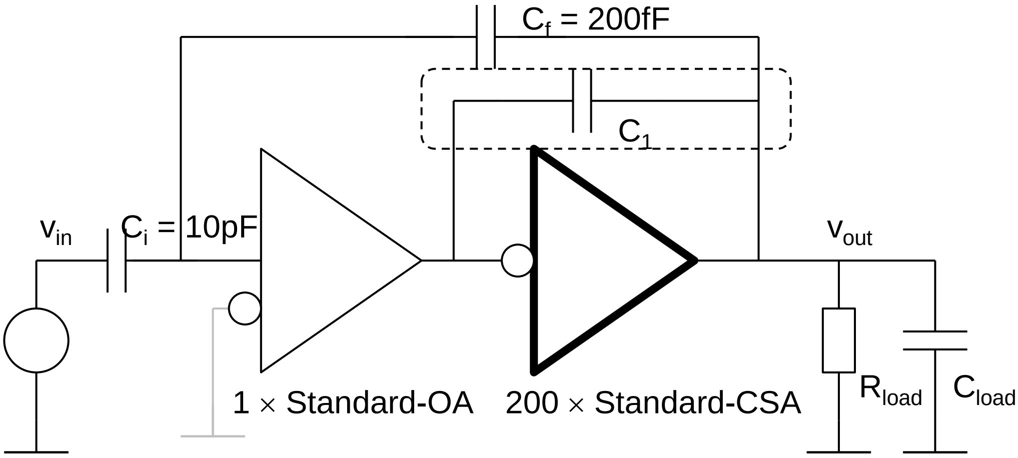


Fig 18: Two-stage amplifier with frequency compensation

We start with the dimensions of the amplifier stages as in the first example:

Generic circuit	Implemented circuit	Value
R_1	r_{out1}	50kΩ
R_2	R_{load}	100Ω
C_2	C_{load}	100pF
C_1	C_1	TBD
g_{m1}	g_{m1}	1mS
g_{m2}	g_{m2}	200mS

A_1	$g_{m1}r_{out1}$	50
A_2	$g_{m1}R_{load}$	20

Let us calculate the factors β, A_{IN}, and A_{OL}.

We set C_i = 10 pF and C_f = 200 fF again. It follows:

$$\beta = \frac{C_f}{C_f + C_i} = 0.02 \qquad (45)$$

and

$$A_{IN} = \frac{C_i}{C_f + C_i} \sim 1 \qquad (46)$$

Let us now calculate A_{OL}. The test circuit is shown in Figure 19.

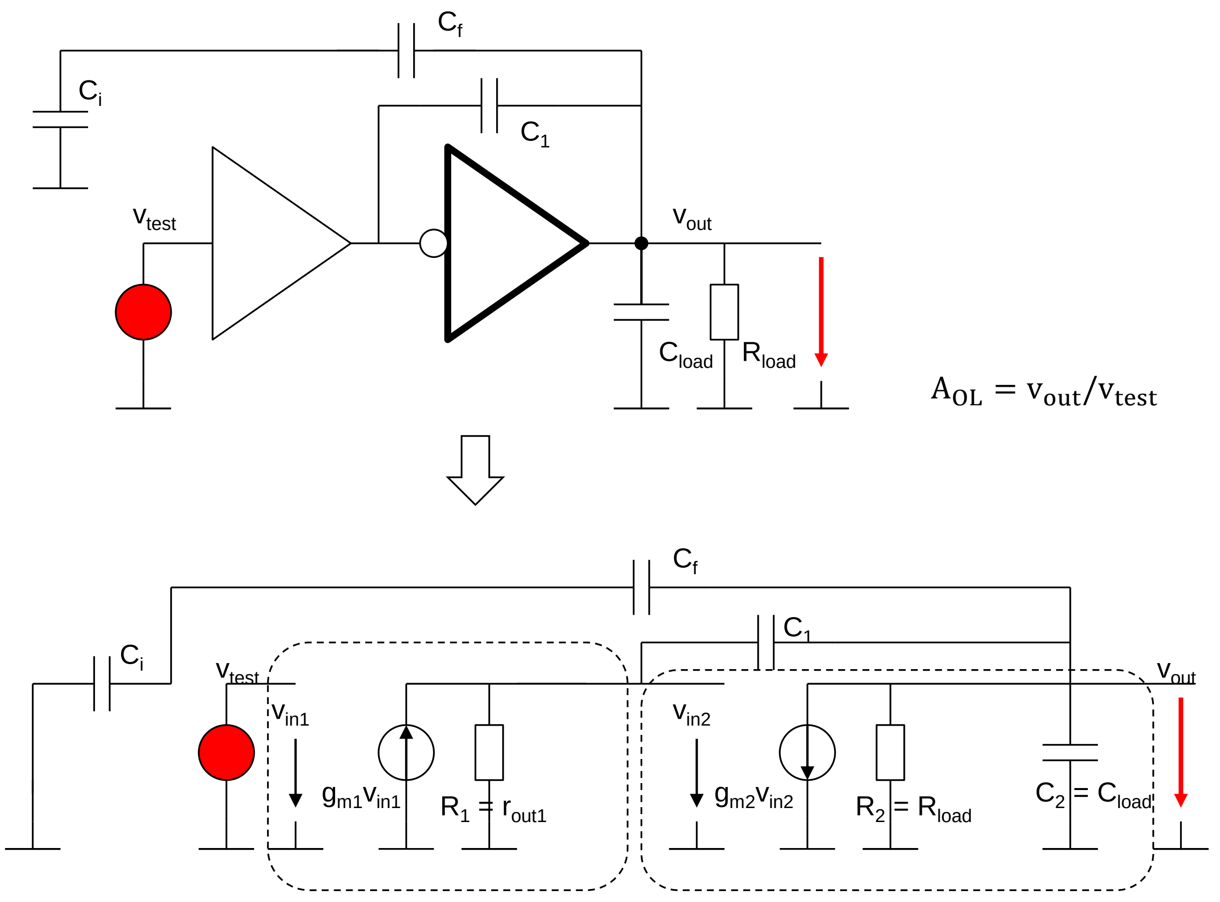


Fig 19: Test circuit for calculating of the open loop gain A_{OL}

If we assume that the serial capacitance $C_f\, C_i \,/\, (C_f + C_i) \sim C_f$ is much smaller than C_{load} and if we replace the current source $g_{m1}\, v_{in1}$ with an equivalent voltage source, we obtain a simplified circuit in Figure 20.

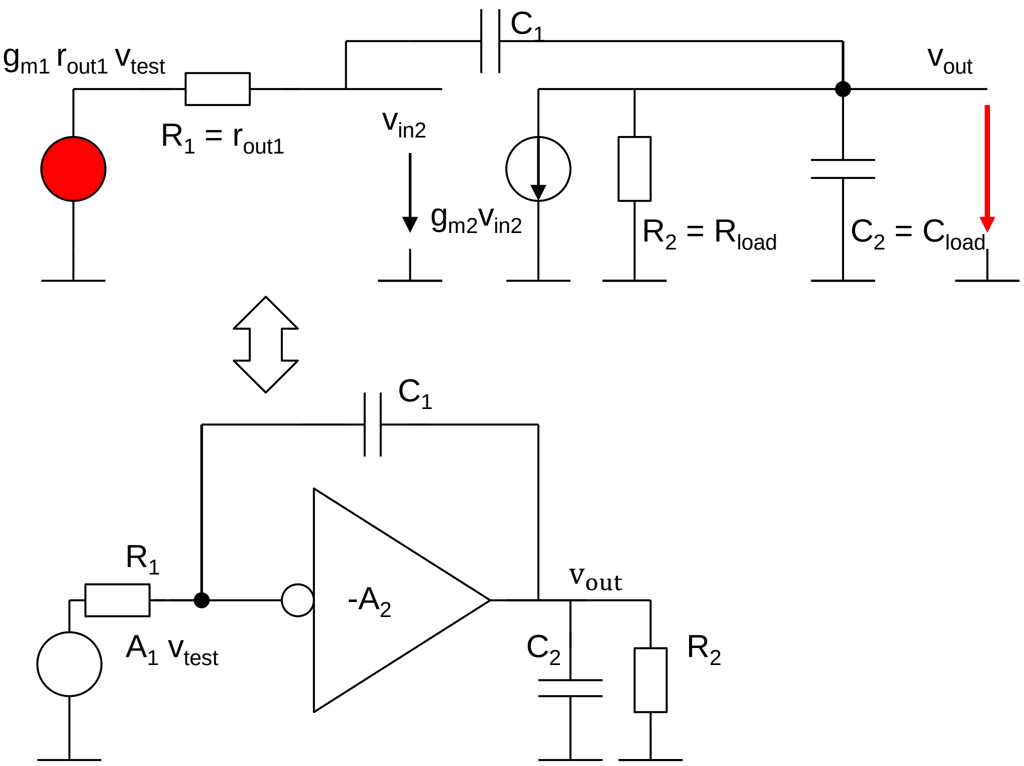


Fig 20: Simplified test circuit for calculating of the open loop gain A_{OL}

The amplification A_{OL} has its own feedback that is created by C_1 and R_1.

We can employ the Mason's formula for A_{OL}:

$$A_{OL}(s) = \frac{A_{IN,AOL}A_{OL,AOL}}{1+\beta_{AOL}A_{OL,OL}} \qquad (47)$$

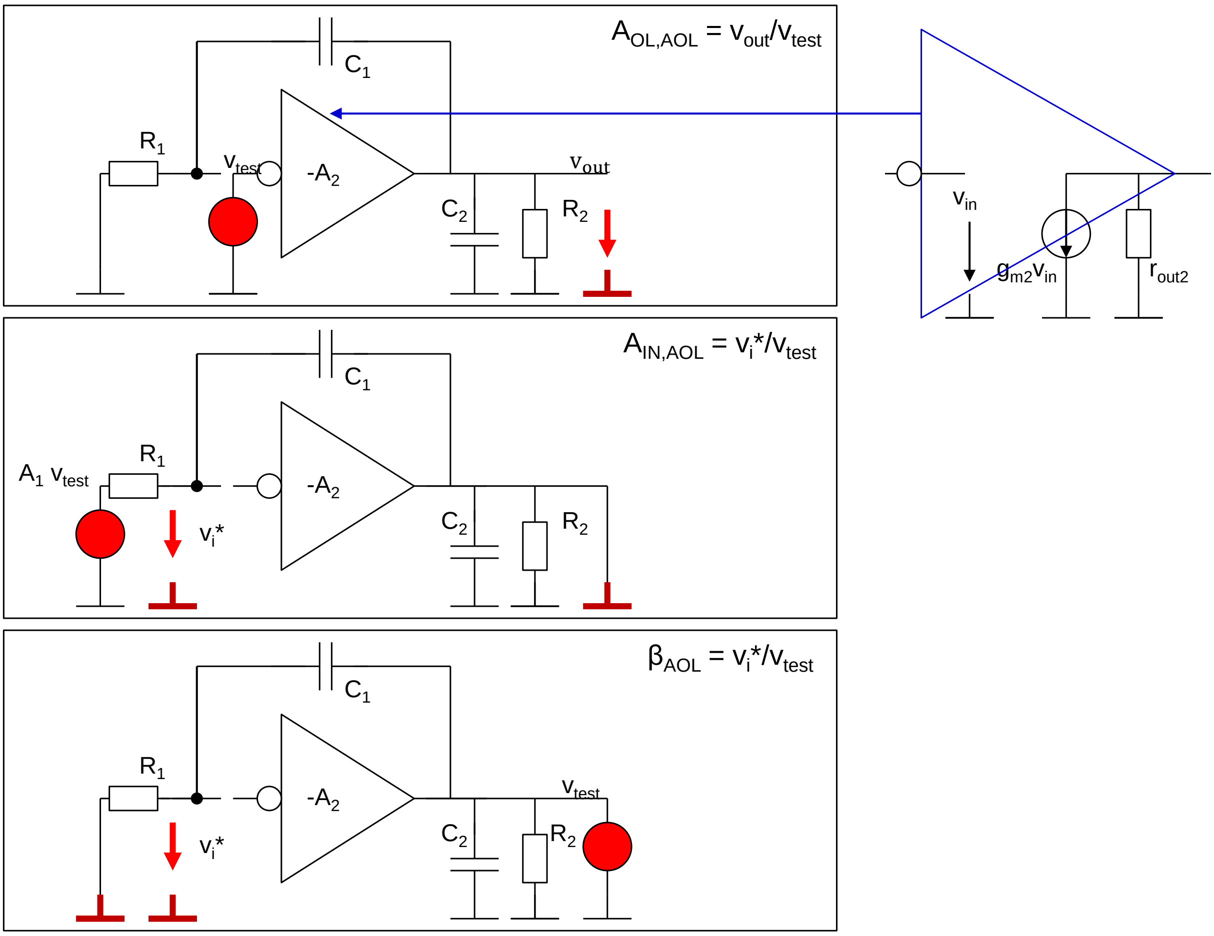


Fig 21: Test circuits for calculating $A_{OL,\,AOL}$ (top), $A_{IN,\,AOL}$ (middle) and β_{AOL} (bottom).

The test circuits for the calculation of factors $A_{OL,\,AOL}$ (top), $A_{IN,\,AOL}$ (middle) and β_{AOL} (bottom) are shown in Figure 21.

The open loop gain $A_{OL,\,AIN}$ is:

$$A_{OL,AOL}(s) = -\frac{g_{m2}R_{load}}{sR_{load}C_{load}+1} \equiv -\frac{A_2}{sT_2+1} \qquad (48)$$

The input gain $A_{IN,AOL}$ is:

$$A_{IN,AOL}(s) = \frac{g_{m1}r_{out1}}{sr_{out1}C_1+1} \equiv \frac{A_1}{sT_1+1} \qquad (49)$$

The time constants T_1 and T_2 are defined as follows:

$T_1 = r_{out1} C_1;\ T_2 = R_{load} C_{load}$

The feedback is:

$$\beta_{AOL}(s) = -\frac{s r_{out1} C_1}{s r_{out1} C_1 + 1} = \frac{sT_1}{sT_1 + 1} \qquad (50)$$

If we insert the factors (48) - (50) in the Mason's formula, we get:

$$A_{OL} = -\frac{\frac{A_1}{1+sT_1}\frac{A_2}{1+sT_2}}{1+\frac{A_2}{1+sT_2}\frac{sT_1}{1+sT_1}} \qquad (51)$$

We can rewrite the formula (51) as follows:

$$A_{OL} = -\frac{A_1 A_2}{1+sT_2+sT_1+sA_2T_1+s^2T_1T_2}$$

Let us sort the factors in the denominator according to their size and try to simplify the expression. The term sA_2T_1 is much larger than sT_1. Therefore sT_1 can be neglected. We assume that sA_2T_1 is much larger than sT_2. The factor $s^2\, T_1\, T_2$ cannot be omitted because it dominates for high frequencies.

A_{OL} is simplified as follows:

$$A_{OL} = -\frac{A_1 A_2}{1+sA_2T_1+s^2T_1T_2}$$

We can add a small term sT_2 / A_2 to the polynomial in denominator - that changes little and allows us to factorize the polynomial. We get:

$$A_{OL} = -\frac{A_1A_2}{\left(1+s\frac{T_2}{A_2}\right)(1+sA_2T_1)} = -\frac{A_1A_2}{(1+s\tau_{2,B})(1+s\tau_{1,B})} \qquad (52)$$

Let us compare A_{OL} in the case when C_1 is connected to ground (case A, without frequency compensation - Figure 22 top) and when C_2 is connected between the input and the output of the second stage (case B, frequency compensation - Figure 22 bottom).

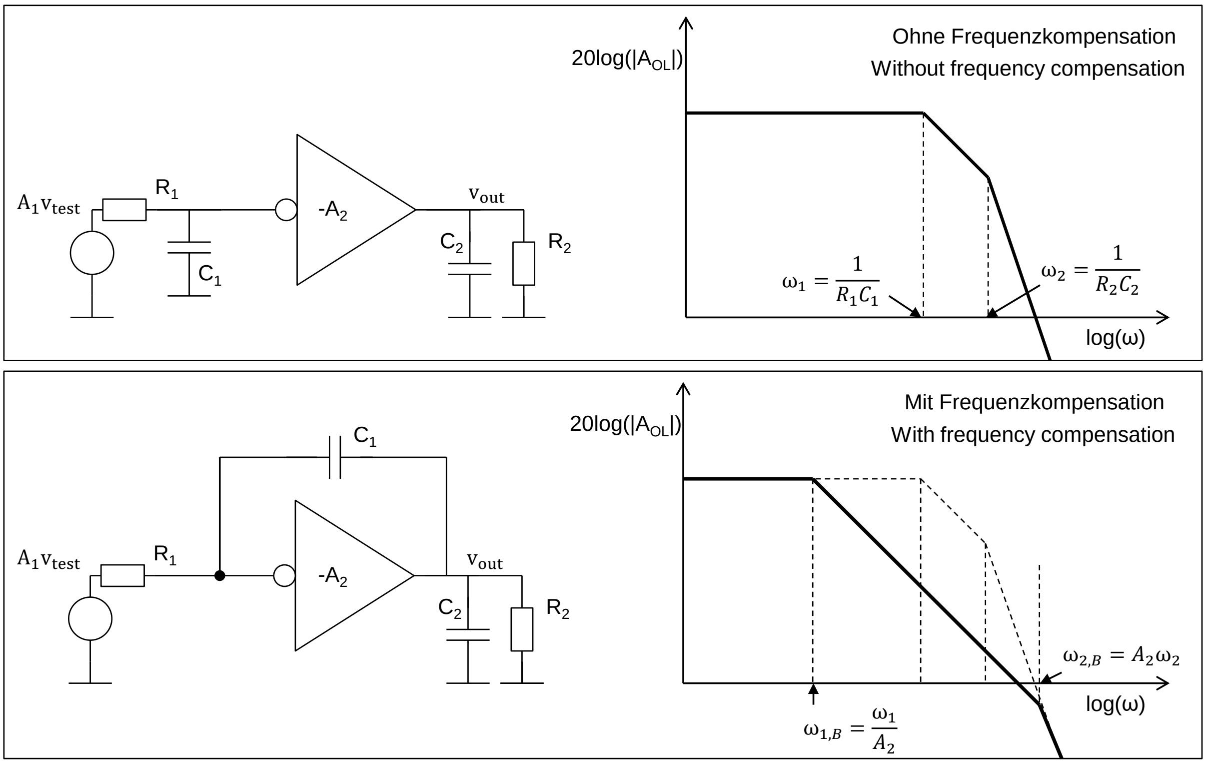


Fig 22: Gain A_{OL} = v_{out} / v_{test} without / with frequency compensation

The frequency compensation separates the poles (*pole splitting*).

The time constants of A_{OL} (s) without frequency compensation are (41):

$\tau_1 = T_1$; $\tau_2 = T_2$

The time constants of A_{OL} (s) with frequency compensation are (52):

$\tau_{1,B} = A_2 T_1$; $\tau_{2,B} = T_2 / A_2$.

One explanation for longer time constants $\tau_{1,B}$ is the *Miller effect*. We will explain this effect in the next paragraph.

In the previous analysis we have neglected the input capacitance of the second stage - the gate-source capacitance of transistor T_{in2}. This neglect is only justified if:

$C_1 \gg C_{gs}$ (52b)

Stability

Let us now calculate the parameters of the circuit C_1, g_{m1} and g_{m2} in order to obtain the rise time of 2 ns (comparable to the single-stage amplifier) and an step response without oscillations.

$$\tau_{r,B} = 2\ \mathrm{ns} \qquad (52c)$$

The condition for an step response without overshoot is (27):

$$\tau_{2,B} < \frac{1}{4}\frac{\tau_{1,B}}{|\beta A_{OL,DC}|}$$

It follows:

$$\tau_{1,B} > \frac{4|\beta A_{OL,DC}| R_{load} C_{load}}{A_2} = 4\beta A_1 R_{load} C_{load} \qquad (53)$$

This condition can be achieved by dimensioning C_1 as follows:

$$\tau_{1,B} = A_2 r_{out1} C_1 > 4\beta A_1 R_{load} C_{load} \Rightarrow C_1 > \frac{4\beta g_{m1}}{g_{m2}} C_{load} \qquad (54)$$

The rise time of step response is:

$$\tau_{r,B} \sim \frac{\tau_{1,B}}{\beta A_{OL,DC}} = \frac{A_2 r_{out1} C_1}{\beta g_{m1} r_{out1} A_2} = \frac{C_1}{\beta g_{m1}} > \frac{4\beta g_{m1} C_{load}}{\beta g_{m1} g_{m2}} = \frac{4C_{load}}{g_{m2}} \qquad (55)$$

From the right-hand side of (55) we obtain the necessary transconductance g_{m2} to achieve the minimum time constant of 2 ns:

$$\frac{4C_{load}}{g_{m2}} = 2\mathrm{ns} \Rightarrow g_{m2} = 4\frac{100\mathrm{pF}}{2\mathrm{ns}} = 200\mathrm{mS}$$

This is the same as our initial value.

Let us now calculate the gate-source capacitance of T_{in2}. To achieve the transconductance of 200 mS we need 200 standard amplifiers in parallel. We assume that a standard amplifier for the second stage has the capacitance C_{gs} of about 10 fF. The total gate-source capacitance of T_{in2} (consists of 200 standard transistors in parallel) is then:

$$C_{gs2} = 200 \times C_{gs,standard} = 200 \times 10\ \mathrm{fF} = 2\ \mathrm{pF}$$

In order for our formulas to be correct, condition (52b) must be fulfilled:

$$C_1 \gg C_{gs} = 2\ \mathrm{pF}$$

We set C1 = 4 pF.

From the left side of (55) we get the transconductance g_{m1} required to actually achieve the time constant of 2 ns and at the same time an step response without oscillations.

$$\frac{C_1}{\beta g_{m1}} = 2\text{ns} \Rightarrow g_{m1} = \frac{4\text{ pF}}{0.02 \times 2\text{ ns}} = 100\text{ mS}$$

Since a standard amplifier has the transconductance of 1 mS, we have to take 100 amplifiers in parallel for the first stage.

The following table summarizes the results:

Generic circuit	**Implemented circuit**	**Value**
R_1	r_{out1}	50kΩ/100
R_2	R_{load}	100Ω
C_2	C_{load}	100pF
C_1	C_1	4pF
g_{m1}	g_{m1}	1mS×100
g_{m2}	g_{m2}	200mS
A_1	$g_{m1}r_{out1}$	50
A_2	$g_{m1}R_{load}$	-20
βA	$\beta A_1 A_2$	20

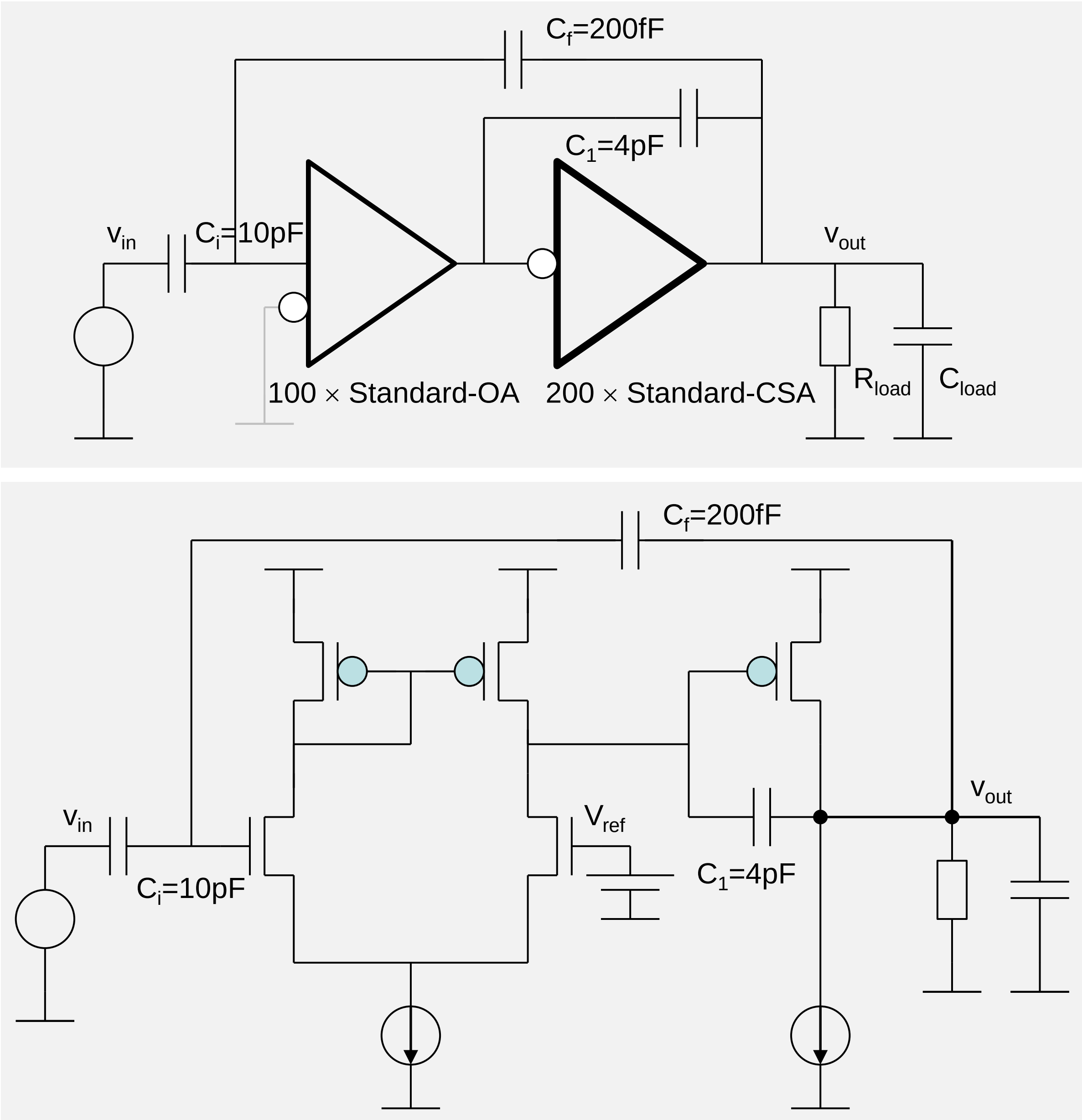
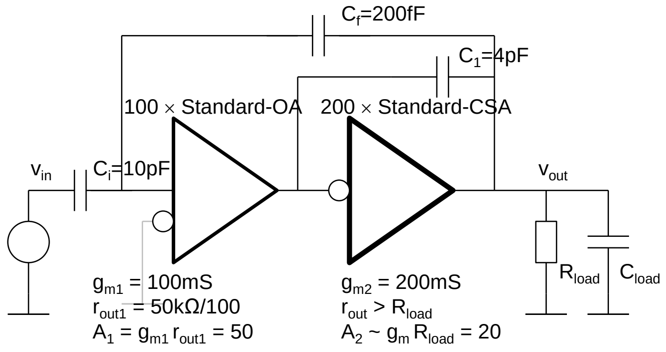


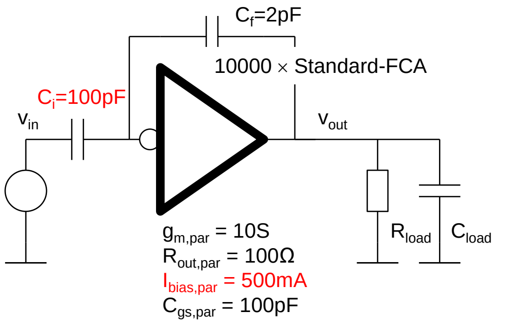
Fig 23: Inverting voltage amplifier with two amplifying stages - complete circuit diagram

Figure 23 shows the complete circuit. The DC voltage source V_{ref} can be implemented as a voltage divider (connected to GND and VDD).

Conclusion: The two-stage amplifier meets the specifications for open loop amplification and has about 33× less power consumption than the single-stage amplifier. The rise time is 2× larger than that of the single-stage amplifier.



Parameter	Wert
C_{load}	100pF
R_{load}	100Ω
A_{FB}	50
A_{OL}	1000
βA	20
τ_r	$4C_{load}/g_{m2}$ = 2ns
I_{bias}	(300 I_0) 30mA



Parameter	Wert
C_{load}	100pF
R_{load}	100Ω
A_{FB}	<50
A_{OL}	500
βA	10
τ_r	$2A_{FB}C_{load}/g_m$=1ns
I_{bias}	(10000 I_0) 500mA

Fig 24: Comparison between voltage amplifiers with two stages and frequency compensation (top) and with one stage (bottom). Disadvantages are marked in red. OA - operational amplifier, CSA - common source amplifier, FCA - folded cascode amplifier.

Miller effect

If the capacitor C is connected between the input and the output of a voltage amplifier with negative gain (-A), its capacitance is increased by ~ A (Figure 25).

A resistor R connected to this circuit creates the time constant

$\tau_1 = R \times A \times C.$

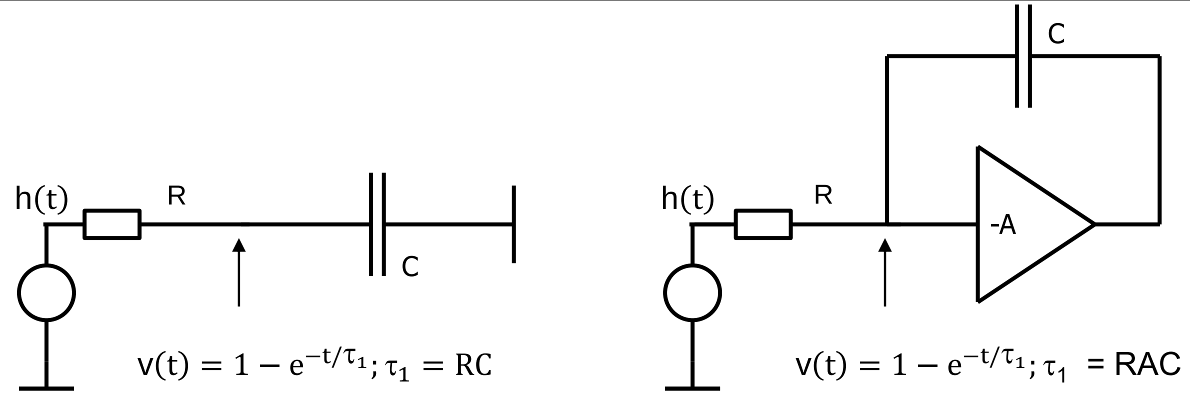


Fig 25: Comparison between time constants. Left: R sees capacitance C. Right: R sees larger capacitance.

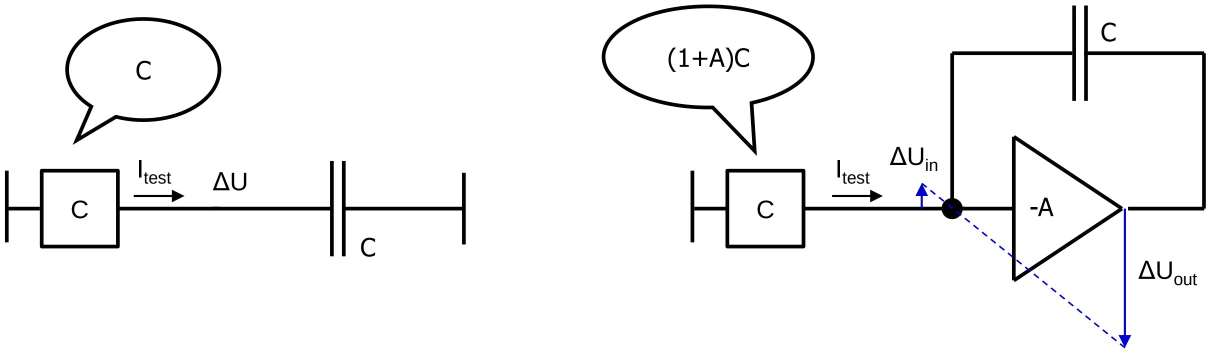


Fig 26: Miller effect, increase of C

Figure 26 shows why the capacitance is increasing.

A "C-Meter" measures the capacitance by generating a current I_{test} and by measuring how much the voltage on the capacitor (ΔU) has risen after time ΔT - Figure 26 (left). The capacitance can be determined with the following formula:

$$I_{test} = C\frac{\Delta U}{\Delta T} \Rightarrow C = I_{test}\frac{\Delta T}{\Delta U}$$

Smaller voltage change means greater capacitance.

Let us now assume that exactly the same current flows into the capacitor with amplifier - Figure 26 (right).

The voltage between the capacitor electrodes after the time ΔT is the same as when we have a capacitor without amplifier:

$$\Delta U = \frac{I_{test}}{C}\Delta T$$

The voltage at the input of the amplifier changes by approximately:

$$\Delta U_{in} = \frac{\Delta U}{A+1} \ll \Delta U$$

The voltage at the output changes by:

$$\Delta U_{out} = -\Delta U \frac{A}{A+1} \sim \Delta U$$

The difference ΔU_{in} - ΔU_{out} is U.

Since the C-meter measures a voltage change that is A + 1 smaller than ΔU, it interprets as a capacitance that is A + 1 larger than C.

If we connect a resistor to the input of the amplifier with C, the amplifier behaves as a large capacitor with the capacitance (A + 1) C. The time constant is correspondingly large. Such an increase of the capacitance is called the Miller effect.

Let us look again at the circuit of Figure 20 and try to understand its behaviour.

The transfer function was (52)

$$A_{OL} = -\frac{A}{\left(1 + s\frac{T_2}{A_2}\right)(1 + sA_2T_1)} = -\frac{A}{\left(1 + s\tau_{2,B}\right)\left(1 + s\tau_{1,B}\right)}$$

with

$T_1 = R_1 C_1$; $T_2 = R_2 C_2$; $A_2 = g_{m2}R_2$

The derivation of this transfer function was relatively long. Since we introduced the Miller effect, we can better understand the time constants. The circuit of Figure 20 can have been drawn in a simplified manner as in Figure 27.

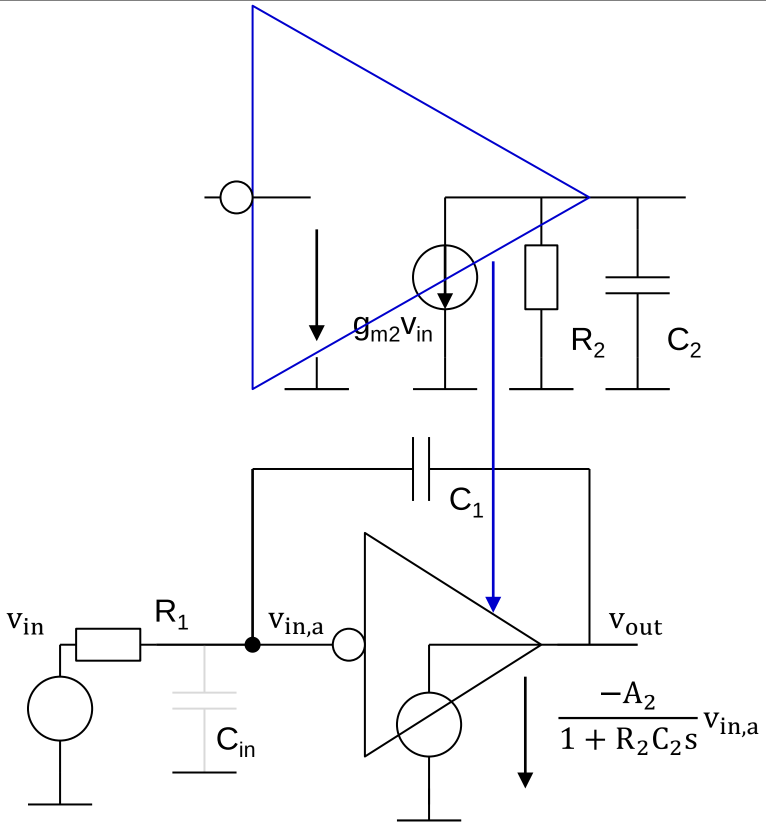


Fig 27: Integrator

The first time constant $\tau_{1,B}$, B arises because R1 is connected to the capacitors. As described above, the capacitance C_1 is increased by a factor of $1 + A_2 \sim A_2$. Resistor R_1 sees capacitance A_2 C_1. The time constant is $\tau_{1,B}$, B is:

$$\tau_{1,B} = R_1 C_1 A_2$$

The explanation for shorter time constant $\tau_{2,B}$ is the feedback. Without feedback, the time constant would be $T_2 = R_2C_2$. We have seen in previous lectures that negative feedback influences the output resistance (or output impedance) (Blackman's formula) by reducing the impedance by $1 - \beta A\ (i\omega)$. If $\beta A\ (i\omega)$ is a real number $\beta A\ (i\omega) \equiv \beta A$, the time constant caused by the output resistance is also by $1 - \beta A$ smaller. In our example this means:

$$\tau_{2,B} = \frac{T_2}{1-\beta A}$$

It holds $\tau_{2,B} < T_1$. For $\omega > 1/T_1$ the loop gain is real number:

$$\beta A(i\omega) \equiv \beta A = -A_2$$

R_1 can be neglected in the serials connection of R_1 and C_1.

Therefore:

$$\tau_{2,B} = \frac{T_2}{-\beta A} = \frac{T_2}{A_2}$$

If we have an input capacitance C_{in} (this capacitance would be e.g. the gate-source capacitance of the input transistor), the time constants change as follows:

Resistor R_1 now sees the increased capacitance A_2C_1 and C_{in} in parallel. Therefore the first time constant is:

$$\tau_{1,B} \sim R_1(A_2C_1 + C_{in}) = A_2T_1\left(1 + \frac{C_{in}}{C_1A_2}\right)$$

The capacitance C_{in} leads to a change in $\beta A(s)$. It holde for $\omega > 1/T_1$:

$$\beta A(s) \equiv \beta A \sim -A_2\frac{C_1}{C_1 + C_{in}}$$

The second time constant is then:

$$\tau_{2,B} \sim \frac{T_2}{-\beta A} = \frac{T_2}{A_2}\left(1 + \frac{C_{in}}{C_1}\right)$$

We see that the input capacitance has a relatively strong influence on the second time constant.

The circuit consisting of a voltage amplifier and capacitive feedback (Figure 27) is important. It is a slow voltage amplifier, with a large DC gain ($-A_2$) and a long time constant $A_2R_1C_1$. For the time intervals that are significantly shorter than the time constant τ_1, the circuit behaves like an integrator.

The following applies:

$$u_{out}(s) = \frac{A_2}{(sA_2R_1C_1+1)\left(s\frac{T_2}{A_2}+1\right)}u_{in}(s) \xrightarrow{A_2=\infty} u_{out}(s) = \frac{u_{in}(s)}{sR_1C_1} \quad (56)$$

Or in time domain:

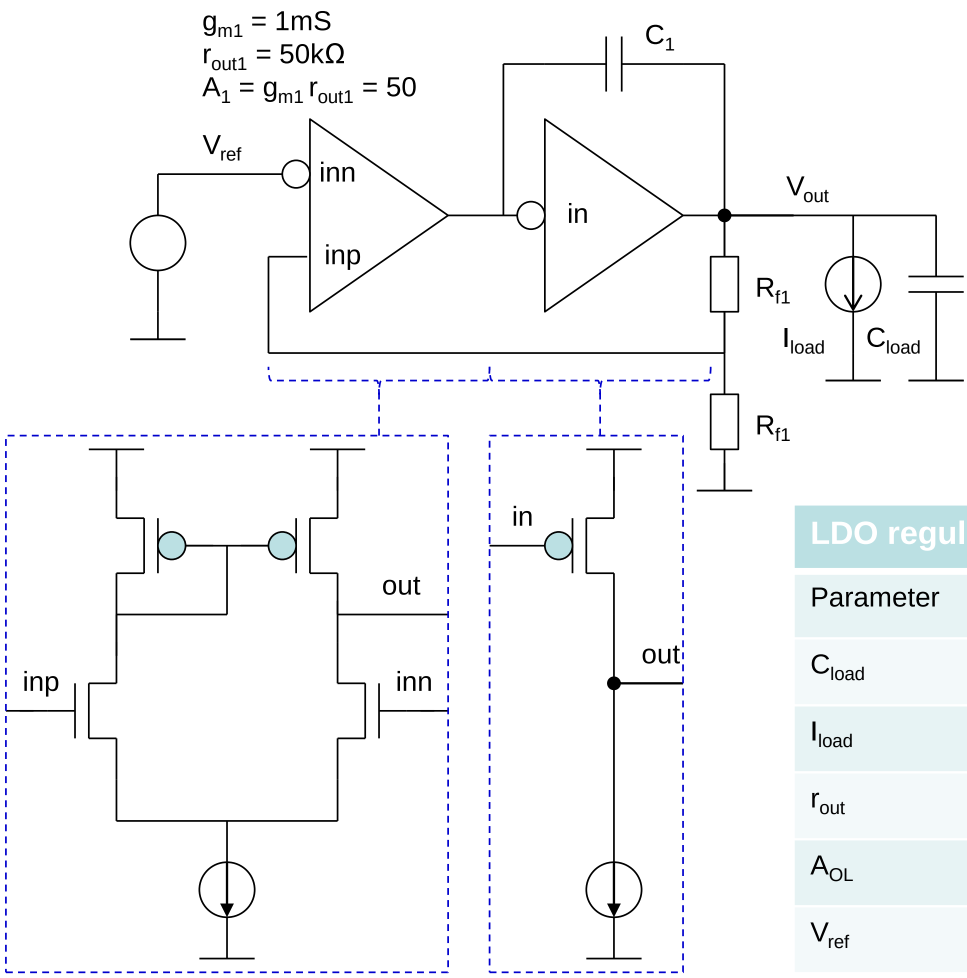
$$u_{out}(t) = \frac{1}{RC}\int u_{in}(t)dt \quad (57)$$

τ is the time constant of the amplifier. In the case of the second amplifier stage:

$$u_{out}(t) = \frac{1}{R_1C_1}\int u_{in}(t)dt \quad (58)$$

Linear regulator

Figure 28 shows the linear regulator implemented as a two-stage amplifier with frequency compensation.



LDO regulator	
Parameter	Wert
C_{load}	10nF
I_{load}	0-100mA
r_{out}	0.1Ω
A_{OL}	1000
V_{ref}	1V

Fig 28: Linear regulator with a two-stage amplifier and frequency compensation

The first stage (an operational amplifier with a current mirror) has the same dimensions as in the voltage amplifier:

g_{m1} = 1 mS

r_{out1} = 50 kΩ

$A_1 = g_{m1}\, r_{out1} = 50$

The second stage is based on the common source amplifier with an open loop gain of 50.

The overal gain is then:

$A = A_1\, A_2 = 2500.$

In order to simplify the analysis et us choose the following values:

$R_{f1} = 0$ and $R_{f2} = \infty$.   (59)

We will determine the transconductance g_{m2} in order to achieve an output resistance with feedback of 0.1 Ω:

$r_{out} = 0.1\ \Omega$.   (60)

First, let us calculate the DC voltage V_{out} using Mason's formula. Figure 29 shows the test circuits for calculating A_{IN}, β and A_{OL}.

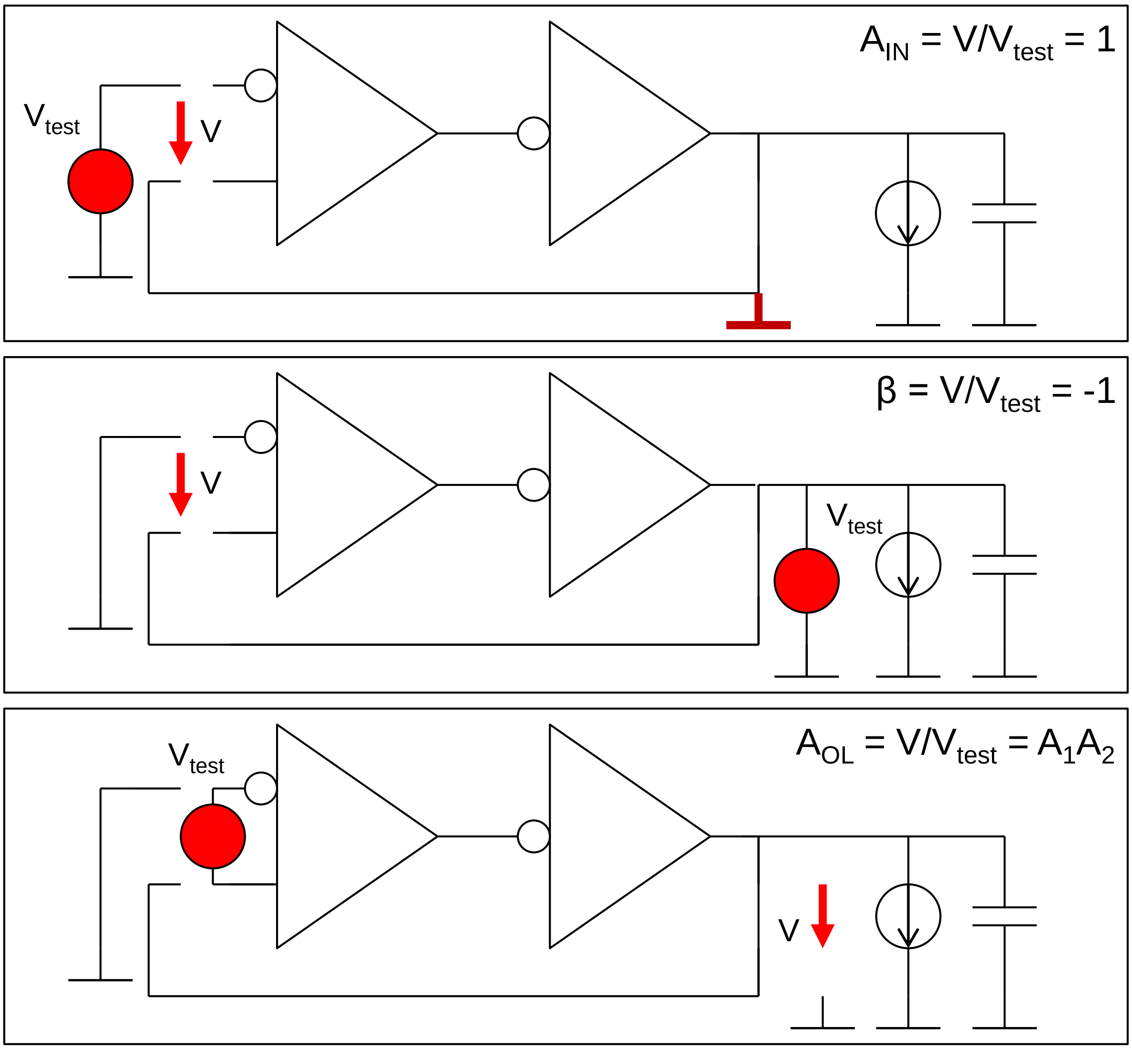


Fig 29: Linear regulator - test circuits for A_{IN}, β and A_{OL}

The following applies:

$A_{IN} = 1$ (Figure 29, top),

$\beta = -1$ (Figure 29, middle),

$A_{OL} = A_1A_2$ (Figure 29, bottom)

If we insert these terms into Mason's formula, we obtain:

$$V_{out} = \frac{A_1A_2}{1+A_1A_2} V_{in} \sim V_{in} \qquad (61)$$

Let us calculate the output resistance (small signal resistance). We use Blackman's formula.

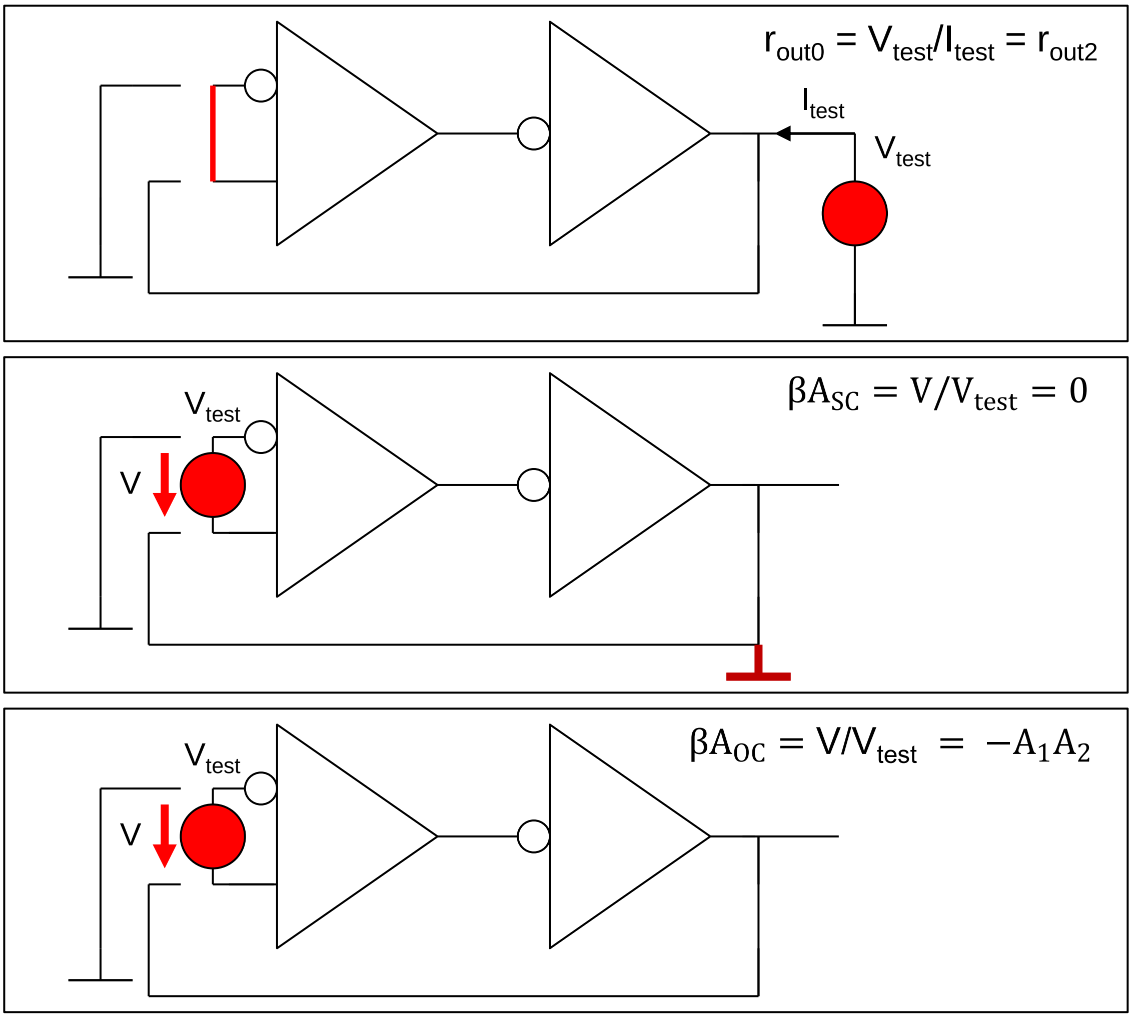


Fig 30: Linear regulator - test circuits for r_{out0}, βA_{SC} and βA_{OC}

$$r_{out} = r_{out0}\frac{1-\beta A_{SC}}{1-\beta A_{OC}} \quad (62)$$

Figure 30 shows the test circuits for calculation of r_{out0}, βA_{SC} and βA_{OC}.

The factors have the following values:

$$r_{out0} = r_{out2};\ \beta A_{SC} = 0;\ \beta A_{OC} = -A_1 A_2 \quad (63)$$

If we insert these terms into Blackman's formula (61) we get:

$$r_{out} = \frac{r_{out2}}{A_1 A_2} = \frac{1}{A_1 g_{m2}} \quad (64)$$

If we assume $A_1 = 50$, we can calculate the required transconductance g_{m2}, which leads to $r_{out} = 0.1\ \Omega$.

$$0.1\Omega = \frac{1}{50 g_{m2}} \Rightarrow g_{m2} = 200\text{mS} \qquad (65)$$

We must connect 200 standard amplifiers (each gm = 1mS) in parallel.

Remember that the second amplifier stage has $r_{out} = 250\Omega$.

The feedback enables us to achieve a significantly lower output resistance.

Stability

Let us dimension C_1 so that there are no oscillations. From the formula (54) we calculate:

$$C_1 > \frac{4\beta g_{m1}}{g_{m2}} C_{load} = 4\frac{1\text{mS}}{200\text{mS}} 10\text{nF} = 200\text{pF} \qquad (66)$$

The rise time of step response can be calculated using (55):

$$\tau_r = \frac{C_1}{\beta g_{m1}} > \frac{4C_{load}}{g_{m2}} = \frac{4 \times 10\text{nF}}{200\text{mS}} = 200\text{ns} \qquad (67)$$

The time constant τ_r tells us among others how quickly the regulator can regulate the output voltage if I_{load} changes.

We can achieve a faster rise time by increasing g_{m2} and g_{m1}.

Input capacitance

It can be also calculated using Blackman's formula that the input source sees a very small capacitive load:

$$C_{in} = \frac{C_{gs,par}}{1+A_1 A_2} \quad (68)$$

$C_{gs,ser}$ is the series capacitance of the C_{gs} capacitances of two input transistors in the operational amplifier. This result holds for frequencies smaller than $1/\tau_r$.

How can we explain that the input capacitance is smaller than $C_{gs,ser}$? The feedback regulates $V_{ref} = V_{out}$ so that the charge stored in $C_{gs,ser}$ does not change. Because of this, the input source does not see the effect of $C_{gs,ser}$ (Figure 31).

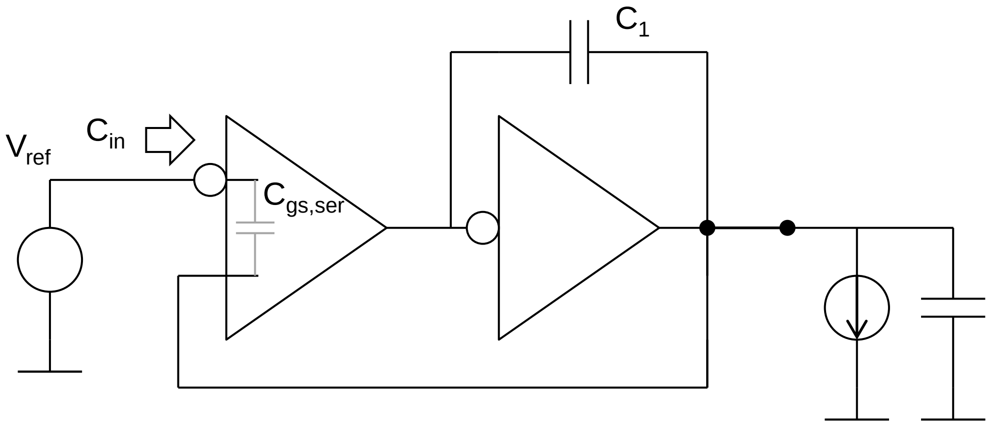
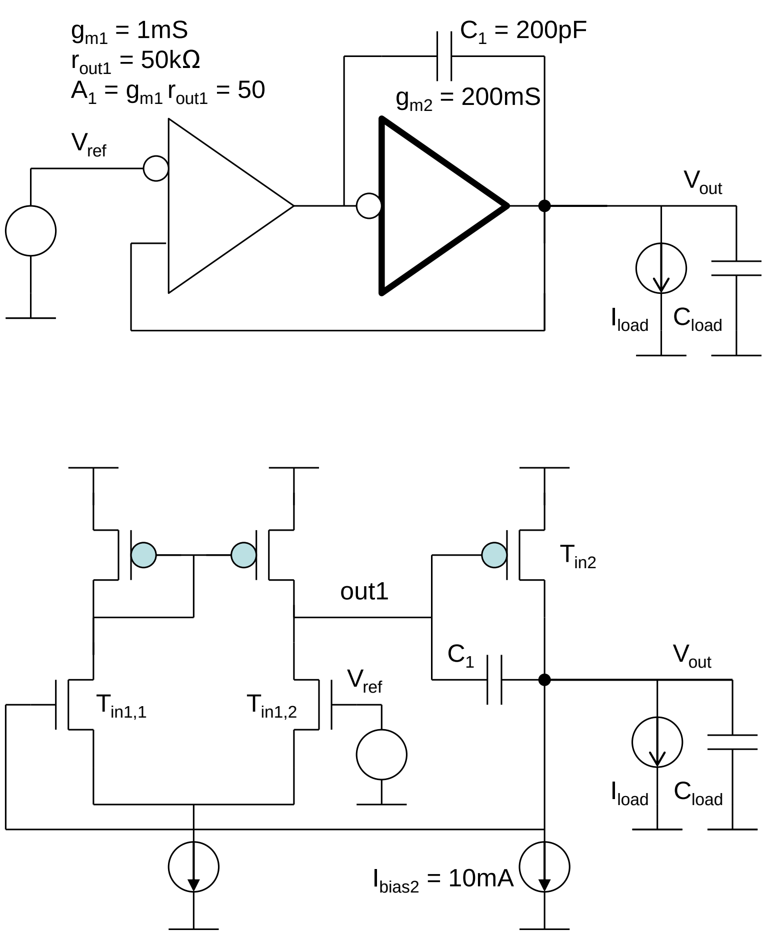


Fig 31: Input capacitance



LDO regulator	
Parameter	Value
C_{load}	10nF
I_{load}	0-100mA
r_{out}	0.1Ω
A_{OL}	1000
V_{ref}	1V
g_{m1}	1mS
g_{m2}	200mS
C_1	200pF
τ_r	200ns

Fig 32: Linear regulator - complete circuit diagram

Figure 32 shows the complete circuit diagram of the linear regulator.

DC analysis

So far we have limited ourselves to the small signal analysis and have not taken into account that the load current can influence the operating point of the second amplifier stage.

Note that the current I_{load} also flows through the transistor T_{in2}. The transconductance of the transistor T_{in2} (g_{m2}) is proportional to I_{load}, for I_{load} > 10 mA.

This has a positive effect on the circuit. A_2 gets larger and rout gets smaller.

Transistor T_{in2} must be dimensioned in such a way (W / L must be large enough) that for $I_{load} = I_{load, max}$ its $| V_{gs} |$ does not get too large. Otherwise it could happen that $T_{in1,2}$ no longer works in saturation and that A_1 becomes small.